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A Modified Bridgeless Converter for SRM Drive with Reduced Ripple Current

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ABSTRACT

A Single Phase Switched Reluctance Motor is more popular in many industrial purposes for high speed applications because of its robust and rugged construction. For low cost and variable speed drive applications SRM are widely used.Due to doubly salient structure of motor, the torque pulsations are high when compared to other sinusoidal machines. The major drawback in using SRM drive is torque pulsations and increased number of switching components. In order to overcome these drawbacks, a bridgeless Single Ended Primary Inductor Converter (SEPIC) is proposed. The major advantages of this converter are continuous output current, smaller voltage ripple and reduced semiconductor current stress when compared to the conventional SEPIC converter. The ripple free input current is obtained by using additional winding of input inductor and auxiliary capacitors. To achieve high efficiency, active power factor correction circuits (PFC) are employed to precise the power factor. Further, the unity power factor can be obtained by making the input current during switching period proportional to the input voltage is proposed. The proposed system consists of reduced components and it is also capable of reducing the conduction losses. The working principles and the waveforms of proposed converter are analyzed. To analyze the circuit operation, theoretical analysis and simulation results are provided. Finally, the comparison between the waveforms of conventional SEPIC and proposed system is presented by using MATLAB/Simulink tools.

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1. INTRODUCTION

In the past two decades, Switched reluctance Motor (SRM) drive has recently developed for many industrial applications. The SRM drive has more advantages over induction motor or other types of special machines such as permanent magnet synchronous motor. The advantages such as lower price, improved performance, better reliability, comparable or better efficiency, lower volume and ease of production and storage when compared to various AC and DC motor drives [1]. The major drawbacks of SRM drive is large torque ripples due to its discontinuity in the generated torque. By using phase current overlapping method, the torque ripples can be reduced to a small extent. Torque ripples also produced due to back emf produced during commutation of each phase causes the stator current to fall behind the reference current. After the occurrence of reference current, the phase current reaches zero causing a negative torque and high torque ripples produced by SRM drive. Therefore, converters which are used in SRM drive are to be modified to

have fast commutation ability for its desirable operation [4], [6] and [8]. In most of the AC-DC converters used for constant speed drive applications [5] requires many active power factor correction circuits (PFC) due to the demand in high efficiency and low harmonic pollution.

Generally, a full-bridge diode rectifier is employed at the input current path so that it produces more conduction losses during low line. To solve this problem, bridgeless converters are proposed to avoid input bridge diode and the conduction loss [2]. A bridgeless SEPIC converter can act as both buck and boost mode as per the applications and most commonly used to reduce input current ripple. For low voltage switched mode power supplies and SRM drives, it requires low voltage when compared to peak voltage of input voltage [2]. So, a bridgeless buck converter is proposed to obtain output voltage which is lower than the peak value of input voltage for SRM drive applications [9]. Recently many researches are going on to overcome the problems associated with efficiency and torque ripples of SRM drives. For example, Krishnan et al. [3] proposed a new low cost converter with a dump resistance. In this type of converter, the voltage across the capacitor depends on dump resistance and it uses single switch at each phase [7]. But the major drawback is phase inductance energy gets wasted in dump resistance and it causes low efficiency. Bagherian et al. [1] proposed a new c-dump converter for SRM drive. This converter employs capacitor in series with the bifilar windings and energy discharge is faster when compared to conventional bifilar type converters. The disadvantage of this converter is that the use of large value capacitor and inductor in the dump circuit increases the voltage rating twice the bus voltage. The monitoring and control of dump capacitor voltage in this type of converter is also difficult. Jae –Won Yang et al. [3] proposed a bridgeless SEPIC converter with reduced input current ripple. The major difference between this converter and previously explained converters is that it has no input bridge diode. So, it produces reduced conduction losses and power factor can be improved compared to conventional converters. The reference [10-13] offers a various SRM drive topologies to overcome the torque ripple problems and improve the performance of drive. In Figure 1, a bridgeless SEPIC converter with ripple-free input current is proposed in [2] is shown. Here, an auxiliary circuit consists of input inductor and capacitor to reduce the input current ripple. In general, coupled inductors are used to minimize the input current ripple [2].

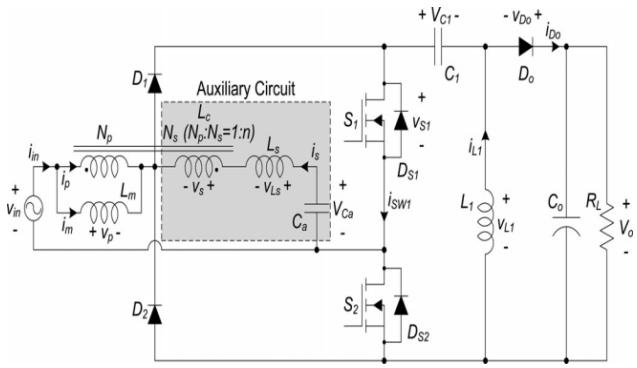

Figure 1. Proposed bridgeless SEPIC converter

2. ANALYSIS OF THE BRIDGELESS SEPIC CONVERTER

The auxiliary circuit consists of N_s as an additional winding of the input inductor L_c, an auxiliary inductor L_s and a capacitor C_a. TheL_c as a coupled inductor can be exhibited as a magnetizing inductance L_m and turns ratio of the ideal transformer is$1{:}\,n$ $(n = N_s/N_p)$. Figure 2(b) shows the proposed gate signals for the switches. One switch is continuously turned ON and current through the intrinsic body diode is forced to run via channel of the switch. So, the conduction loss on the switch can be reduced and improved efficiency. The value of the capacitance C_a is assumed to be high and during switching period V_{Ca} is considered as voltage source. By volt-second balance law, under steady state the average inductor voltage is zero and average capacitor voltage V_{ca} is equal to the input voltage V_{in}during switching period. Likewise, average capacitor voltage V_{C1} is equal to the input voltageV_{in}. The diodes D_1 and D_2 act as input rectifiers. The intrinsic body diodes D_{S1} and D_{S2} of the switches S_1 and S_2simultaneously gets operated by the gate signals as shown in Figure 2(b). The components such as C_1, L_1, D_o, C_o are same as that of conventional converter.

The operation of the converter is similar in both half cycles of the input voltage. So, it is sufficient to analyze the positive half cycle of the input voltage during one switching period. Before the main switch gets turned ON, the output diode D_o is in OFF mode during discontinuous conduction mode (DCM). In order

to consider the output voltageV_o as a constant, the value of output capacitor C_o is considered as adequately large. During the switching period T_s, the input voltage is assumed to be constant which is equal to V_{in}.

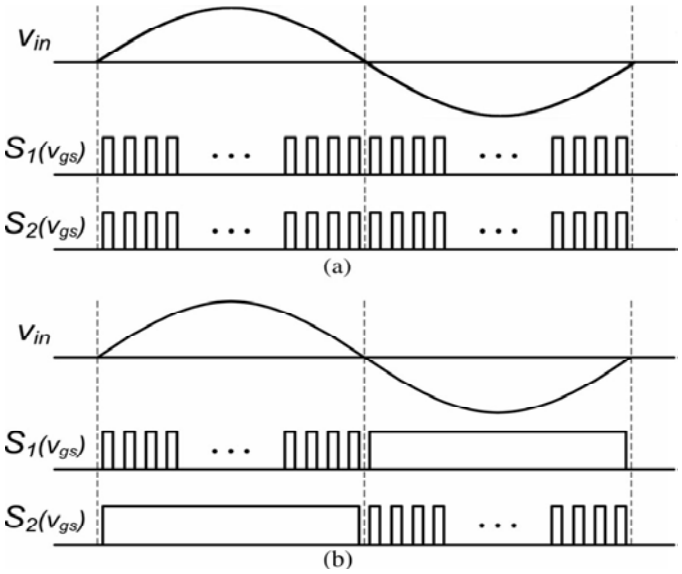

Figure 2. (a) Gate drive signals for S_1 and S_2 (b) Proposed gate signals for S_1 and S_2

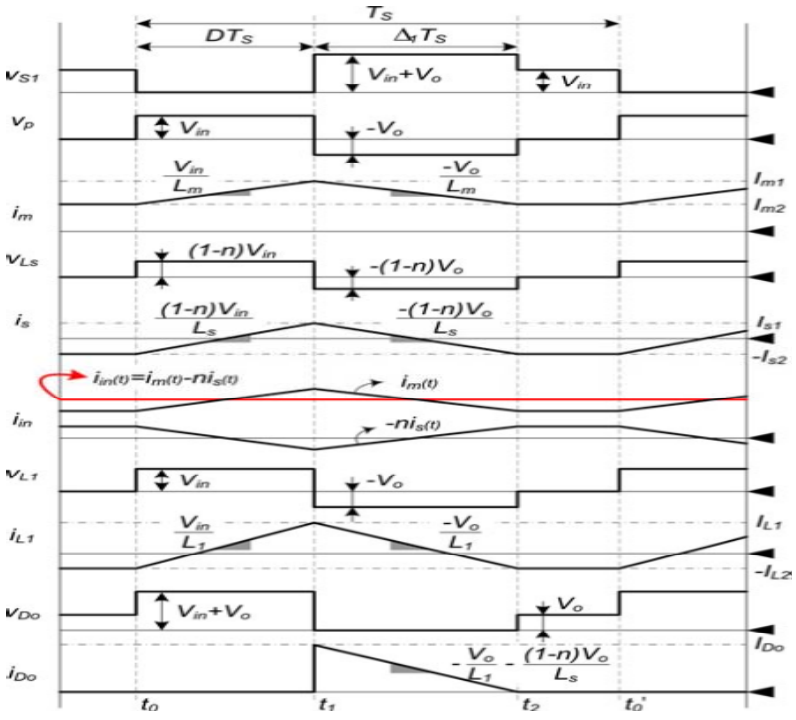

Figure 3. Waveforms of the Proposed Converter

The waveform of the proposed system is shown in the Figure 3. Here, the magnetizing currenti_m varies from the maximum value of I_{m1} to the minimum value of I_{m2} and also the inductor current i_s varies from the maximum value of I_{s1} to the minimum value of $-I_{s2}$. At one switching periodT_s, the operation of the proposed converter can be divided into three modes of operation. The various operating modes of the converter are shown in the Figure 4. The switch S_1 and diode D_o is turned OFF and the switch S_2 is

conducting before the instant T_0. The sum of freewheeling currents I_{s2} and I_{L2} gives the value of the input current.

3. MODES OF OPERATION OF SEPIC CONVERTER

Mode 1 [t_0, t_1]: In Figure 4(a), switch S_1 is turned ON and switch S_2 is still conducting at the time instantt_0. The magnetizing current i_m increasesfromits minimum value of I_{m2} linearly with slope of $\frac{V_{in}}{L_m}$ due to the voltage v_p across magnetizing inductance is V_{in}.

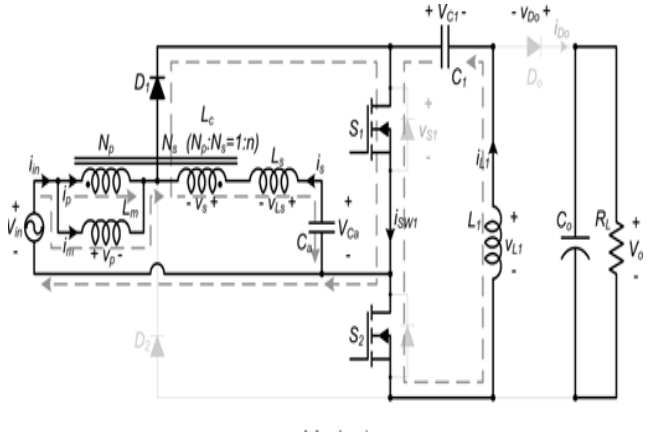

Figure 4(a). Operation of Mode 1

The voltage V_{Ls} across L_s is $(1-n)V_{in}$ and therefore, the current i_s increases from its minimum value -I_{s2} linearly with a slope of $(1-n)\, i_n/L_s$.

Mode 2 [t_1, t_2]: In Figure 4(b), switch S_1 is turned ON and switch S_2 is still conducting at the time instant t_1. The magnetizing current i_m decreases fromits minimum value of I_{m1} linearly with slope of $-\frac{V_o}{L_m}$ due to the voltage v_p across magnetizing inductance is-V_o.
The voltage V_{Ls} across L_s is $-(1-n)V_o$ and therefore, the current i_s decreases from its maximum value I_{s1} linearly with a slope of$-(1-n)\, V_o/L_s$.

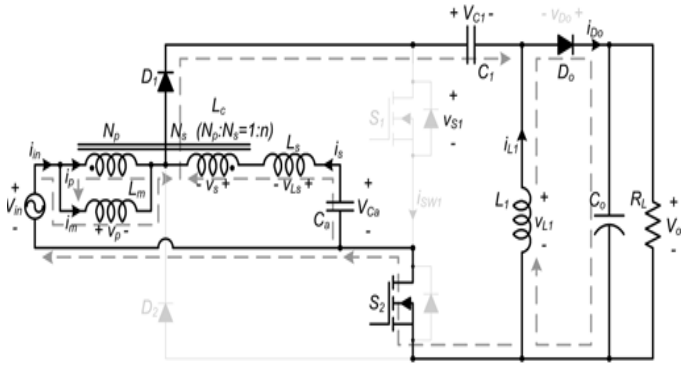

Figure 4(b). Operation of Mode 2

Mode 3 [t_2, t_0[1]]: In Figure 4(c), the current i_{Do}becomes zero and the diode D_o is turned OFF at the instant t_2. The input current i_{in} is the sum of freewheeling currents I_{s2} and I_{L2}. The input current is given as $i_{in} = i_m - ni_s = -i_s - i_{L1}$.

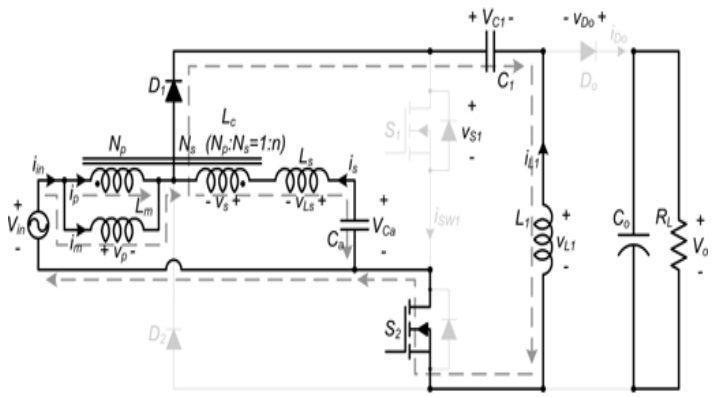

Figure 4(c). Operation of Mode 3

4. DESIGN VALUES

The proposed converter is simulated by using MATLAB with the specifications and parameters as follows: v_{in}=130 V_{ac}, f_L=60 Hz, f_{sw} = 100 kHz, D = 0.25, L_m= 600 μH, n = 0.7, L_s= 127 μH, L_1= 63 μH, C_a= 0.3 μF, C_1 = 440μ F, C_o= 880 μF, and R_L= 77 Ω.

5. RESULTS AND ANALYSIS

The Figure 5 shows the Simulink model of conventional SEPIC converter. The output from the SEPIC is given as an input to SRM after inverted by inverter.

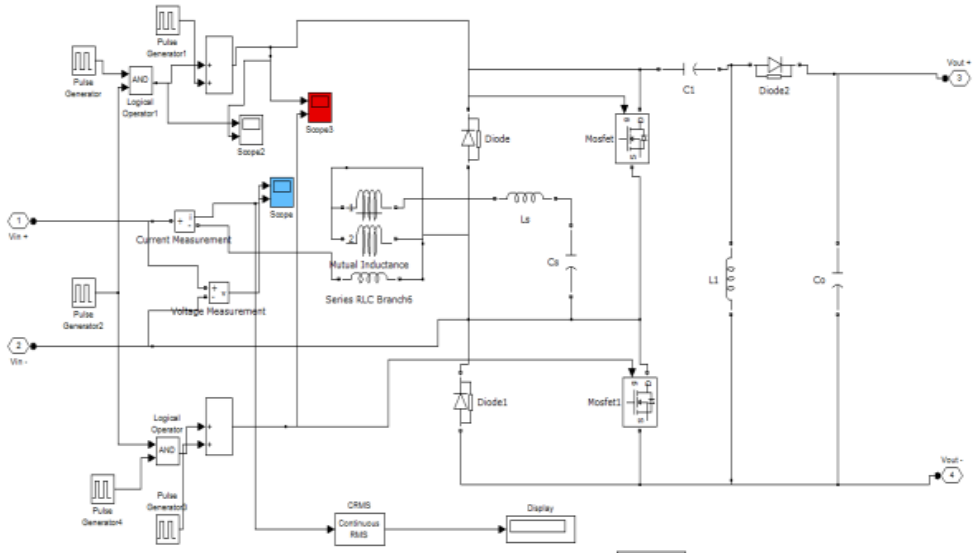

Figure 5. Simulink Model of Conventional SEPIC

The Figure 6 shows the output waveform of conventional system. It depicts that the current and torque ripple produced is more. So, the performance of the motor is greatly affectedby the converter. The input voltage consists of more ripple current due to the presence of an input bridge diode at the SEPIC. The gate pulses from the pulse generator are used to trigger the MOSFET. The turn ON and turn OFF time of the MOSFET enables the inductor L to charge and discharge. The output is displayed taking flux, torque, current with reference to time. The output waveform implies that more current and torque ripple produced during simulation.

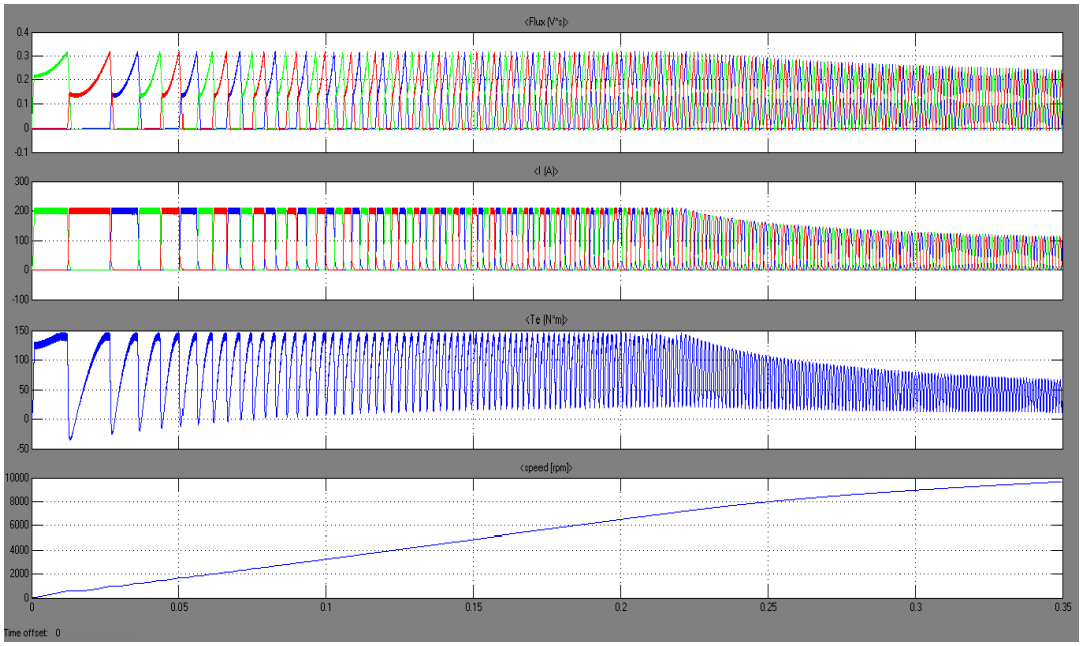

Figure 6. Output Waveform of Conventional SEPIC

The simulink model of a proposed bridgeless SEPIC converter is shown in the Figure 7. Initially, AC voltage source is used as input.

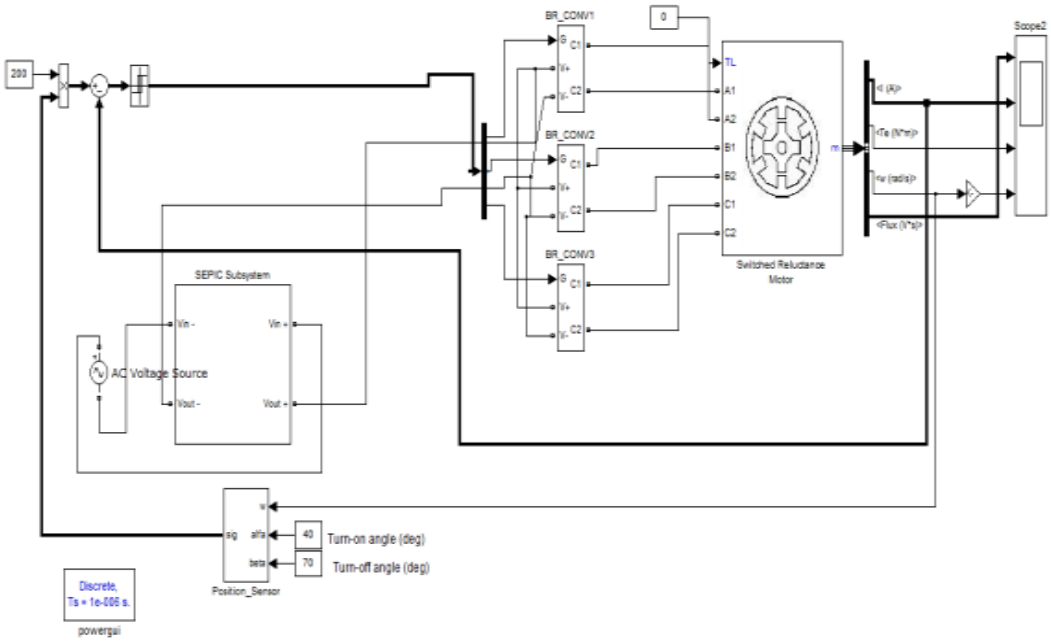

Figure 7. Simulink Model of Proposed Bridgeless SEPIC Converter

This AC voltage source is given to the bridgeless SEPIC converter to produce DC with reduced ripple current, which is given to SRM after converting into AC by an inverter.

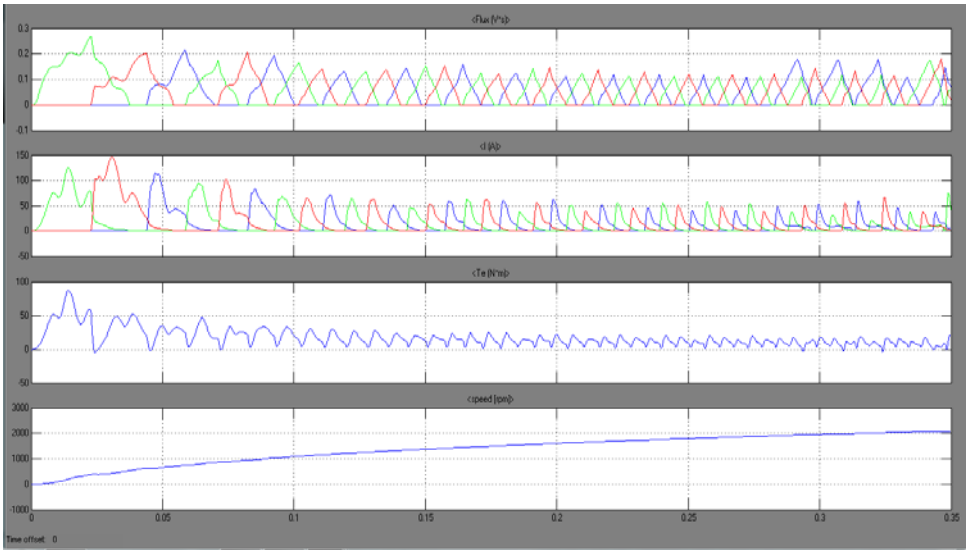

Figure 8. Output Waveform of Proposed Bridgeless SEPIC

The output waveform implies that current and torque ripple produces is reduced during simulation compared to conventional system is shown in the Figure 8. The outputs are displayed taking flux, current, torque and speed with reference to time.

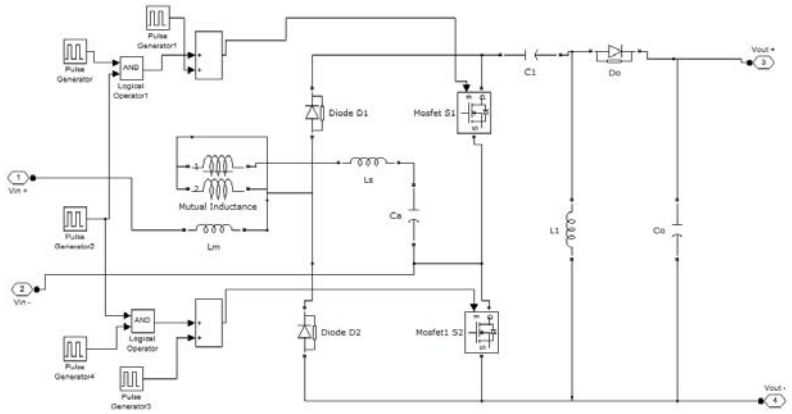

Figure 9. Model of Proposed Bridgeless SEPIC Converter

The subsystem model of proposed bridgeless SEPIC converter is shown in the Figure 9. The output of conventional and the proposed bridgeless SEPIC converter are given and the reduced output current ripple is also shown in the waveform.

6. CONCLUSION

The proposed method uses half-bridge switch modules which is more compact and has higher utilization of power switches and lower cost, without degrading in performance. By employing this bridgeless SEPIC converter, the ripples can be greatly reduced with improved performance. A comparison between the proposed topology and the conventional SEPIC converter shows that the component current ripples are much lower in the presented topology. In low-voltage high-current applications, the proposed topology can be more beneficial than a conventional SEPIC converter. Thus, the simulation and its outputs have shown that, the output has a tendency of improved performance with reduced torque ripples throughout its operation. The theoretical analysis and simulation results were provided.

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