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Control of Indirect Matrix Converter by Using Improved SVM Method

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ABSTRACT

A novel space vector modulation (SVM) method for an indirect matrix converter (IMC) is used to reduce the common -mode voltage (CMV) in the output. The process of selecting required active vectors and to describe the switching sequence in the inverter stage of the IMC is explained in this paper. This novel SVM method used to decrease the peak -to-peak amplitude voltage of CMV without using any external hardware. The other advantage of this SVM method is to reduce the total harmonic distortion of line-to-line output voltage. This new modulation technique is easily implemented through simulation and its results are used to demonstrate the improved performance of the input/output waveforms.

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1. INTRODUCTION

Matrix converters (MCs) produce ac outputs with variable magnitudes and frequencies from an ac power supply. These matrix converters have received significant consideration since they provide fairly sinusoidal input/output waveforms as well as bidirectional power flow. In addition, the MCs have better reliability and a compact design due to the absence of large electrolytic capacitor at intermediary energy storage. These topologies of MCs are classified into two types: the conventional or direct matrix converter (DMC) and the indirect matrix converter (IMC) [1-5].

This topology of IMC is a group of power switches which is analogous to the conventional rectifier/dc-link/inverter topology. The power circuit of IMC consists of a rectifier stage and a inverter stage. A six bidirectional switches are used for the rectifier stage and the inverter stage has six unidirectional switches as shown in Figure 1. By using IMC one can generate same input and output wave forms similar to DMC [6].

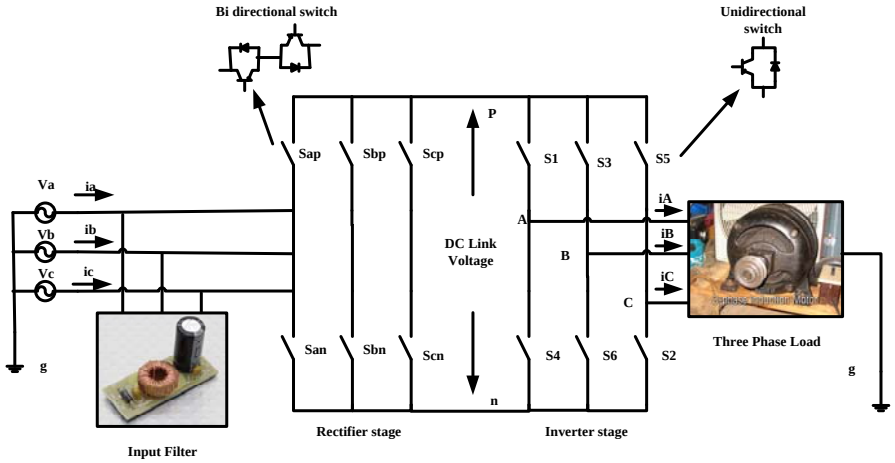

Figure 1. A Topology of an Indirect Matrix Converter

In addition, this IMC topology has the advantages as follows [7].

1) A simple commutation and clamp circuit for overvoltage protection is provided.
2) There is a possibility of reduction of power switches in the rectifier stage.
3) There is a possibility of modified topology according to a given application, for example, to improve the quality of the output, to supply a three-phase unbalanced load, to drive various three-phase loads and to increase the voltage transfer ratio more than 0.866.

In power converters, common-mode voltages (CMV) due to the high-speed pulse width modulation (PWM) introduce many problems inside an electrical system. The CMV causes the following: Winding failure of motor, deterioration of bearing and electromagnetic interference. Hence, the reduction of CMV within the power converter is important.

This paper proposes a new SVM method to decrease the CMV, to improve the quality of output voltage and also to reduce the number of switching states in the inverter stage. The method which is proposed is based on the three active vectors instead of four, which is used in the standard SVM method. The effect of the standard SVM method on the output performance and a comparative evaluation of the THD are discussed in order to identify the effectiveness of the new SVM method.

2. NEW SVM METHOD

The new SVM method uses a group of three neighbor active vectors to synthesize the reference output voltage vector. The maximum value of CMV is reduced to 42% only by applying the active vectors in the inverter stage for generating the reference output voltage vector. To overcome the limitations of the standard SVM method, such as, line-to-line output voltage having high ripple and the inverter stage having high switching loss at the inverter stage, a PWM technique is applied at the inverter stage [1]. This technique uses a group of three neighbour active vectors to generate a reference output voltage vector. In the new SVM method the inverter stage sectors are defined differently as compared with the standard SVM method. These sectors are defined by using three nearest active vectors in order to generate the reference output voltage vector. The space vector division into six sectors and the group of three selected active vectors in each sector are shown in Figure 2.

The proposed SVM method can be illustrated by assuming the desired output voltage and the input current space vectors to be located in sector 1($-\pi/6 \leq \alpha_o \leq \pi/6$, $-\pi/6 \leq \alpha_i \leq \pi/6$)[2] .

The combination of the two active vectors I_{ab} and I_{ac} are used to generate the reference input current vector in the rectifier stage which is similar to that of the standard SVM method. Three active vectors V_6, V_1 and V_2 are used in the inverter stage to generate the reference voltage vector (refer to Figure 1).

The switching sequence of three vectors in sector I is 101-100-110-110-100-101 and the switching sequence in sector II is 110-010-100-100-010-110 are assumed. When the reference output voltage vector changes from sector I to sector II, during the given time, the switching state is changed from 101 to 110. The selection of the switching sequence of the active vector in all six vectors is properly selected as shown in Table 1.

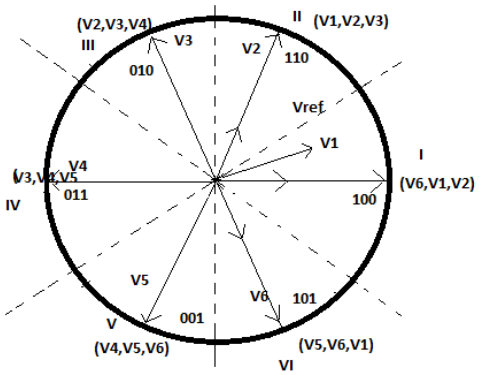

Figure 2. The Reference Output Voltage Vector Generation at the Inverter Stage by Using New SVM Method

Table 1. Inverter stage switching sequence

Output sector	Switching sequence
1	101-100-110-110-100-101
2	110-010-011-011-010-110
3	100-110-010-010-110-100
4	010-011-001-001-011-010
5	011-001-101-101-001-011
6	001-101-100-100-101-001

The Switching losses are greatly affected by the number of switching commutations. Figure 3 and Figure 4 show the different switching patterns of the standard SVM method and new svm method [4].

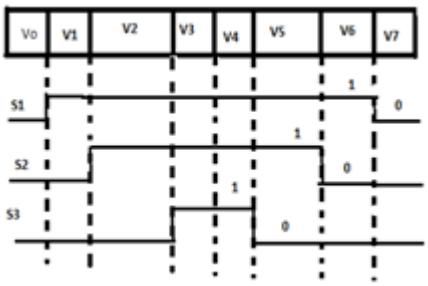

Figure 3. Switching pattern of the inverter stage with the Standard SVM method

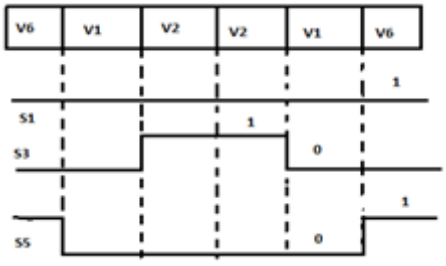

Figure 4. Switching pattern of the new SVM method

From the switching pattern it is easily observed this for the new SVM method each power switch does not change its state during two to six sectors in the inverter stage. We can see that the switch has no switching commutations during sectors 1 and 4. Hence, the new SVM method is used to reduce the number

of switching commutations. Therefore, by using new SVM method the power switching losses can be reduced in the inverter stage.

The synchronization between the switching state of the rectifier and the inverter stages of the new SVM method are shown in Figure 5.

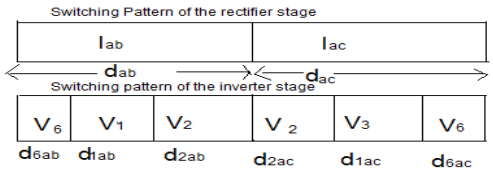

Figure 5. The new SVM method switching pattern

In the inverter stage, the group of three active vectors V_6, V_1 and V_2 are used to generate the reference output voltage vector by applying duty cycles d_6, d_1, and d_2, respectively. Therefore, the reference output voltage can be generated as:

$$V_{ref} = d_6V_6+d_1V_1+d_2V_2$$

The switching patterns of the inverter stage are divided into two groups similar to that of the standard SVM method. In the inverter stage, voltage vectors are arranged in a double-side switching sequence:

V_6-V_1-V_2-V_2-V_1-V_6. In the rectifier stage, active current vector I_{ab} is applied and the first side switching sequence V_6-V_1-V_2 is applied in the inverter stage. The duty cycles for the three active vectors V_6, V_1 and V_2 are calculated by multiplying d_1, d_2 and d_6 with d_{ab}, as shown below:

$$d_{1ab}=d_1.d_{ab};\ d_{2ab}=d_2.d_{ab};\ d_{6ab}=d_6.d_{ab}$$

During the active vector, I_{ac} which is applied to the rectifier stage and the second side switching sequence V_2-V_1-V_6 is given in the inverter stage.

From the Table 2, it is observed that the value of CMV depends on the value of the input voltage and the switching states of the rectifier and inverter stages. The peak CMV is not affected by the desired output frequency and voltage. The peak value of CMV for the new SVM method is $1/\sqrt{3}$ the input phase voltage magnitude which is shown in the Figure 6.

Table 2. Peak value of CMV

The peak CMV		Input current vector	
		1,3,5	2,4,6
Output Voltage Vector	V_0	$\sqrt{3}/2V_i$	$-V_i$
	V_7	V_i	$-\sqrt{3}/2\ V_i$
	V_1,V_2,V_3,V_4,V_5,V_6	$1/\sqrt{3}\ V_i$	$-1/\sqrt{3}\ V_i$

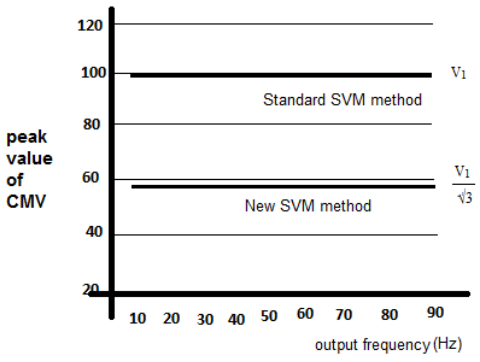

Figure 6. Comparison of peak value of CMV for standard SVM and New SVM method

3. RESULTS AND ANALYSIS

The performance of the new SVM method is evaluated by using the total harmonic distortion (THD) for the line-to-line output voltage. The THD of the line-to-line output voltage, which contains both fundamental and harmonic components, is defined as:

$$THD=\frac{\sqrt{Vrms^2-V1^2}}{V1}$$

Where V_1 is the fundamental component and V_{rms} is the root mean square of the line-to-line output voltage.

The new SVM method is shown to generate a small harmonic component, according to the fast Fourier transform (FFT) of the CMV as compared with the standard SVM method which is shown in the following simulation results in Figure 7.

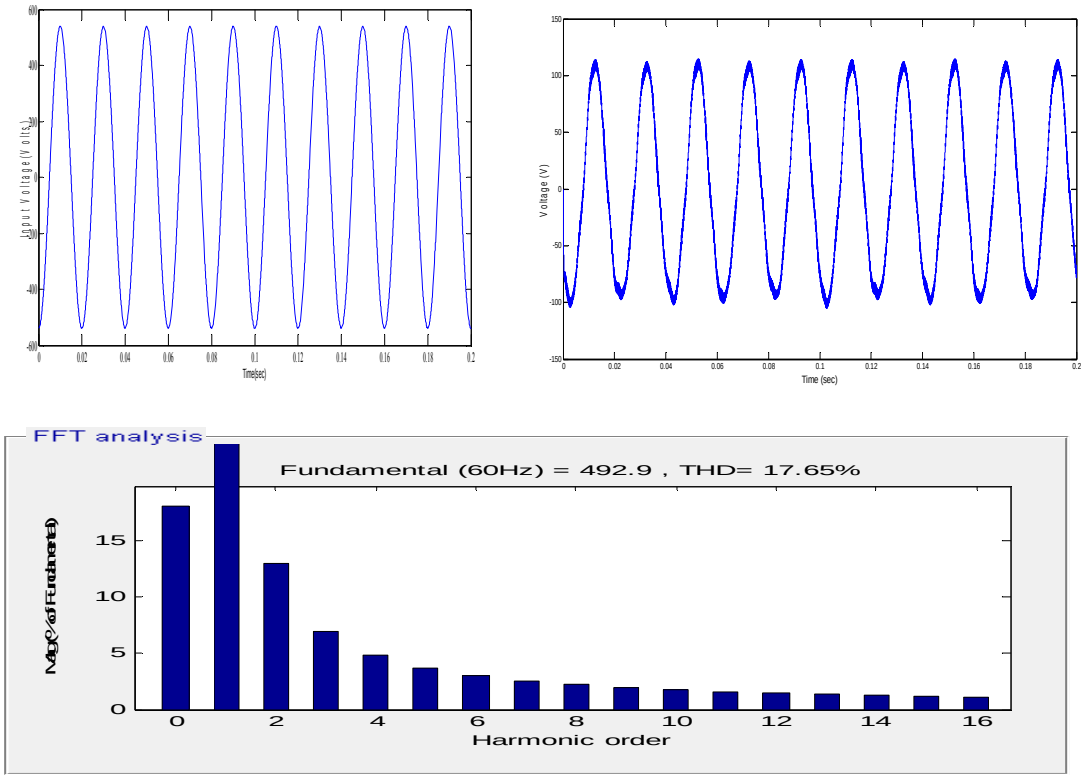

Figure **7.** Waveform of Input voltage, CMV and its FFT at f=50Hz by using new SVM method

4. CONCLUSION

The reduction of CMV by using the new SVM method for IMC is proposed in this paper. In addition, this method is also used to decrease the total harmonic distortion in order to control the IMC over the full output voltage range [2] [3]. Simulation results are provided to demonstrate the effectiveness of the proposed method.

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