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Soft Switched Multi-Output Flyback Converter with Voltage Doubler

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ABSTRACT

A novel multi-output voltage doubler circuit with resonant switching technique is proposed in this paper. The resonant topology in the primary side of the flyback transformer switches the device either at zero voltage or current thus optimizing the switching devices by mitigating the losses. The voltage doubler circuit introduced in the load side increases the voltage by twice the value thereby increasing the load power and density. The proposed Multi-output Isolated Converter removes the need for mutiple SMPS units for a particular application. This reduces the size and weight of the converters considerably leading to a greater payload. This paper aims at optimizing the proposed converter with some design changes. The results obtained from the hardware prototype are given in a comprehensive manner for a 3.5W converter operating at output voltages of 5V and 3.3V at 50 kHz switching frequency. The converter output is regulated with the PI controller designed with SG3523 IC. The effects of load and line regulation for ±20% variations are analyzed in detail.

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1. INTRODUCTION

Flyback converters are best suited for low power applications, as reported in literatures. Many Flyback conveters topologies implementation [17, 18] have been discussed in the area of resonance and its importance in high switching frequency applications [12, 13]. Resonance (ZVS/ZCS) introduced in these converters solve the issue of reducing switching losses during ON and OFF conditions. Hence nowadays, Resonance Topologies [1] are preferred to PWM converters [2-3]. Literatures have reported that the RCD snubber circuits [4, 15] were used to dissipate leakage inductance energy, which in turn introduces a drawback when leakage inductance [5, 6] value is high. On the other hand, resonant circuits engulf the effect of leakage inductance, switch capacitance and parasitic capacitance; in essence, removing the necessity for an extra inductor and capacitor for resonance. This paper emphasises on the load power, density and efficiency of the multioutput converters. The multi-output [9, 10] and voltage doubler [8, 11, 14, 16] concepts increase the number of outputs in the converter and hence the power density. The switching losses due to the devices used in the converter are reduced to zero with ZVS/ZCS during ON/OFF [7].

To the author's knowledge, previous works reported in literature concentrate on reducing switching losses in the primary circuit by introducing resonance in the primary switches; while in secondary diodes, the switching losses are not considered for single/multi-output converter. This work focuses on multi-output topology and voltage doubler in the secondary circuit. As there are no major changes in the energy storage elements except for the addition of a tertiary winding in the flyback transformer, more than one output can be obtained from the same sized converter and the latter increases the output voltage. Moreover, it has the added advantage of reducing the switching stress in secondary diodes. Lastly, implementation of closed loop circuit regulates the output voltage by using a low cost IC (SG3525) resulting in compactness, economical usage, simple control methodology and regulated SMPS.

2. PROPOSED CONVERTER

The power stage circuit diagram of the multi-output ZVS-PWM flyback DC-DC converter with voltage doubler is presented in Figure 1. The converter consisting of a switch S_m, an isolated transformer, transformer magnetising inductor L_m, transformer leakage inductor L_s, output filter capacitors C_{o1} and C_{o2}, diodes D_2 and D_3, resonant inductor L_r, resonant capacitor C_r, auxiliary switch S_a , secondary resonant capacitors C_{d1} and C_{d2} and rectifier diodes pairs D_{11}, D_{12} , and D_{21}, D_{22} [7]. The voltage doubler circuit has the advantage of increased power density in the converter over its counterpart - the multi-output ZVS-PWM, thus facilitating reduced converter size. Multi-output converters are equivalent to many single output converters connected in parallel to each other; hence the operation is similar to the single output converters as explained by authors in [14].

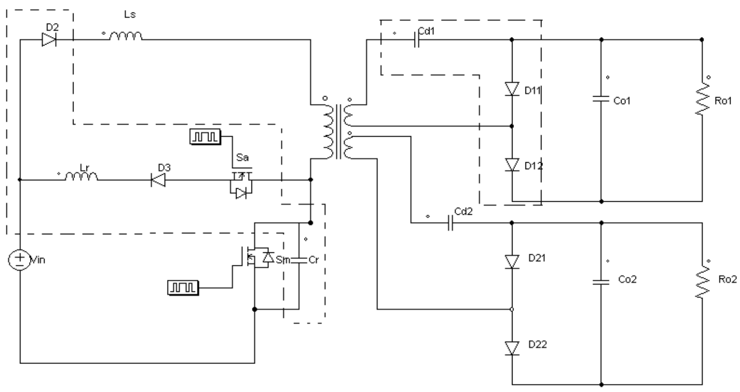


Figure 1. Circuit diagram

3. DESIGN DETAILS

Isolated flyback converters are a derivative of non-isolated buck-boost converters. The voltage input-output relation is given as:

$$V_0 = \frac{V_{in}}{n}\left(\frac{D}{1-D}\right) \quad (1)$$

Where, n >1 for the proposed converter and D is the duty ratio (< 1); implying that V_0 is always less than V_{in}. As the voltage doubler is introduced in the secondary side, it has no effect on the primary voltage but acts only to increase the voltage on the load side.The characteristics of the proposed converter are tabulated in Table 1. The design calculations are done using equations (2)-(6) and the obtained values are listed in Table 1.

Table 1. Converter specification and designed values

Specifications	Designed values		
Input voltage, V_{in} : 12 ± 10%V	Magnetising inductance, L_m : 81μH		
Output voltage, V_{o1} : -3.3V	No.of turns in primary, N_p : 36		
Output current, I_{o1} : -0.33A	No.of turns in first secondary, N_{s1} : 19		
Output voltage, V_{o2} : -5V	No.of turns in second secondary, N_{s2} : 12		
Output current, I_{o2} : -0.5A	Transformer Core selected : EE/20/10/15		
Switching frequency, f_s : 50kHz	L_r = 25μH	C_r = 27.77nF	L_s = 50 μH
Power rating, P_o : 3.5W	C_{d1} = 300nF	C_{d2} = 1000nF	f_r = 250kHz

For achieving ZVS criteria $$\frac{f_s}{f_r} = 0.2 \quad (2)$$

Characteristic impedance, $$Z_o > \sqrt{\frac{L_r}{C_r}} \quad (3)$$

Resonant frequency, $$\omega_r = \sqrt{\frac{1}{L_r C_r}} \quad (4)$$

The transformer design [5, 6] is carried out and the details are tabulated in table 1.

Output filter capacitance, $$C_{o1} = C_{o2} = \frac{I_{o1} * T_{on}}{V_{r1}} = 100\mu F \quad (5)$$

The secondary resonant capacitor C_d [8, 11] and the rectifier diodes D_{11} and D_{12} double the output voltage.

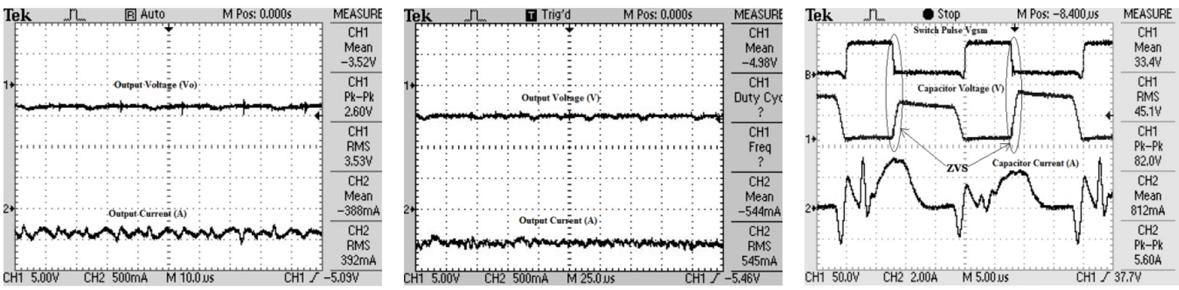
Output resonant capacitor, $$C_d \geq \frac{4(\pi n_s D T_s)^2}{L_s} \quad (6)$$

4. RESULTS AND ANALYSIS

The hardware results obtained are presented and analysed in this section.

4.1. Hardware Implementation

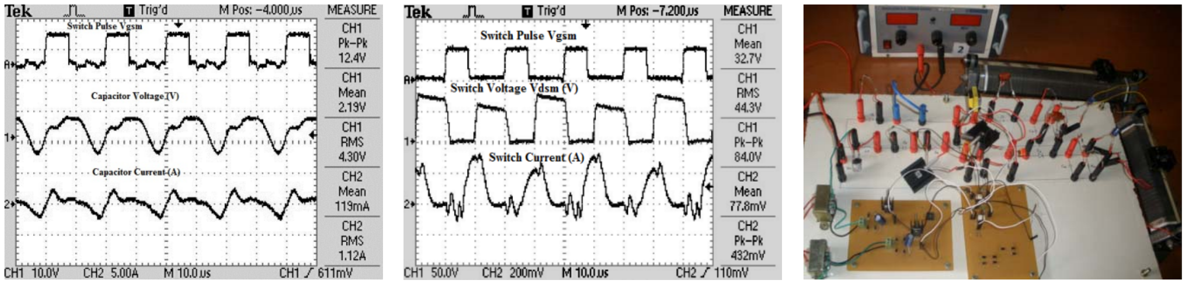
The hardware laboratory prototype was developed for Multi-output voltage doubler ZVS flyback converter with the designed values (listed in Table 1). IRF840 was used as power switches and IN5819 as diodes. The gating pulses for the switches S_a and S_m were generated using ARM processor with pulse width of 40% and 20% respectively. Figure 2(a) and (b) depict the output voltage and current values (-3.3V, -0.33A and -5V, -0.5A) for the converter. The resonant capacitor voltage V_{cr} and I_{cr} obtained is shown in Figure 2(c).



(a) (b) (c)

Figure 2 Load and Resonant. (a) Load-1 voltage and current (b) Load-2 voltage and current (c) Resonant capacitor voltage and current with main pulse

From the figure it can be seen that that the main switch is turned ON/OFF when the resonant capacitor voltage becomes zero (i.e) at ZVS and 82V is the peak voltage across the resonant capacitor. And when the resonant current decreases to zero (ZCS), the auxiliary switch is also turned OFF. The voltage and current for output resonant capacitor with main switch pulse are shown in Figure 3(a). The peak switch voltage of 84V obtained and the hardware prototype are presented in Figure 3(b) & (c) respectively. It is also observed from the open loop results that when the load is increased, output voltage tends to increase, and a similar state is observed during supply voltage increase which is not preferred mostly by load applications. Hence a closed loop operation is necessary.



(a) (b) (c)

Figure 3. (a) Secondary resonant capacitor voltage and current with main switch pulse (b) Main switch voltage (V_{dsm}) and current (I_{dm}) with main switch pulse (V_{gsm}) (c) Experimental setup

4.2. Closed Loop Employment

The closed loop hardware execution of the converter is completed with SG3525 IC as shown in Figure 4. The second output voltage is controlled with the analog controller IC SG3525, which is a 16 pin IC commonly used for PWM generation. The feedback voltage is fed to the inverting pin (1st pin) of the IC and the reference voltage is fed to the non-inverting pin (2nd pin) from the 16th pin. The PI controller output at the 9th pin and the sawtooth waveform generated in the same IC are compared. PWM generator is used for generating the pulses from 11th and 14th pin. The pulse generated from 11th pin is used to trigger the main switch S_m. The behavior of the converter with closed loop circuit is studied in detail for load and line transients as explained below.

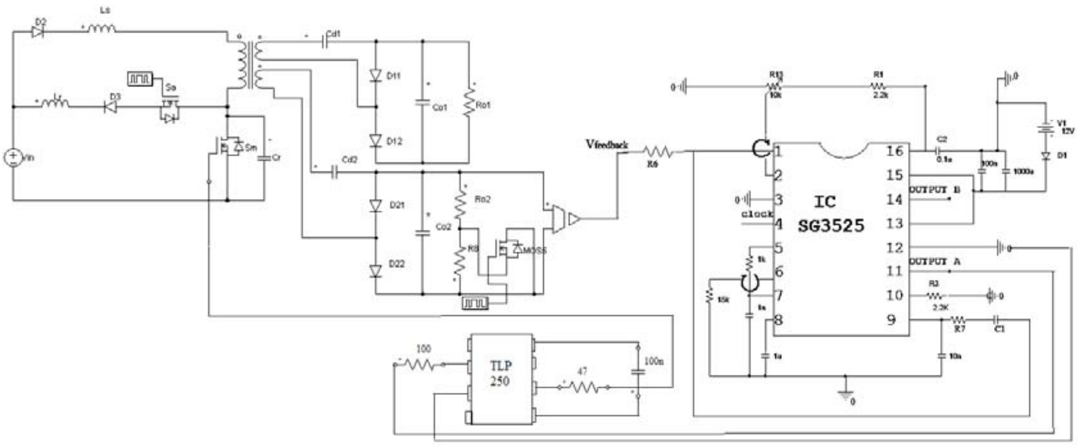


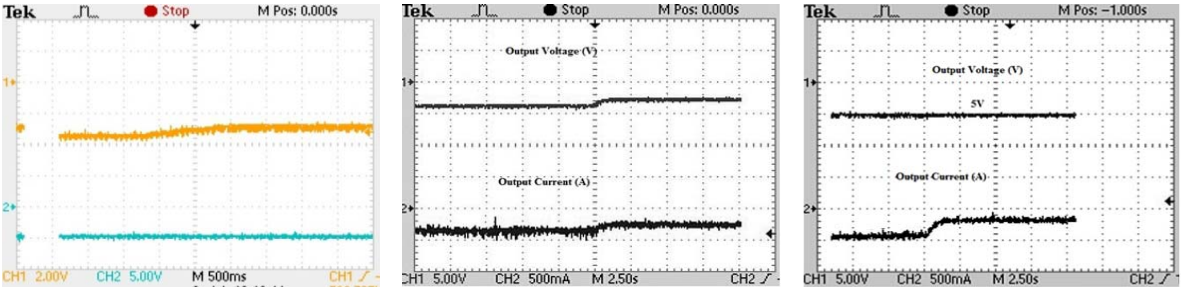
Figure 4. Closed loop employment

4.2.1 Load Transients

For a fall in load-1, the effect on output voltages is shown in Figure 5(a). Further it also reiterates that the load voltage-2 is regulated at 5V for the load variation of -20%. Similar results are obtained for increase in load also. The effect on output-1 and 2 for rise in load-2 can be seen in Figure 5(b) and (c). Load voltage-1 is diminished to 2V while load voltage-2 is regulated at 5V for +20% variations in load-2.

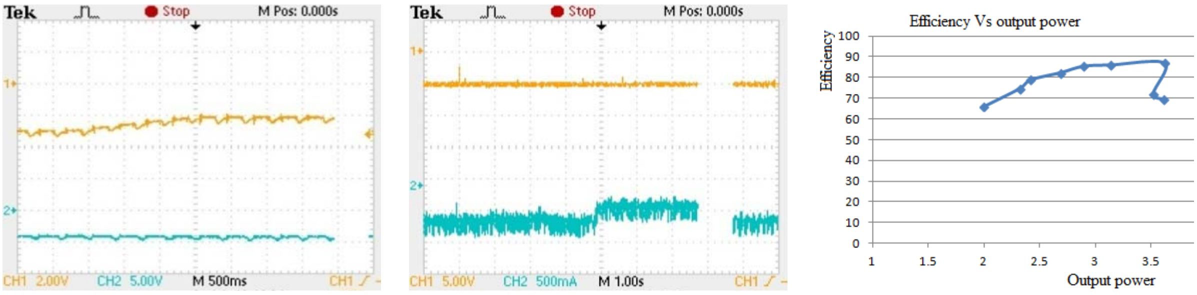
4.2.2 Line Transients

A variation of ±20% is applied for line voltage and the effect on load voltage-1 and 2 for fall in supply voltage is presented in Figure 6(a). It is witnessed that the output voltage-1 decreases to 2V from rated 3.3V for decrease in supply. Figure 6(b) confirms the effect of load-2 voltage and current for fall in supply voltage. The load voltage-2 is detected to be regulated for both upswing and decline in supply voltage. The supply change applied is apparent in the change in current.



(a) (b) (c)

Figure 5. (a) Load voltages when R_{o1} decline (b) V_{o1}, I_{o1} for load variations in R_{o2} (c) V_{o2}, I_{o2} for load variations in R_{o2}



(a) (b) (c)

Figure 6. (a) Load voltages for decrease in supply voltage (b) Regulated load voltage and current (V_{o2}, I_{o2}) for line voltage reductions (c) Efficiency curve

5. ANALYSIS OF THE CONVERTER

From these evaluations we determine that the output voltage-2 is regulated for ±20% variation in both line and load variation. Efficiency of the converter is calculated from Equations (7 -9).

Output power, $$P_{out} = \frac{V_0^2}{R_0} \tag{7}$$

Input power, $$P_{in} = V_{in} I_{in(rms)} \tag{8}$$

Efficiency, $$\eta = \frac{P_{out}}{P_{in}} \tag{9}$$

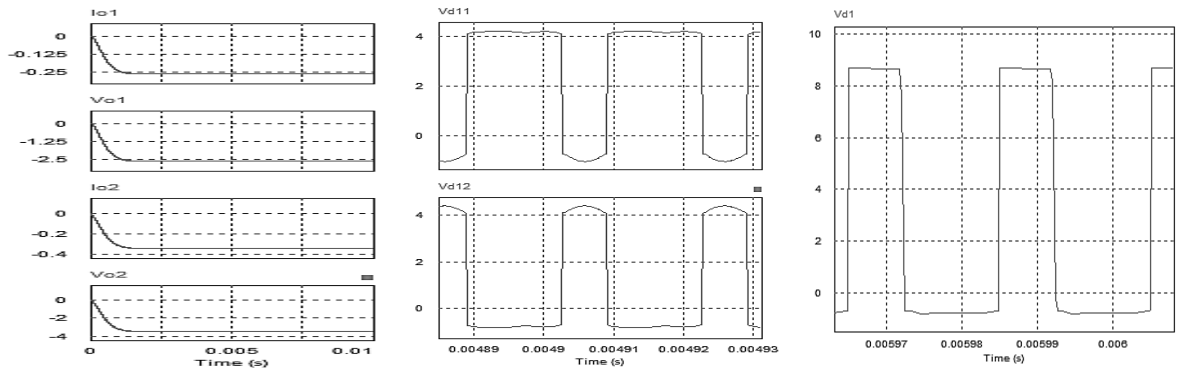
The multi-output voltage doubler ZVS flyback converter gives an efficiency of 88%, which is significantly higher than that of the multi-output ZVS flyback converter as revealed in efficiency curve Figure 6(c). A comparison of the efficiencies of single output and multi-output ZVS flyback converter with and without voltage doubler is illustrated in Table 2. From the table it is can be seen that multi-output ZVS topology with voltage doubler is more efficient than the other topologies.

Table 2. Efficiency appraisal

	PWM based Flyback	ZVS Flyback	ZVS Flyback with VD
Single-Output	40%	75%	85%
Multi-Output	72%	80%	88%

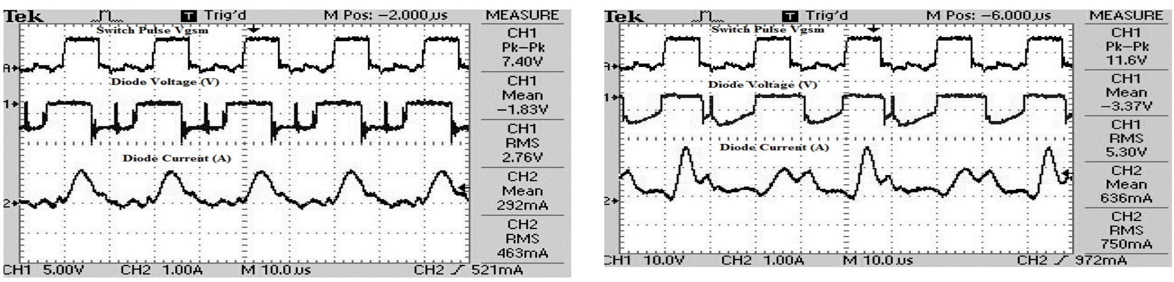
The proposed circuit implemented without voltage doubler circuit (C_{d1}, D_{11} and C_{d2}, D_{21} are removed) resulted in outputs -2.6V, -0.26A and -3.4V, -0.34A, as shown in Figure 7(a). From this waveform it is clear that the secondary output voltage and currents respectively are doubled due to the introduction of a voltage doubler circuit in the load side of the flyback transformer.

Power density is measured as power per unit volume. Adding a capacitor and a diode at the secondary side has an insignificant effect on volume. Without a voltage doubler, the power obtained is 1.832W, while with the voltage doubler the power is 3.589W. Taken as a ratio, we observe that the power density is doubled. Similarly, multi-output ZVS flyback converter exhibits double the voltage stress on the secondary diodes than the proposed converter, as verified in simulation (Figure 7 (b) & (c)) and hardware results (Figure 8(a) & (b)). The voltage RMS across the device is 5.3V compared to just 2.8V in the proposed converter. Thus it is vibrant that the voltage stress on the secondary diode is double that of the proposed converter.



(a) (b) (c)

Figure 7. (a) Output voltages and currents without voltage doubler circuit; Voltage across the secondary diodes in simulation for (b) multi-output voltage doubler ZVS flyback converter (c) multi-output ZVS flyback converter



(a) (b)

Figure 8. Voltage across the secondary diodes (a) with voltage doubler (b) without voltage doubler

This research paper proposes that - for applications of power supplied to diverse subsystems such as drives, tuners, audio stages and complex processor and logic circuits; multiple output flyback converters with voltage/current [19] ranges of 5V/0.5A, 3.3V/0.33A, etc are vital. Typical application is also noted in set top boxes, decoders and small DVD players [19].

6. CONCLUSION

Analysis of the Multi-output voltage doubler ZVS flyback DC-DC converter concludes that the auxiliary switch S_a operates at ZCS during turn ON and turn OFF, and all other semi conductor devices operate at ZVS during turn ON and turn OFF. This is achieved without any current/voltage spike that persists in conventional hard switching circuit. Thus, ZVS flyback converters have reduced switching losses when compared to conventional flyback converters. This significantly improves the performance and efficiency of the circuit. It is also prominent that by coupling the multi-output ZVS flyback converter with a voltage doubler, the power density of the converter can be increased. Also, given that the switching losses in the active and passive devices are negliglble the efficiency is more than doubled, when compared to hard switched converters. Simulation was carried out for rated 3.5W output power and the results obtained are analyzed. The hardware prototype was modeled for the same power rating and the results obtained are similar to those obtained in simulations. Thus a multi-output voltage doubler topology occupies the same space as that of the multi-output flyback converters and has better efficiency also. The output of the converter is regulated for line and load transients with the PI controller designed with a simple and low cost laboratory purpose IC SG3525.

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