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The Operating Improvement of the Supply Source and the Optimization of PWM Control

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ABSTRACT

In this paper the operating improvement of the supply source and the optimization of PWM control are proposed. A comparison (based on the better operating in terms of input voltage) between the multilevel inverters (NPC multilevel inverter and H bridge inverter) is studied. Then two control strategies (the SPWM and the suboptimal PWM) are applied to the multilevel inverter which has the better voltage performance. At last a comparison between these two control techniques based on two essential points, the THD and the output voltage value. A comparison between our results and results taken from literature is also presented in this paper. Simulations are carried out using PSIM environment.

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1. INTRODUCTION

The increasing use in industry of static devices to convert energy, called static converters, brings out more and more disturbance problems at the main electrical grid level. Thus there is today an increase in the voltage THD. To resolve this problem, multilevel inverter structures were developed.

Initially, created both to put several switches in series and to accurately ensure the voltage withstand across them. Thereafter these converters have shown interesting properties on the output waveforms [1]. The output of multilevel inverter is a staircase wave, which is nearly sinusoidal [2].

The multilevel inverters still require many improvements and optimization in the control area. Among these, the Diode clamped, and the cascaded H-bridge inverter are the two main different multilevel inverter structures which are used in industrial applications with separate dc sources. In diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter [3], [4], [5]. Among the control strategies, we distinguish four PWM structures; the SPWM, the SVPWM [6], the SHEWPM [7] and the suboptimal modulation. This work is dedicated to the performance improvements of inverter voltage and the optimization of PWM control strategies.

2. MULTILEVEL INVERTER

2.1. Neutral Point Clamped Inverter

The NPC converter is one of the reference structures in the multilevel conversion (see Figure 1). This converter uses the series connection of switches. The voltage distribution across the switches is carried out by diodes connected at middle point.

The voltage across the capacitors are all equal to $E/(N-1)$, E is the overall direct voltage.

The number of levels is computed by the following formula [8]:

$$N = P + 1 \quad (1)$$

N: Number of voltage levels

P: Number of complementary switch pairs per phase.

Figure. 1 shows an NPC three level inverter.

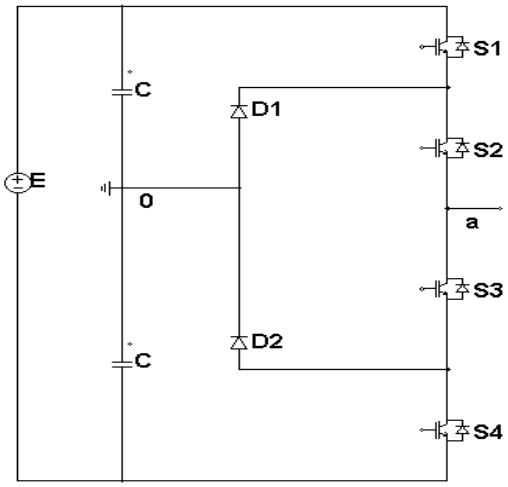


Figure 1. Three level neutral diode-clamped legs

Table 1 shows the relationship between the allowed switch configurations and the output voltages of a three level diode-clamped leg:

Table 1. Three level neutral diode-clamped leg relationships between switch configurations and output voltages

Switch state				
K1	K2	K3	K4	Vao(V)
1	1	0	0	E/2
0	1	1	0	0
0	0	1	1	-E/2

2.2. H Bridge Inverter

This conversion structure family is the first one described in literature as a multilevel conversion structure. The principle of this topology is to put in series several single phase two level bridges in H. Each inverter is fed by a direct source E, and composed of four switches which are unidirectional in voltage and bi-directional in current. It is an association between an IGBT and a diode connected in anti-parallel [9], [10].

These bridges are connected to separate voltage sources. The number of sources is equal to the number of bridges.

$$N = 2D + 1 \quad (2)$$

N: Number of voltage levels
D: Number of single phase bridges per phase

The structure of a multilevel inverter based on the series connection of H bridges (single phase inverter or partial cell) is shown in Figure 2.

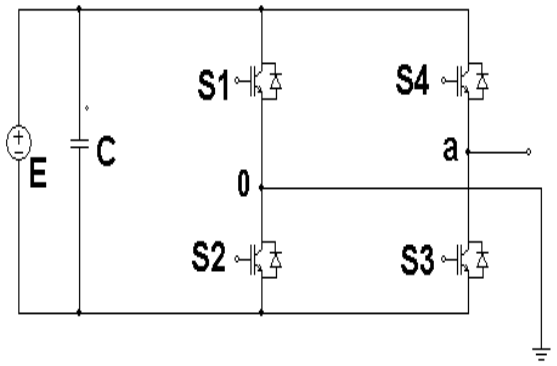


Figure 2. Three level cascaded H-bridge leg

Table 2 shows the relationship between the allowed switch configurations and the output voltages of a three level cascaded leg inverter.

Table 2. Three level cascaded H-bridge leg relationships between switch configurations and output voltages

Switch state				
K1	K2	K3	K4	Vao(V)
1	0	1	0	E
1	1	0	0	0
0	1	0	1	-E

Considering the same DC source voltage, it can be seen that even cascaded inverter output voltage amplitudes are greater here than in the diode-clamped.

3. SIMULATION RESULTS

In order to compare between the two topologies (NPC and H bridge), simulations are carried out to confirm the veracity of Tables 1 and 2 concerning the relationship between the allowed switch configuration and the output voltage.

The SPWM control is used with the same simulation parameters. PSIM program is used as simulation environment. Simulation parameters are grouped in Table 3.

Table 3. Simulation parameters for SPWM control

E (V)	F_p (Hz)	F_m (Hz)	A_p	A_m
220	20k	50	1	1

E: Direct voltage feeding the inverter
F_p: Carrier frequency
F_m: Modulating frequency
A_p: Carrier amplitude
A_m: Modulating amplitude

3.1. Simulation Example of Three Level NPC

Simulation Example of Three Level NPC is shown in Figure 3.

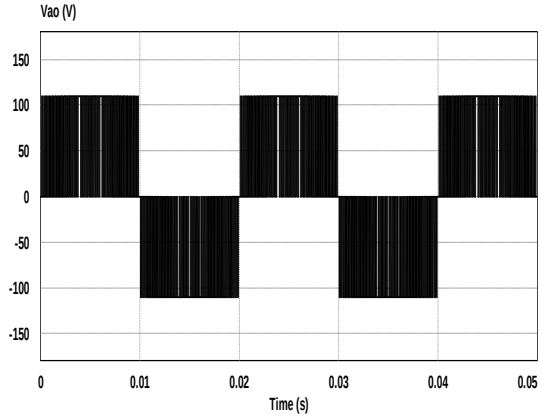


Figure 3. Vao voltage waveform for three level NPC (THD=56,39 %; Vmax=110V)

3.2. Simulation Example of Three Level H Bridge

Simulation Example of Three Level H Bridge is shown in Figure 4.

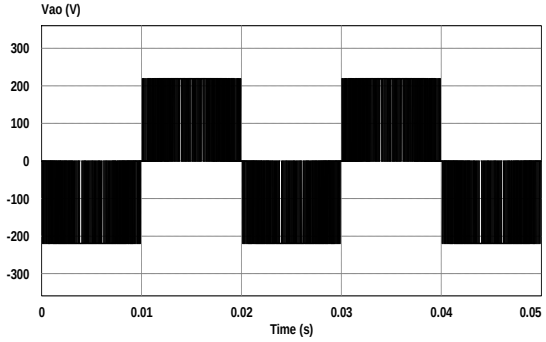


Figure 4. Vao voltage waveform for three level H bridge (THD=56,39 %; Vmax =220V)

4. ANALYSIS OF RESULTS

The obtained simulation results show that the Vao voltage value for three level NPC is equal to: $V_{ao1} = 110\ (V)$; and Vao voltage value for three level H bridge is equal to: $V_{ao2} = 220\ (V)$, for the same direct source voltage $E = 220\ (V)$.

Thus:

$$V_{ao1} = \frac{E}{2} \tag{3}$$

$$V_{ao2} = E \tag{4}$$

Relying on the obtained simulation results, we notice that the H bridge inverter exploits at most the direct supply, on the other hand the NPC inverter exploits only the half of the direct supply, causing the decommissioning of power of the supply.

The control strategies (SPWM and suboptimal PWM) are applied to the chosen multilevel inverter (H bridge multilevel inverter) according to the obtained results.

5. MODULATION TECHNIQUES

5.1. SPWM strategy

This strategy is based on the comparison of a sine wave reference voltage *Um* called modulating signal which has an amplitude *Am* and a frequency fm, to one or more triangle carriers Up which have the same amplitude $A_p = 2/(N-1)$ and the same frequency *fp*.

Each comparison gives 0 if the modulating signal is higher than the carrier. Otherwise it gives 1. The sum of signals obtained from the comparisons gives the phase voltage value of each level.
Two parameters typify this strategy [11]:

Modulation index: $Q = f_p / f$ (5)

Voltage adjustment coefficient: $r = A_m/((N-1)A_p$ (6)

The Figure 5 shows the necessary signals to generate a five level voltage, with *Q=30* and *r= 1*.

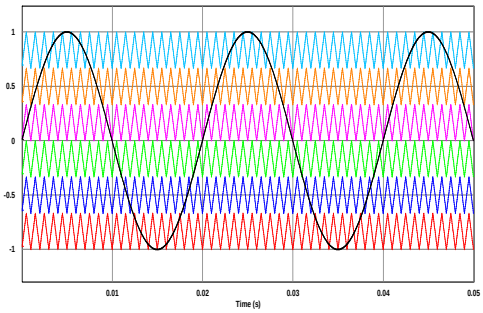


Figure 5. Reference voltage and triangle carriers for a five multilevel inverter (*Q=20, r = 1*)

5.2. The Suboptimal PWM Strategy

Optimal or suboptimal PWM enables to reduce voltage waste by injection of harmonic order 3 in the reference (modulating signal) [12].

The injection of harmonic order 3 at modulating signal level enables to increase the fundamental maximum amplitude of the resulting wave, and consequently in the output voltages without the modulating amplitude goes beyond Ap/2. This harmonic order 3 contained in the output voltage of the inverter is eliminated by the three-phase system in single and phase voltages [13]. This method is illustrated by Figure 6.

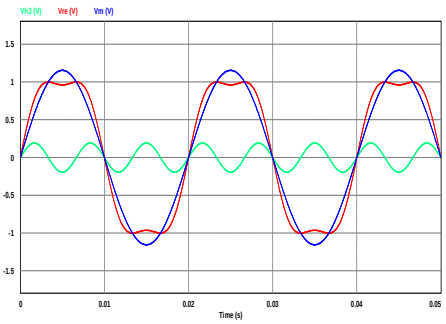


Figure 6. Voltage waveforms: waveform of the resulting voltage *Vre* (red); waveform of the modulating voltage *Vm* (blue); waveform of the third harmonic voltage *Vh3* (green)

The modulating is expressed as follows:

$$V_{re} = V_m + V_{h3} \quad (7)$$

$$V_{re} = A_m \sin(\theta) + A_{h3} \sin(3\theta) \quad (8)$$

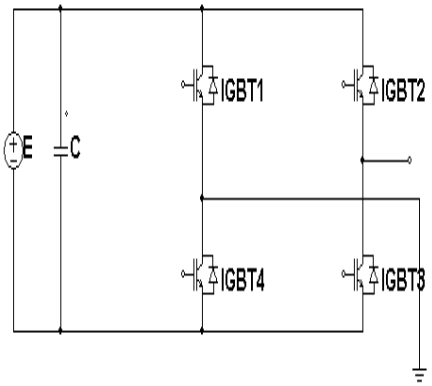
$$A_{h3} = A_m / 6 \quad (9)$$

Vre: Resulting voltage waveform
Am: Modulating amplitude
Ah3: Harmonic order 3 amplitude

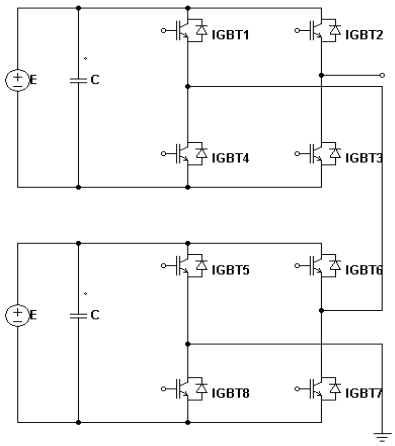
The H bridge 3, 5, 7 and 15 level inverters are implemented in PSIM environment in order to define which of the two control strategies (SPWM and PWM) is the most efficient.

The phase voltage waveform Vab (V) with a fundamental frequency of 50 Hz and a switching frequency of 20 kHz is presented for all simulations.

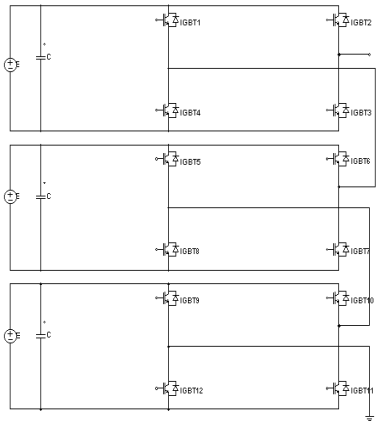
For the comparison, the THD and the fundamental voltage are measured and presented for all simulations. Figure 7 represents H bridge 3, 5, 7 and 15 level inverter one-leg.



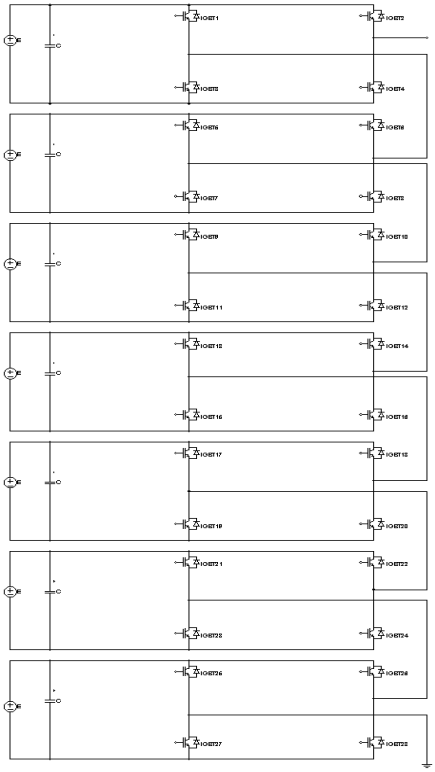
(a)



(b)



(c)



(d)

Figure 7. (a) 3-level cascaded H-bridge leg, (b) 5-level cascaded H-bridge leg (c) 7-level cascaded H-bridge leg (d) 15-level cascaded H-bridge leg.

6. SIMULATION RESULTS

6.1. SPWM Simulations

Simulation parameters of SPWM control are grouped in Table 4.

Table 4. Simulation parameters for SPWM control.

E (V)	Fp (Hz)	Fm (Hz)	Ap	Am
110	20k	50	1	1

6.1.1. Simulation Results of H bridge 3 Level Inverter: Aspect of Phase Voltages Vab(V)

Simulation Example of H bridge 3 Level Inverter: Aspect of Phase Voltages Vab(V) in Figure 8.

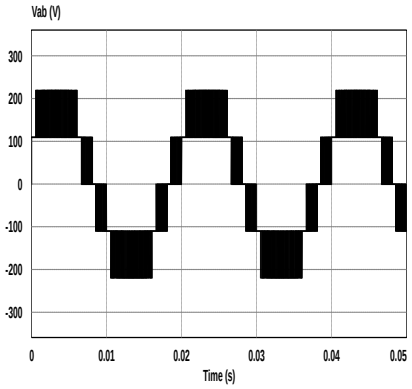


Figure 8. Phase voltage waveform *Vab(V)*for H bridge 3 levels

6.1.2. Simulation Results of H Bridge 5 Level Inverter: Aspect of Phase Voltages Vab (V)

Simulation Example of H bridge 5 Level Inverter: Aspect of Phase Voltages Vab(V) in Figure 9.

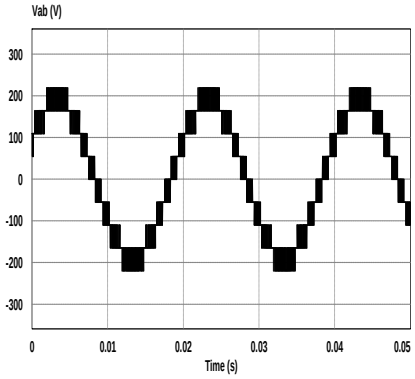


Figure 9. Phase voltage waveform *Vab(V)* for H bridge 5 levels

6.1.3. Simulation Results of H Bridge 7 Level Inverter: Aspect of phAse Voltages Vab (V)

Simulation Example of H bridge 7 Level Inverter: Aspect of Phase Voltages Vab(V) in Figure 10.

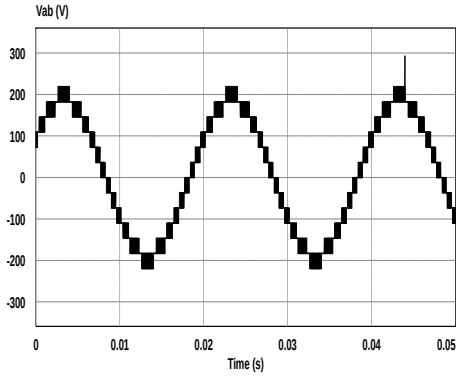


Figure 10. Phase voltage waveform *Vab(V)*for H bridge 7 levels

6.1.4 . Simulation Results of H bridge 15 Level Inverter: Aspect of Phase Voltages V_{ab}(V)

Simulation Example of H bridge 15 Level Inverter: Aspect of Phase Voltages V_{ab}(V) in Figure 11.

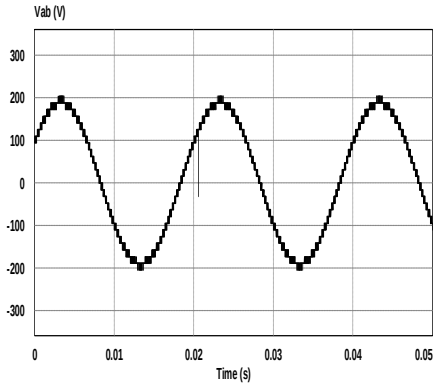


Figure 11. Phase voltage waveform *Vab(V)*for H bridge 15levels

6.2. PWM Suboptimal Simulations

Simulation parameters of suboptimal PWM are grouped in Table 5.

Table 5. Simulation parameters for the suboptimal PWM control

E (V)	Fp(Hz)	Fm(Hz)	Ap	Am	Ah3
110	20k	50	1	1.155	0.1925

6.2.1. Simulation Results of H Bridge 3 Level Inverter: Aspect of Phase Voltages V_{ab} (V)

Simulation Results of H bridge 3 Level Inverter: Aspect of Phase Voltages V_{ab}(V) in Figure 12.

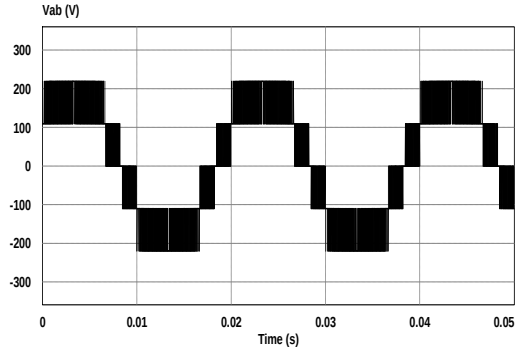


Figure 12. Phase voltage waveform *Vab(V)*for the H bridge 3 levels

6.2.2. Simulation Results of H Bridge 5 Level Inverter: Aspect of Phase Voltages Vab (V)

Simulation Results of H bridge 5 Level Inverter: Aspect of Phase Voltages Vab(V) in Figure 13.

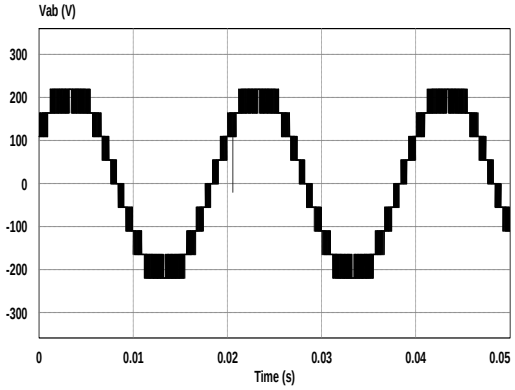


Figure 13. Phase voltage waveform *Vab(V)*for the H bridge 5 levels

6.2.3. Simulation Results of H Bridge 7 level Inverter: Aspect of Phase Voltages Vab (V)

Simulation Results of H bridge 7 Level Inverter: Aspect of Phase Voltages Vab(V) in Figure 14.

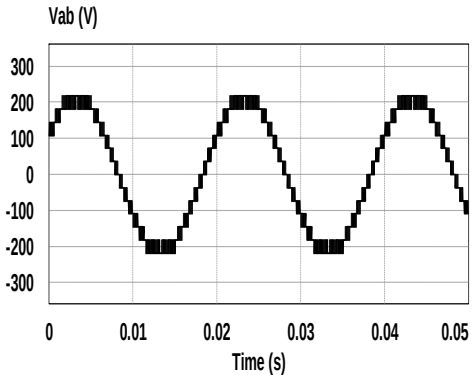


Figure 14. Phase voltage waveform *Vab(V)*for the H bridge 7 levels

6.2.4. Simulation Results of H Bridge 15 Level Inverter: Aspect of Phase Voltages Vab(V)

Simulation Results of H bridge 15 Level Inverter: Aspect of Phase Voltages Vab(V) in Figure 15.

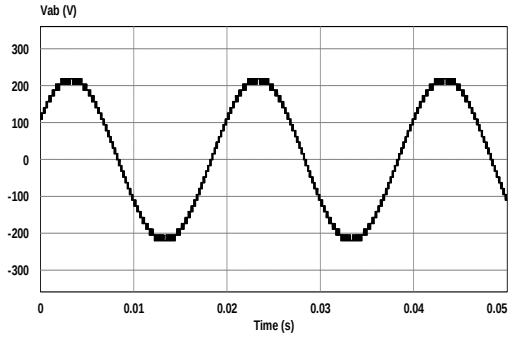


Figure 15. Phase voltage waveform *Vab(V)* for the H bridge 15 levels

7. ANALYSIS OF RESULTS

Table 6 aggregates all the obtained simulation results. We note that the application of SPWM control to the H bridge inverter has led to an increase of the fundamental voltage value at each rise of inverter levels. Table 6 shows the increase of H bridge inverter levels leads to a THD decrease and improves the quality of the output voltage waveform for the two control strategies.

Table 6. Simulation results

Number of level	SPWM		Suboptimal PWM	
	THD (%)	V1	THD (%)	V1
3	35.66	119.08	31.4	133.75
5	17.75	121.53	14.86	138.57
7	11.09	122.22	9.81	138.79
15	4.74	122.33	4.2	141.09

The obtained results concerning the THD from the suboptimal PWM are better than those obtained from the SPWM. Concerning the application of suboptimal PWM control, we see an increase of the fundamental voltage value of the inverter at each level rise.

The Table 7 compares the values of THD resulting from the use of suboptimal PWM of this study with those resulting from the SPWM of the reference [12].

Table 7. THD of output voltage V_{ab} (V) for the suboptimal PWM and the SPWM of reference [12]

Number of level	Suboptimal PWM THD (%)	SPWM [12] THD (%)
3	31.4	61.95
5	14.86	32.04
15	4.2	9.75

8. CONCLUSION

This paper summarizes the research we have done in order to obtain a multilevel inverter and an optimal control with a better value of the fundamental voltage and a reduced THD.

The obtained simulation results show that the H bridge inverter is better than the NPC inverter in terms of operating of the supply source. And the performance in terms of THD and fundamental voltage value of the suboptimal PWM is better than the SPWM.

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