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New Hybrid Structure Based on Improved Switched Inductor Z-Source and Parallel Inverters for Renewable Energy Systems

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ABSTRACT

Nowadays, more and more distributed generations and renewable energy sources, such as wind, solar and tidal power, are connected to the public grid by the means of power inverters. They often form microgrids before being connected to the public grid. Due to the availability of high current power electronic devices, it is inevitable to use several inverters in parallel for high-power and/or low-cost applications. So, inverters should beconnected in parallel to provide system redundancy and high reliability, which are important for critical customers. In this paper, the modeling, designing and stability analysis of parallel-connected three-phaseinverters are derived for application in renewable energy systems. To enlarge voltage adjustability, the proposed inverter employs an improved switched inductor Z-source impedance network to couple the main circuit and the power source. Compared with the classical Z-source inverter (ZSI) and switched inductor Z-source inverter (SL-ZSI), the proposed inverter significantly increases the voltage boost inversion ability and also can increase the power capacity and the reliability of inverter systems. The proposed topology and its performances are validated using simulation results which are obtained in Matlab/Simulink.

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1. INTRODUCTION

In some renewable energy utilization applications, the input power source is a DC voltage source which has a wide voltage variation range, such as the grid-tied photovoltaic generation and fuel cell generation. In these cases, an inverter with boost capability is required to generate electricity at low input DC voltage. Different inverter topologies meeting the requirement can be found and classified into two categories: the isolated inverters and non-isolated inverters. The isolated inverters are usually equipped with a step-up transformer which makes the system bulky and low efficiency while the non-isolated inverter is considered high efficiency and high power density [1]. There are typically two popular non-isolated topology candidates for these applications. One is the traditional two-stage boost-buck inverter (BBI), and the other one is the newly proposed Z-source inverter (ZSI) [2].

The ZSI presents a new single-stage structure to achieve the voltage boost/buck character in a single power conversion stage, which has been reported in applications to renewable energysystems. The ZSI has gained popularity as a single-stage buck-boost inverter topology among many researchers. However, its boosting capability could be limited and therefore it may not be suitable for some applications requiring very high boost demanding of cascading other dc-dc boost converters. This could lose the efficiency and demand more sensing for controlling the added new stages.

Over the recent years, many researchers have given their focus in many directions to develop ZSI to achieve different objectives [3]-[8]. In [9]-[12], the focus is on improving the boost factor of the ZSI. For instance, [9]-[11] add inductors, capacitors, and diodes to the Z-impendence network to produce a high dc-link voltage for the main power circuit from a very low input dc voltage. In [12], two inductors of the impedance Z-network are replaced by a transformer with a turn ratio of 2:1 to obtain high voltage gain. These topologies suit solar cell and fuel cell applications that can require high voltage gain to match the source voltage difference.

Applying switched-capacitor, switched-inductor, hybrid switched-capacitor/switched-inductor structures, voltage-lift techniques, and voltage multiplier cells [13]-[15] to dc–dc conversion provides the high boost in cascade and transformerless structures with high efficiency and high power density. A successful combination of the ZSI and switched-inductor structure, called the switched inductorZSI (SL-ZSI) [9], provides strong step-up inversion to overcome the boost limitation of the classical ZSI.

On the other hand, many industrial systems demand a reliable power supply. One way to increase the reliability is to increase the number of sources. Another way to increase the reliability is to have parallel inverters and this would increase the redundancy as well as the maintainability of the inverters. Moreover, the parallel connected inverters effectively offer a significantly higher level of availability than conventional approaches. Commercially available ratings range from several kVA to hundreds of kVA. Parallel connection techniques for inverters have been gaining increasing attentions in motor-drive systems, converter systems, and distributed generation systems [16]-[19].

Paralleled inverters can be built in numerous ways. First and the most obvious way is to have independent inverters with separate dc sources [20] and the other possibility is to connect the inverters into a common dc source [21]. First method is common as it is simple. However, it requires more than one power source. In the context of *Z*-source inverter, this method requires more than one independent *Z*-source impedance network.Therefore, this paper proposes a new hybrid structure based on improved SL Z-source impedance network and parallel inverters which share one dc-input voltage to increasethe output voltage in a wide range, usable in renewable energy systems. Moreover, because of the divided output current among parallel inverters, the proposed topology has the ability of supplying high load currents.

The remainder of this paper is organized as follows. The next section is devoted to a detailed topology analysis of the improved SL Z-source impedance network. Operating principles and the equivalent circuit of the proposed topology are presented in section 3. Section 4 presents the simulation results and finally, conclusions are included in Section 5.

2. CIRCUIT ANALYSIS OF THE IMPROVED SL Z-SOURCE IMPEDANCE NETWORK

As illustrated in Figure 1, the proposed improved SL Z-source impedance network consists of six inductors, two capacitors and twelve diodes. The combination of L_1, L_2, L_3, D_1, D_2, D_3, D_4, D_5, D_6 and the combination of L_4, L_5, L_6, D_7, D_8, D_9, D_{10}, D_{11}, D_{12} performs the function of the top SL cell and the bottom SL cell, respectively. Both of these two SL cells are used to store and transfer the energy from the capacitors to the dc bus under the switching action of the main circuit.

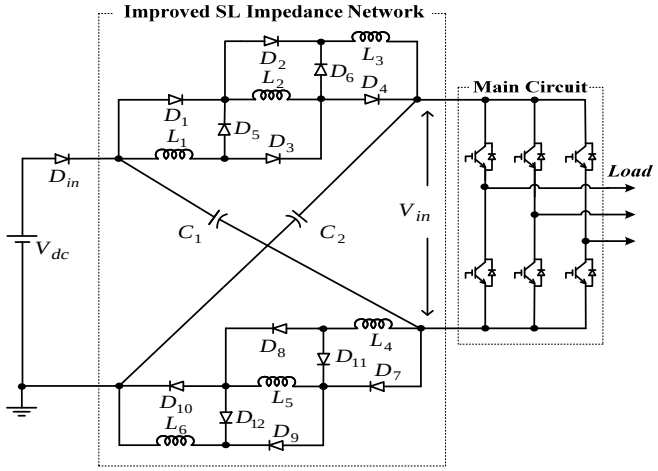

Figure 1. Topology of the improved SL-ZSI

From the viewpoint of the switching states of the main circuit connected with SL impedance network, the operation principles of this impedance network are similar to those of the classical Z-source impedance network. For the convenience of analysis, the equivalent circuit of the improved SL Z-source impedance network viewed from the dc bus is shown inFigure 2(a) in which a virtual active switch S and a passive switch D_o are introduced tosimulate the practical shoot-through actions of the top and bottom arms.Therefore, the sub-states of this impedance network are classified into the shoot-through state and the non-shoot-through state, respectively.

2.1. Shoot-Through State

During this sub-state, S is ON, while both D_{in} and D_o are OFF.For inductors of the top branch, four diodes D_1, D_2, D_3 and D_4 are ON, while two diodes D_5 and D_6 are OFF. Then, three inductors L_1, L_2, L_3 are connected in parallel and charged by capacitor C_1. For inductors of the bottom branch, four diodes D_7, D_8, D_9 and D_{10} are ON, while two diodes D_{11} and D_{12} are OFF. Three inductors L_4, L_5, L_6 are connected in parallel and charged by capacitor C_2. The equivalent circuit is shown in Figure 2(b).

2.2. Non-Shoot-Through State

This state corresponds to the six active states and two zero states of the main circuit and the equivalent circuit is shown inFigure 2(c).During this sub-state, S is OFF, while both D_{in} and D_o are ON. For inductors of the top branch, four diodes D_1, D_2, D_3 and D_4 are OFF, while two diodes D_5 and D_6 are ON. Then, three inductors L_1, L_2, L_3 are connected in series and stored energy is transferred to inverter circuit. For inductors of the bottom branch, four diodes D_7, D_8, D_9 and D_{10} are OFF, while two diodes D_{11} and D_{12} are ON. Then, three inductors L_4, L_5, L_6 are connected in series and stored energy is transferred to inverter circuit.

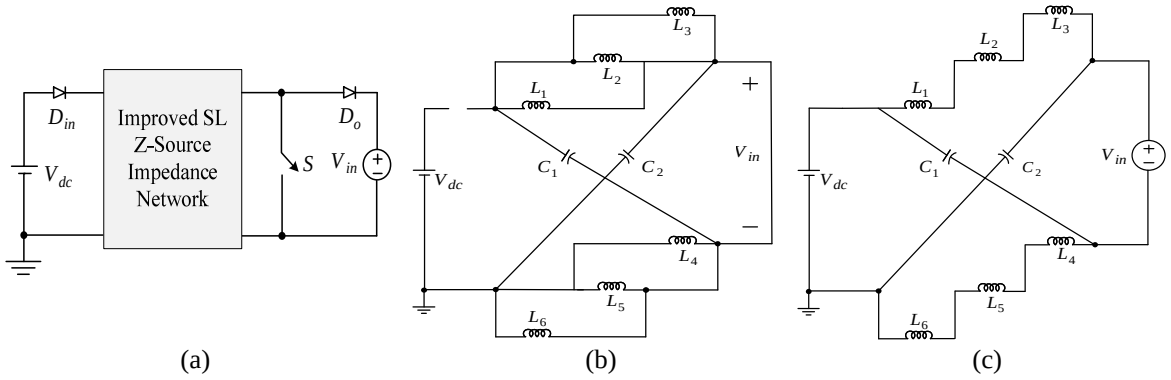

Figure 2. Equivalent circuits. (a) Improved SL-ZSI viewed from the dc-link bus.
(b) Shoot-through zero state. (c) Non-shoot-through zero state.

Assuming that the six inductors (L_1, L_2, L_3, L_4, L_5 and L_6) have the same inductance (L) and two capacitors(C_1 and C_2) have the same capacitance (C). As aresult, the network becomes symmetrical. From symmetrical circuit, the voltage across the capacitors and inductors become:

$$V_{C1} = V_{C2} = V_C \tag{1}$$

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_{L5} = v_{L6} = v_L \tag{2}$$

From Figure 2(b) that shows the equivalent circuit of the shoot-through state:

$$v_L = V_C \ , v_{in} = 0 \tag{3}$$

Now consider non-shoot-through state. From Figure 2(c), the voltageequations can be obtained:

$$3v_L = V_{dc} - V_C \tag{4}$$

$$v_{in} = V_C - 3v_L = 2V_C - V_{dc} \tag{5}$$

From the fact that the average voltages across the inductors during each switching cycle T are zero, the following equation can be derived:

$$V_L = \bar{v}_L = \frac{T_0 V_C + (T - T_0)(\frac{V_{dc} - V_C}{3})}{T} = 0 \tag{6}$$

Where, T_0 is the shoot-through time interval over a switching cycle, or $(T_0 / T) = D$ is the shoot-through duty ratio.

From (6),

$$V_C = \frac{1-D}{1-4D} V_{dc} \tag{7}$$

Therefore, the peak dc-link voltage across the inverter bridge can be written:

$$\hat{v}_{in} = V_C - 3v_L = 2V_C - V_{dc} = \frac{1+2D}{1-4D} V_{dc} \tag{8}$$

Thus, the boost factor B is expressed as:

$$B = \frac{1+2D}{1-4D} = \frac{1+2(T_0/T)}{1-4(T_0/T)} \geq B_1 \geq B_0 \tag{9}$$

Where, B_0 and B_1 are defined as the boost factor of the classical Z-source and switched inductor Z-source impedance networks, respectively. Their expressions are given by [9] as:

$$B_0 = \frac{1}{1-2D} = \frac{1}{1-(T_0/T)}, \quad B_1 = \frac{1+D}{1-3D} = \frac{1+(T_0/T)}{1-3(T_0/T)} \tag{10}$$

For the comparison of the individual boost ability, the curves of the boost factor B versus the duty ratio D for improved SL Z-source, SL Z-source and classical Z-source impedance networks are shown in Figure 3. As shown in Figure 3, the boost ability of the improved SL Z-source impedance network is significantly increased compared with SL Z-source and classical Z-source impedance networks.

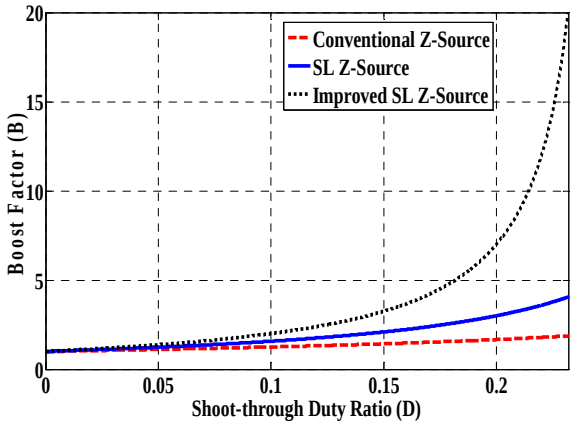

Figure 3. Boost ability comparison

3. THE PROPOSED TOPOLOGY

Parallel operation of inverters has many advantages such as modularity, ease of maintenance, $(n+1)$ redundancy, high reliability and many others [22-24]. In addition to these, output current ripple of the paralleled inverter can be reduced significantly by virtue of interleaving effect [25]. The basic concept of the proposed improved SL Z-source impedance network with N-parallel inverters is shown in Figure 4.

It is assumed that all inverters share the same dc bus that is fed from improved switched inductor Z-source impedance network.Since the voltage at the point of common connection is derived from the switching of different power semiconductors, an intermodule reactor is absolutely necessary to interconnect the different inverters.

As described in [3], two PWM control methods, termed as the simple boost control method and the maximum boost control method have been explored, which result in the different relationships of the voltage boost inversion ability versus the given modulation index M . Since the aforementioned two methods can be regarded as the theoretical basis of various advanced PWM strategies such as the third-harmonic injection method and the space vector PWM method, the proposed structure under the condition of these two methods will be explored in the following discussions, respectively. For the convenience of illustration, the waveforms and switching strategies of aforementioned two methods are shown together in Figure 5.

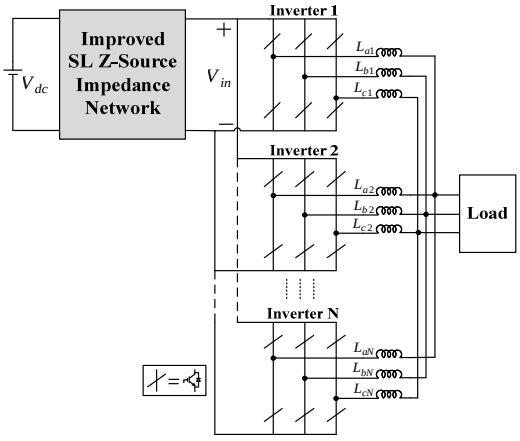

Figure 4. Parallel improved SL Z-source inverters

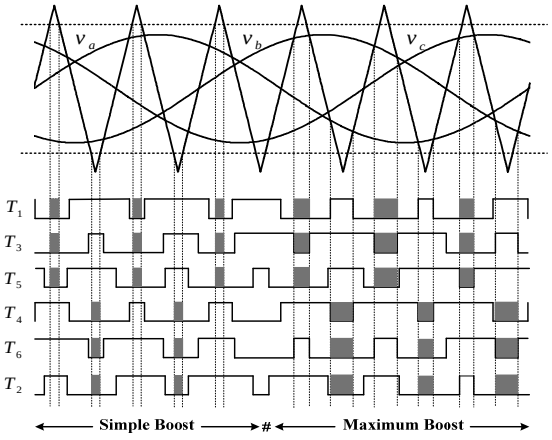

Figure 5. Waveforms and switching strategies of two basic PWM control methods

It is seen fromFigure 5that in the simple boost control, a straight line equal to or greater than the peak value of the three phase references is employed. The obtainable duty ratio of the shoot-through state can be regarded as a constant value, and its maximum value is limited to $(1-M)$. The voltage conversion ratio of the whole inverter G can be expressed by:

$$G = MB = \frac{\hat{v}_{out}}{V_{dc}/2} \tag{11}$$

Where, $\hat{v}_{out}$ is the peak value of the output phase voltage. Therefore, the maximum voltage conversion ratio $G_{\max}$ versus any desired modulation index M can be expressed by:

$$G_{\max} = MB\big|_{D=1-M} = \frac{M(3-2M)}{4M-3} \geq G_{1-s} \geq G_{0-s} \tag{12}$$

Where, G_{0-s} and G_{1-s} are defined as the maximum voltage conversion ratio of the classical ZSI and SL-ZSI, respectively. Their expressionsare given by [9] as follows:

$$G_{0-s} = \frac{M}{2M-1}, G_{1-s} = \frac{M(2-M)}{3M-2} \tag{13}$$

For the maximum boost control method as shown in Figure 5, the key point is that all zero states need to be turned into the shoot-through state so as to make the duty ratio as large as possible. Therefore, the shoot-through duty cycle varies in each cycle. As described in [3], the average duty ratio of the shoot-through zero state, $\bar{D}$ is expressed by:

$$\bar{D} = \frac{\bar{T_0}}{T} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \tag{14}$$

Substituting (14) into (9), we can get the equivalent boost factor $\bar{B}$ under the condition of variable duty ratios:

$$\bar{B} = \frac{1+2\bar{D}}{1-4\bar{D}} = \frac{6\pi - 6\sqrt{3}M}{12\sqrt{3}M - 6\pi} \tag{15}$$

Therefore, the maximum voltage conversion ratio $G_{\max}$ versus any desired modulation index M approximates to:

$$G_{\max} = M\bar{B} = \frac{M(6\pi - 6\sqrt{3}M)}{12\sqrt{3}M - 6\pi} > G_{1-m} > G_{0-m} \tag{16}$$

Where, G_{0-m} and G_{1-m} are defined as the maximum voltage conversion ratio of the classical ZSI and SL-ZSI, respectively. Their expressionsare given by [9] as follows:

$$G_{0-m} = \frac{\pi M}{3\sqrt{3}M - \pi}, G_{1-m} = \frac{M(4\pi - 3\sqrt{3}M)}{9\sqrt{3}M - 4\pi} \tag{17}$$

Figure 6(a) shows the maximum obtainable voltage conversion ratios versus the given modulation index under the simple boost control condition. It is shown that the voltage boost ability is unavailable at $M = 1$.However, if $M < 1$, with the decreasing of M, the voltage boost inversion ability of the proposed inverter becomes much stronger than SL-ZSI and classical ZSI. It means that for a given voltage conversion ratio, a higher modulation index can be used in the proposed inverter to improve the inverter output performance.

Figure 6(b) shows the maximum obtainable voltage conversion ratios versus the given modulation index under the maximum boost control condition. It is shown that the voltage boost inversion abilities of theseinverters have been enhanced to a wider range by this method. Similar to the observation in Figure 6(a), the proposed inverter exhibits its advantage of stronger voltage boost inversion ability at the low modulation index.

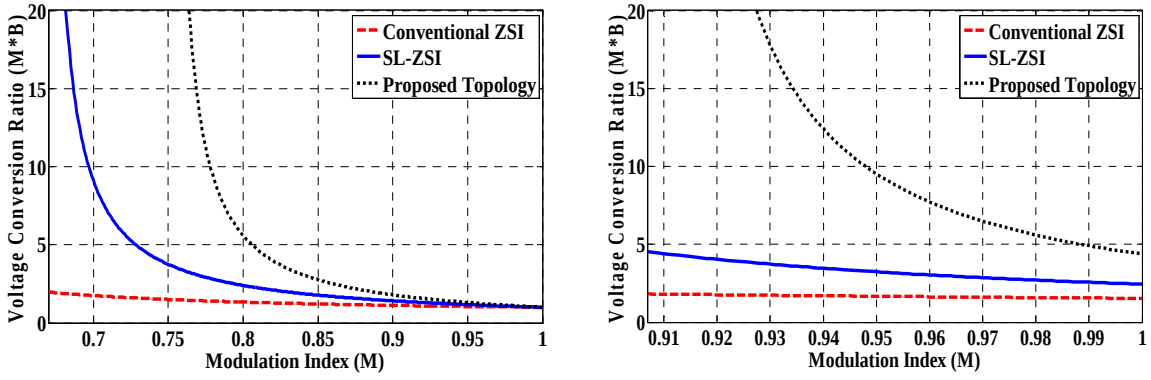

Figure 6. Maximum voltage conversion ratio. (a) Under the simple boost control condition. (b) Under the maximum boost control condition.

Figure 7 shows a simplified equivalent circuit of the system illustrated in Figure 4. It is assumed that each inverter develops a balanced three phase voltage and its intermodule reactor consists of identical phase inductors. However, differences may exist between different inverter modules, both in voltage and reactance.

Under such assumptions, the equivalent circuit illustrated in Figure 7, may be further simplified into a phasor equivalent circuit shown in Figure 8. Here, each inverter is represented by its internal phasor voltage source, and one inductor and one resistor representing the equivalent series resistance of the circuit.

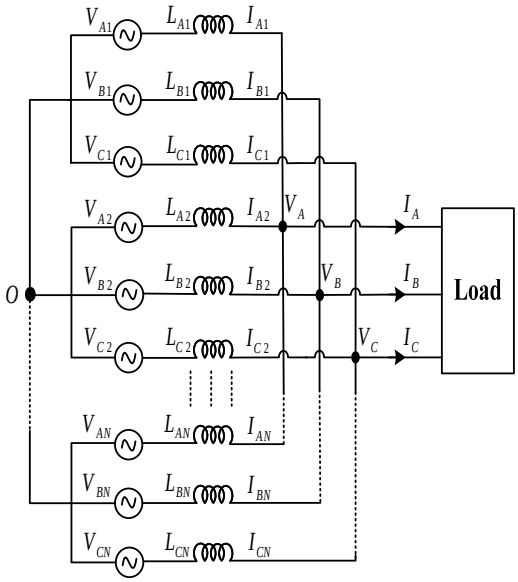

Figure 7. Simplified equivalent circuit

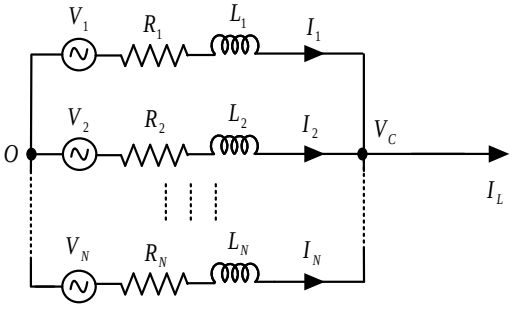

Figure 8. Simplified phasor model

Inverter pole voltage and current vectors can be defined as $(V_1\ V_2\ ...\ V_N)^T$ and $(I_1\ I_2\ ...\ I_N)^T$ respectively, corresponding to the labels illustrated in Figure 8. Now, the thevenin impedance of i^{th} inverter, Z_i may be identified to be:

$$Z_i = R_i + j\omega L_i \quad , \quad i = 1, 2, ..., N \tag{18}$$

And the equivalent thevenin impedance of all inverters in parallel, Z_{TH} , may be determined as:

$$Z_{TH} = Z_1 \square Z_2 ... \square Z_N \tag{19}$$

Furthermore, the voltage at the common coupling point can be calculated to be:

$$V_C = Z_{TH}\left(\sum_{j=1}^{N} \frac{V_j}{Z_j} - I_L\right) \tag{20}$$

Now, the output current of the i^{th} inverter can be evaluated as:

$$I_i = \frac{Z_{TH}}{Z_i} I_L + \frac{V_i}{Z_i} - \sum_{j=1}^{N}\left(\frac{V_j}{Z_j}\frac{Z_{TH}}{Z_j}\right) \quad , \quad \forall i \tag{21}$$

From equation 21 and Figure 6, it can be derived the proposed structure can achieve higher voltage than the previous converters and also, because of dividing the output current between parallel inverters, the probable damages to the switches which can be caused by high currents are preventable and this will increase the reliability of the system.

It may be observed from (21), that various Z_i play an important role in determining the sharing of current between the different modules. In order to quantify this phenomenon, the sensitivity of the current to the thevenin impedance, Z_i can be determined to be:

$$\frac{\partial I_i}{\partial Z_i} = -Z_{TH}\frac{I_L}{Z_i^2} - \frac{V_i}{Z_i^2} + 2V_i\frac{Z_{TH}}{Z_i^3} \quad , \quad \forall i \tag{22}$$

Therefore, small deviations in equivalent thevenin impedances of inverters can result in uneven current distributions as suggested by (21).From (22), we can also observe that, if the thevenin impedance is increased, the dependence of output current on the output impedance is also decreased leading to better current distribution.

4. SIMULATION RESULTS

Extensive computer simulation using MATLAB-Simulink has been performed to prove performance of the proposed inverter. The simulation schematic for the proposed topology is shown in Figure 9and the selected parameters are: $V_{dc} = 36\text{V}$, $L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = 1\text{mH}$, $C_1 = C_2 = 1000\mu\text{F}$, Switching frequency = 10kHz, $L_f = 1\text{mH}$ and $C_f = 22.5\mu\text{F}$ (Three-phase output filter), Three-phase resistive load = 10/phase. In the simulation, all components are assumed ideal. The proposed topology is compared to the other topologies which have been proposed in [2] and [9], under the simple boost control method (case 1) and the maximum boost control method (case 2) with the same shoot-through duty ratio.

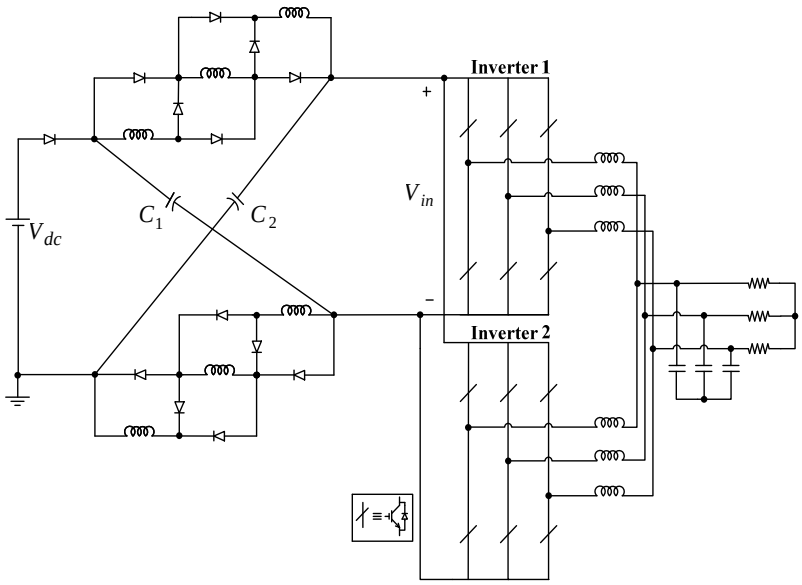

Figure 9. Schematic of two parallel inverters based on improved SL Z-source impedance network

4.1. Simple Boost Control

The proposed system works with shoot-through duty ratio $D = 0.2$ and modulation index $M = 0.8$. We obtain $B = 7$ and $G = 5.6$ using mentioned equations.Figure 10 showsthe simulation results for the proposed topology which are voltage across the inverters (V_{in}), voltage of capacitors (V_C), output voltage, current waveforms of the up and down inverters and also the load current waveform, respectively. It is seen that the steady-state performance in the simulation is identically matching to the theoretical analysis.

In order to compare the proposed structure with previous structures, we apply the same values of D and M to the classical ZSI and SL-ZSI, and the boost inversion ability will be decreased sharply. The corresponding parameters are $B = 1.67$, $G = 1.336$ for the classical ZSI and $B = 3$, $G = 2.4$ for the SL-ZSI, which are much lower than those achieved by the proposed inverter. The simulation results for these

structures are shown in Figures 11 and 12, respectively. By comparison between simulation results, it is completely obvious that the proposed structure can transfer higher power than the other topologies.

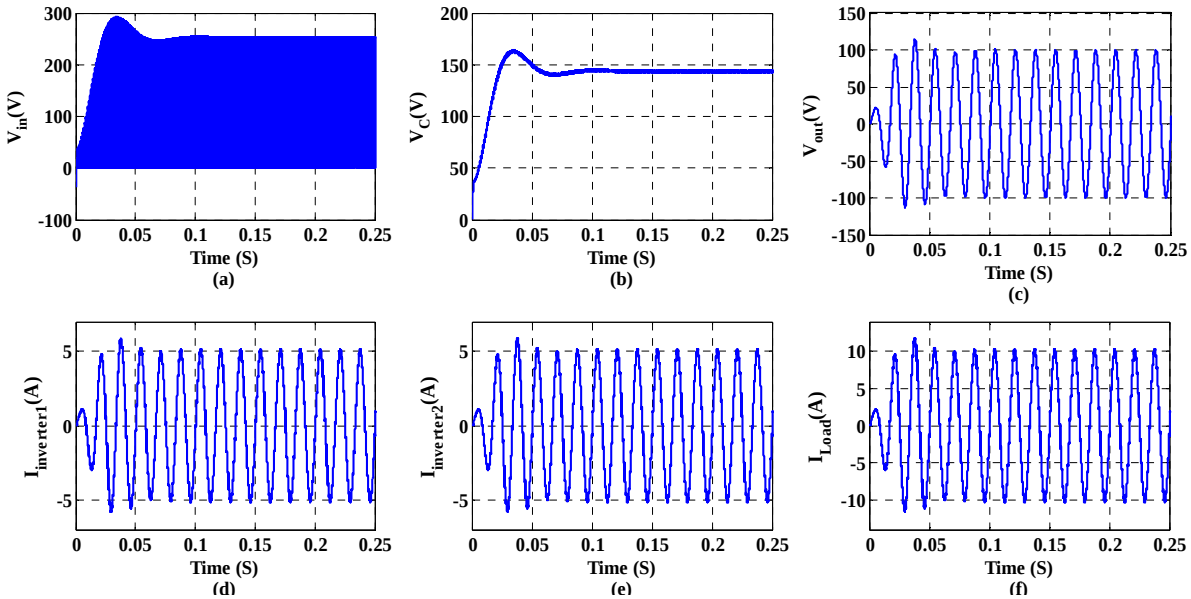

Figure 10. Simulation results of the proposed topology (case 1)

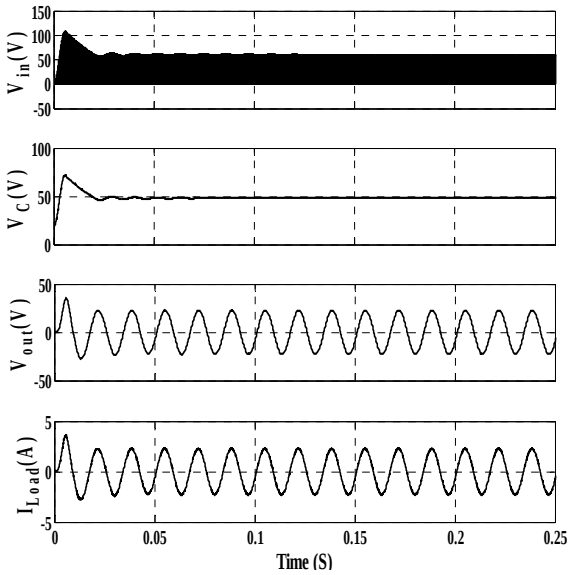

Figure 11. Simulation results of the ZSI (case 1)

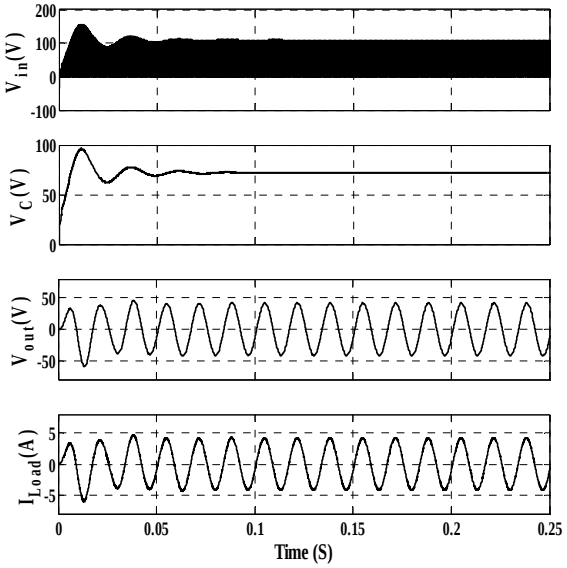

Figure 12. Simulation results of the SL-ZSI (case 1)

4.2. Maximum Boost Control

Under the condition of the maximum boost control, according to (14-16), we consider $M = 0.967$. Therefore, we obtain $\bar{D} = 0.2$, $\bar{B} = 7$ and $G_{\max} = 6.769$. The simulation results for the proposed topology are plotted in Figure 13, which are voltage across the inverters (V_{in}), voltage of capacitors (V_C), output voltage, current waveforms of the up and down inverters and also the load current waveform, respectively. Because the duty ratio varies periodically, a small oscillation has been introduced into V_{in} and V_C. All simulation results comply with the equations derived in sections 2 and 3.

For the case of the classical ZSI and SL-ZSI, when M is taken as 0.967, the boost inversion ability is still very weak. The corresponding parameters are: $\overline{B} = 1.668$, $G_{\max} = 1.613$ for the classical ZSI and $\overline{B} = 3$, $G_{\max} = 2.901$ for the SL-ZSI. The simulation results for these structures are shown in Figures 14 and 15 respectively.

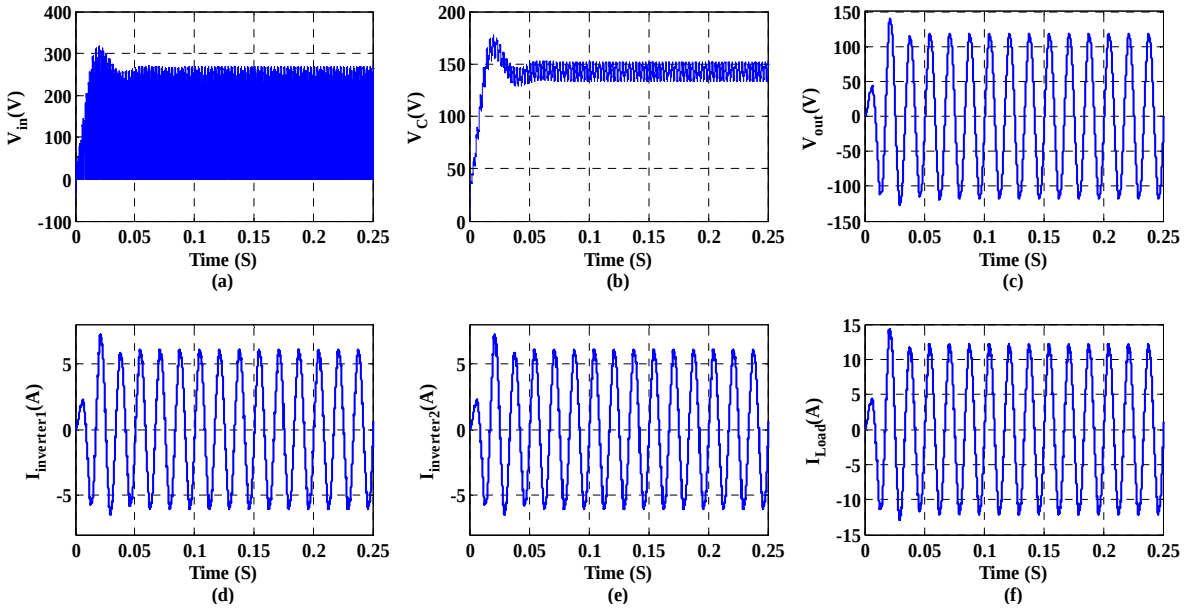

Figure 13. Simulation results of the proposed topology (case 2)

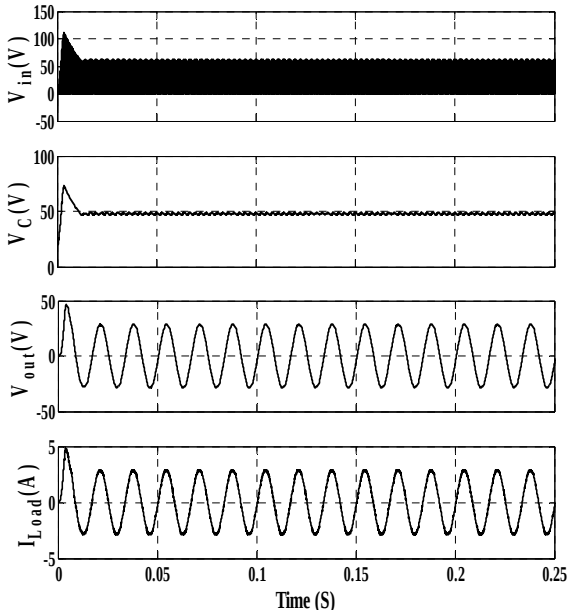

Figure 14. Simulation results of the ZSI (case 2)

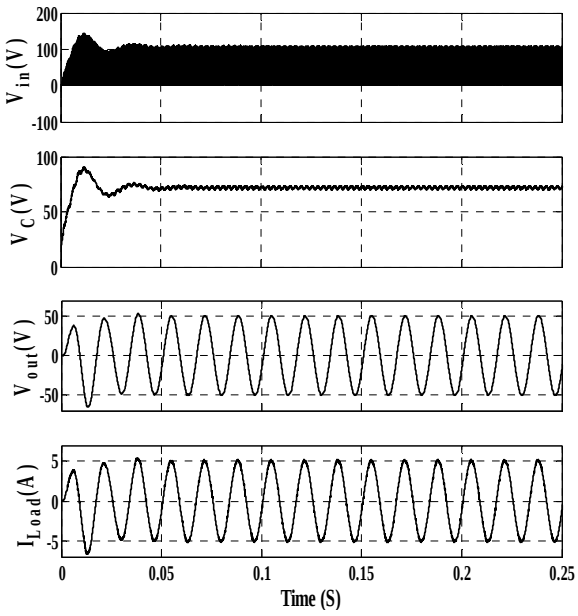

Figure 15. Simulation results of the SL-ZSI (case 2)

The improved switched inductor Z-source structure is extensible for the further development using the coupled inductor techniques and other potential improving techniques.Additionally, in conditions where the load requires higher current, in order to prevent the probable damages to the switches, by increasing the number of inverters in parallel we can supply the load by desired current.

5. CONCLUSION

This paper has presented a new hybrid structure based on improved switched inductor Z-source and parallel inverters to expand the range of system's voltage gain and supply high load currents. With this structure, the proposed inverter has the following features:

- The proposed inverter has all the advantages of paralleling power converters such as modularity, ease of maintenance, (n + 1) redundancy, high reliability, reducing of the output current ripple, etc.
- It can be short- or open-circuited without damaging switching devices. Therefore, it is very resistant to EMI noise and therefore its robustness and reliability are significantly improved.
- The boost factorhas been increased to (1 + 2D)/1-4D).
- Since here the load current can be divided between all inverters, in conditions where the load requires high current, the probable damages to the switches which can be caused by high currents are preventable.

The steady state operation is performed to analyze the boosting capability then it is validated by simulation results.

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