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On the Impact of Timer Resolution in the Efficiency Optimization of Synchronous Buck Converters

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ABSTRACT

Excessive dead time in complementary switches causes significant energy losses in DC-DC power conversion. The optimization of dead time prevents the degradation of overall efficiency by minimizing the body diode conduction of power switches and, as a consequence, also reduces reverse recovery losses. The present work aims at analyzing the influence of one of the most important characteristics of a digital controller, the timer resolution, in the context of dead-time optimization for synchronous buck converters. In specific, the analysis quantifies the efficiency dependency on the timer resolution, in a parameter set that comprises duty-cycle and dead-time, and also converter frequency and analog-to-digital converter accuracy. Based on a sensorless optimization strategy, the relationship between all these limiting factors is described, such as the number of bits of timer and analog-to-digital converter. To validate our approach experimental results are provided using a 12-to-1.8V DC-DC converter, controlled by low- and high-resolution pulse-width modulation signals generated with an XMC4200 microcontroller from Infineon Technologies. The measured results are consistent with our analysis, which predicts the power efficiency improvements not only with a fixed dead time approach, but also with the increment of timer resolution.

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1. INTRODUCTION

Digital control has been making inroads in the design of low-power dc-dc converters. Besides the benefits brought by digital processing on nonlinear control capabilities, reconfigurability, and reduced noise susceptibility [1, 2], other useful functions become feasible with a digitally-controlled power converter. For instance, the ability to further optimize the energy efficiency, while keeping track of it, is of great value for any power converter system. The present work addresses specifically this issue, by implementing an algorithm for minimizing specific power losses on a synchronous buck-converter, and investigating the influence of the main resources on the optimization performance.

In a synchronous buck-converter, a minimum dead time is often required to prevent the occurrence of shoot-through currents. However, this short time has the side effect of forward biasing the internal body diode in the synchronous switch, causing high conduction losses. These energy losses can be described as [3]

$$P_{\text{loss}} = V_D I_{\text{out}} \frac{t_{\text{d,r}} + t_{\text{d,f}}}{T_{\text{s}}} \tag{1}$$

where V_D is the diode voltage drop, I_{out} the output current, T_s the switching period, and $t_{\text{d,r}}$ and $t_{\text{d,f}}$ the rising and falling edge dead times, respectively. Fig. 1 illustrates these control signals together with the schematic for the buck topology used in this work. A single feedback loop is applied for voltage mode control, with a digital proportional-integral (PI) controller. The proposed efficiency optimization takes place in the digital domain, following the PI controller, without the need for significant changes in the feedback structure.

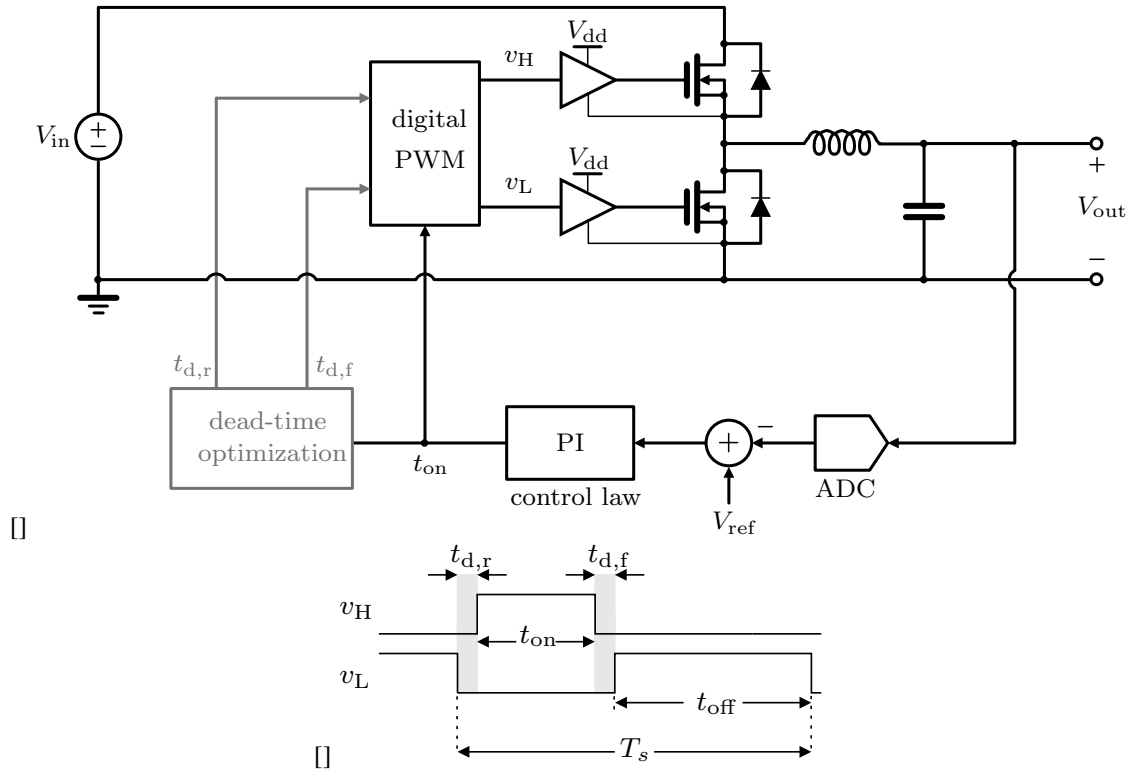


Figure 1. Synchronous buck converter (a) block diagram; and (b) PWM signals with dead time.

Numerous solutions can be adopted for dead-time optimization. The simplest approach relies on a fixed dead time $t_{\rm d}$. Most gate driving integrated circuits (ICs) and microcontrollers already have complementary PWM modes with fixed dead time. Nevertheless, as the optimum efficiency varies according to operation conditions (e.g. load, input voltage, temperature, aging, etc.), the worst condition is often used to define $t_{\rm d}$ to avoid shoot-through, thus the efficiency is not kept maximized. Alternatives to define an optimum dead time imply detecting body-diode conduction [4], or preventing its occurrence by emulating a diode behavior in the control [5, 6], or by zero crossing detection of the switching-node voltage ($v_{\rm DS}$) on the synchronous switch [7]. Although such adaptive methods can be quite fast – about one switching cycle – their main drawback is the additional hardware required to sense $v_{\rm DS}$, and in some cases the control signal $v_{\rm GS}$ as well. If some speed can be sacrificed, an interesting improvement is the so called predictive delay [3, 4], in which information from the previous cycle is also included in deciding the present dead time.

Most of the optimization approaches just mentioned make use of supplementary circuitry to sense the voltage at the switching node. In contrast, sensorless approaches rely only on existent hardware [8, 9, 10]. These methods make use of parameters being already sensed, such as the output voltage usually acquired for regulation purposes, or the input current, which is sometimes sensed for current-mode control or circuit protection. In [10], the authors employ input current sensing to keep track of the maximum efficiency. Optimum conditions for the dead time are achieved at a minimum input current. Similarly, in [11, 12] the dead times are varied until the duty cycle gets its minimum value. At this particular point, the losses at the body diode should be minimized, which as a consequence reduce also the reverse recovery losses. This way the peak efficiency can be tracked without actually measuring it.

In this paper, the impact of the digital controller resources on the efficiency improvement is studied, namely the timer resolution that affects the dead time and duty cycle accuracies, the resolution of the analog-to-digital conversion (ADC), input and reference voltages, and the switching period. A dead-time optimization algorithm similar to [11] is adopted here, for its simplicity and the relatively low computation overhead. The remainder of this paper is organized as follows. Next section presents the dead-time optimization analysis of the proposed digitally-controlled synchronous buck-converter, in terms of digital resource usage, operation limits, and attainable improvement. Practical implementation and prototype measurements are presented in the third section, and final remarks are following presented, concluding this paper.

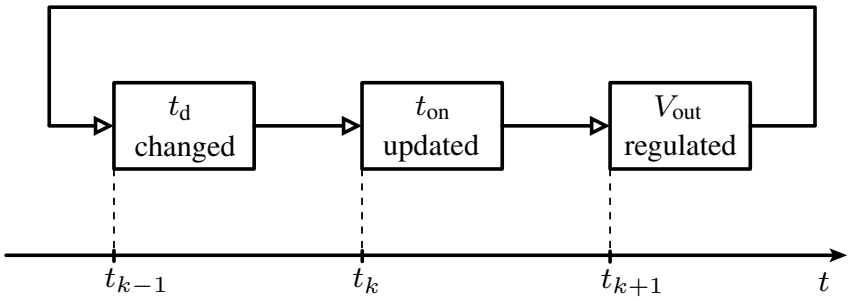


Figure 2. Dead time optimization algorithm steps.

2. ANALYSIS OF DEAD-TIME OPTIMIZATION

The proposed buck converter with dead-time optimization is depicted in Fig. 1. The voltage at the output is sensed by an ADC channel and the feedback control loop is completely performed in the digital domain, whereas the duty cycle is set by a digital PI controller. When the output is stable, its value is determined by a function of the dead time and duty cycle, such as follows

$$V_{\mathrm{out}} = V_{\mathrm{in}} \frac{t_{\mathrm{on}}}{T_{\mathrm{s}}} - V_D \frac{t_{\mathrm{d,r}} + t_{\mathrm{d,f}}}{T_{\mathrm{s}}} \tag{2}$$

where V_{in} is the input voltage and $t_{\mathrm{on}}/T_{\mathrm{s}}$ the duty cycle. In fact, the dead time has an opposite effect to the duty cycle on the output voltage. Nevertheless, if V_{out} is constant, changing one of these parameters automatically affects the other. This is actually the essence of some dead-time algorithms [8, 9, 10, 11, 12]. Fig. 2 depicts the three main steps of a generic algorithm, which can be summarized as follows[1]

1. At a given time instant $t_{\mathrm{k\text{-}1}}$, the dead time t_{d} is changed (for simplicity let us assume $t_{\mathrm{d,r}} + t_{\mathrm{d,f}} = t_{\mathrm{d}}$). Prior to any compensation in the duty cycle, $\Delta t_{\mathrm{on}} = 0$, this change in t_{d} will disturb the output voltage, introducing some variation ΔV_{out} given by
$$\Delta V_{\mathrm{out}} = V_D \frac{\Delta t_{\mathrm{d}}}{T_s}, \qquad \Delta t_{\mathrm{on}} = 0 \tag{3}$$
2. At t_{k}, the controller detects the output voltage variation and compensates this deviation by changing the duty cycle accordingly
$$\Delta t_{\mathrm{on}} = T_s \frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{in}}}, \qquad \Delta t_{\mathrm{d}} = 0 \tag{4}$$
3. At $t_{\mathrm{k+1}}$, the output returns to its regulated value, with the converter now operating with new values both for the duty cycle and dead time
$$\Delta t_{\mathrm{d}} = \frac{V_{\mathrm{in}}}{V_D} \Delta t_{\mathrm{on}}, \qquad \Delta V_{\mathrm{out}} = 0 \tag{5}$$

The three equations (3)–(5) have been derived derived from (2) and define the set of possible operation points for the algorithm. This set of points is represented by

$$\mathbf{r} = (\Delta t_{\mathrm{on}}, \Delta t_{\mathrm{d}}, \Delta V_{\mathrm{out}}) = \Delta t_{\mathrm{on}} \cdot (1, V_{\mathrm{in}}/V_D, V_{\mathrm{in}}/T_{\mathrm{s}}) \tag{6}$$

which, geometrically, represents a straight line in $\mathbb{R}^3$. Naturally, $\mathbf{r}$ is limited in domain because the algorithm is running on a microcontroller with finite resources, in specific the ADC and timer.

2.1. Operation limits

The output voltage variation is only detectable if it is larger than one least-significant bit of the ADC. The duty cycle and dead time are defined by the PWM signals produced by the timer, which also has a limited resolution. These constraints can be represented in terms of ADC and timer bits, respectively N_{ADC} and N_{timer}, given by

$$\Delta V_{\mathrm{out}} \geq \frac{V_{\mathrm{ref}}}{2^{N_{\mathrm{ADC}}}} \tag{7}$$

$$\Delta t_{\mathrm{d}}, \Delta t_{\mathrm{on}} \geq \frac{T_{\mathrm{s}}}{2^{N_{\mathrm{timer}}}} \tag{8}$$

[1]The time instants relative to t_k are merely indicative of the algorithm states rather than true sequential sample times.

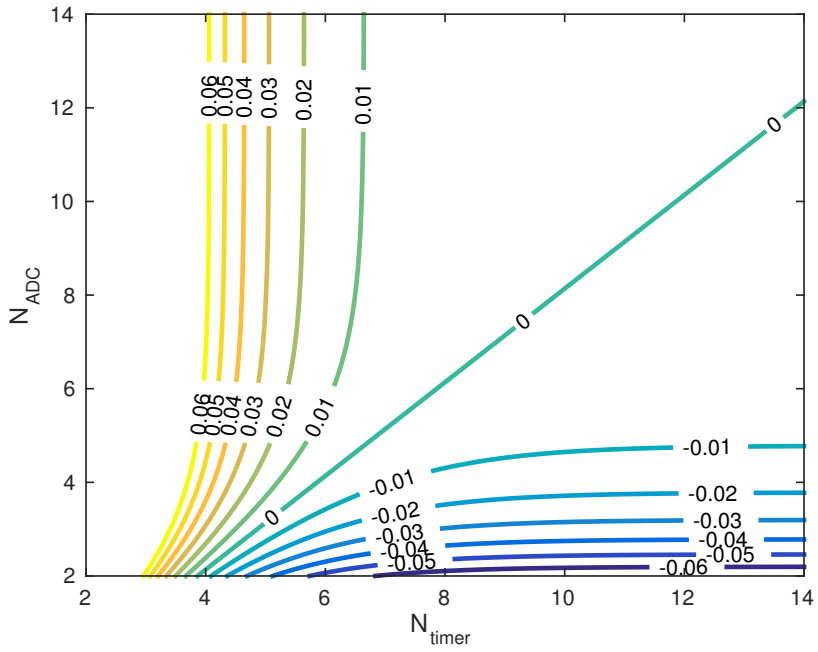


Figure 3. Contour plot of φ for $V_{\text{ref}}/V_{\text{in}} = 0.275\text{V}$ in terms of number of bits for the timer (N_{timer}) and ADC (N_{ADC}).

Taking such limitations into account, the minimum dead time variation, $\Delta t_{\text{d,min}}$, can be expressed as

$$\Delta t_{\text{d,min}} = T_{\text{s}} \frac{V_{\text{in}}}{V_D} \cdot \max\left\{ \frac{1}{2^{N_{\text{timer}}}}, \frac{V_{\text{ref}}}{V_{\text{in}}} \frac{1}{2^{N_{\text{ADC}}}} \right\} \tag{9}$$

where the minimum operation point guarantees the maximum algorithm resolution. Graphically, the minimum operation point can be determined by simply finding the intersection between the line containing the set of all possible solutions with one of the three planes that impose the aforementioned constraints.

2.2. Resource utilization

The algorithm operation point is defined by one of two arguments of function $\max(\cdot)$ given in (9). Let us now define the parameter φ as the difference between the two arguments so that one can evaluate the usage of resources in the algorithm

$$\varphi = \frac{1}{2^{N_{\text{timer}}}} - \frac{V_{\text{ref}}}{V_{\text{in}}} \frac{1}{2^{N_{\text{ADC}}}} \tag{10}$$

Fig. 3 depicts the contour plot of φ given by (10). When φ is positive, the minimum dead-time variation $\Delta t_{\text{d,min}}$ is defined by the first argument in (9) and the optimization is limited by the timer resolution. Conversely, if φ is negative, $\Delta t_{\text{d,min}}$ is defined by the second argument and the optimization is limited by the ADC. Such limitation means that, no matter how much the other resource is improved, $\Delta t_{\text{d,min}}$ will not decrease and the optimization will not improve. Ideally, in this context, φ is null and there are no unused resources, which implies

$$N_{\text{ADC}} = N_{\text{timer}} - \log_2\left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right) \tag{11}$$

Thus, typically, $N_{\text{ADC}} > N_{\text{timer}}$.

2.3. Power efficiency improvement

Considering the minimum algorithm operation point, which yields a dead-time variation of $\Delta t_{\text{d,min}}$, the power losses caused by an initial dead time $t_{\text{d,ini}}$, $P_{\text{loss,ini}}$, can be eliminated in power steps

$$\Delta P_{\text{loss,min}} = V_{\text{D}} I_{\text{out}} \cdot \frac{\Delta t_{\text{d,min}}}{T_s} \tag{12}$$

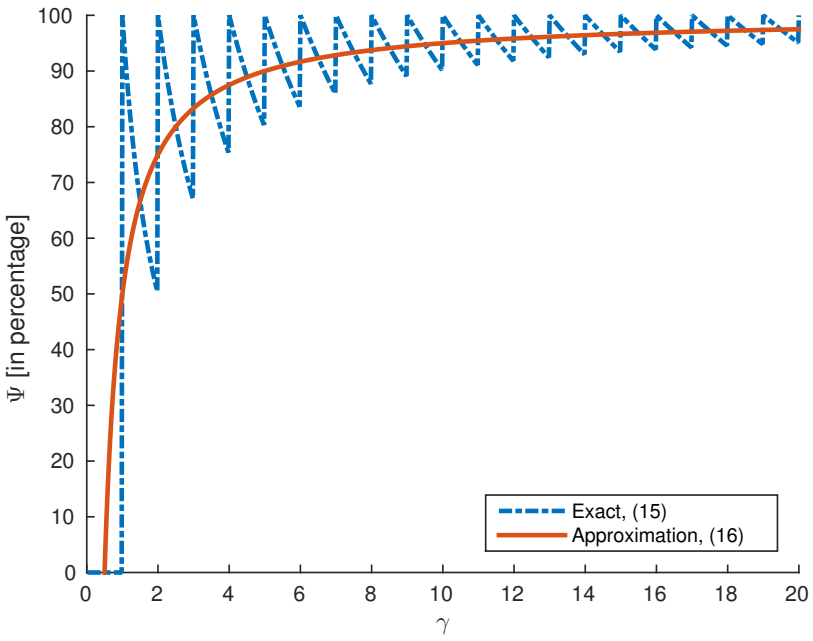


Figure 4. Plots of $\Psi(\gamma)$ using the floor function and its approximation.

The number of steps necessary to fully eliminate the initial losses can be expressed as

$$\gamma = \frac{\Delta P_{\text{loss,min}}}{P_{\text{loss,ini}}} = \frac{\Delta t_{\text{d,min}}}{t_{\text{d,ini}}} \tag{13}$$

Since only an integer number of steps can be taken, i.e. $\lfloor \gamma \rfloor$, the ratio between eliminated and initial losses, Ψ, can be expressed as

$$\Psi = \frac{P_{\text{loss,elim}}}{P_{\text{loss,ini}}} = \frac{\lfloor \gamma \rfloor}{\gamma} \tag{14}$$

The parameter Ψ as a function of γ is depicted in Fig. 4. Note that when γ is an integer, even at small values, theoretically the losses are completely eliminated. However, this only happens at very precise points. If γ suffers a slightest variation, the improvement Ψ will drop significantly. An average value can be computed with an approximation of the floor function $\lfloor \cdot \rfloor$, i.e. $\lfloor x \rfloor = x - \frac{1}{2} + \frac{1}{\pi} \sum_{k=1}^{\infty} \frac{1}{k} \sin(2\pi k x) \simeq x - \frac{1}{2}$. By substitution of γ, (14) ends up as

$$\Psi \simeq 1 - \frac{\Delta t_{\text{d,min}}}{2 t_{\text{d,ini}}} \tag{15}$$

If (9) is replaced in (15) it is possible to predict the amount of power losses that will be eliminated by a duty cycle minimizing algorithm, running in a controller with defined resources. Naturally, the loss elimination is closer to 100 % as the resolution of the ADC and timer increase. Fig. 5 illustrates the possible improvements attainable under a realist scenario.

3. IMPLEMENTATION

The hardware implementation consists of a synchronous buck converter with input-to-output voltage 12-to-1.8 V and maximum current of 5 A (9 W peak power). A fixed load of 0.5 Ω was used in the experiments. For the control and dead-time algorithm implementation, an XMC4200 microcontroller unit was adopted, featuring both low- and high-resolution PWM generation peripherals – the low resolution has a time step of 8.3 ns and high resolution has a time step of 150 ps. These features allow for a comparison between two different timer resolutions, as well as their influence in the power efficiency optimization to be performed. A duty-cycle minimizing algorithm was designed in the microcontroller. Fig. 6 shows the prototype boards used for the experimentation purpose.

3.1. Output voltage control law

The control loop that regulates the output voltage is not only essential to keep the converter operating within the desired set point, but also because the dead optimization algorithm depends on the minimization of the duty cycle,

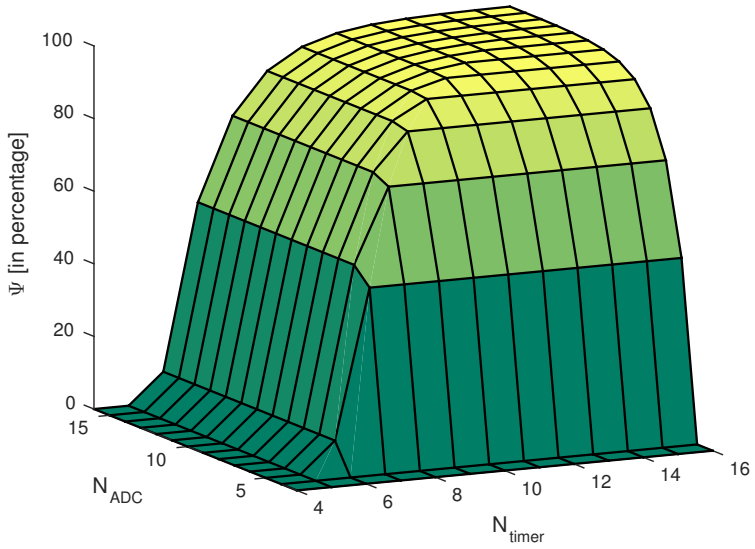


Figure 5. Dependency of the efficiency improvement factor Ψ with ADC and timer resolutions for $t_{\text{d,ini}} = 400\,\text{ns}$, $V_{\text{in}} = 12\,\text{V}$, $V_D = 0.8\,\text{V}$, $V_{\text{ref}} = 3.3\,\text{V}$ and $T_s = 1/320\,\text{kHz}$.

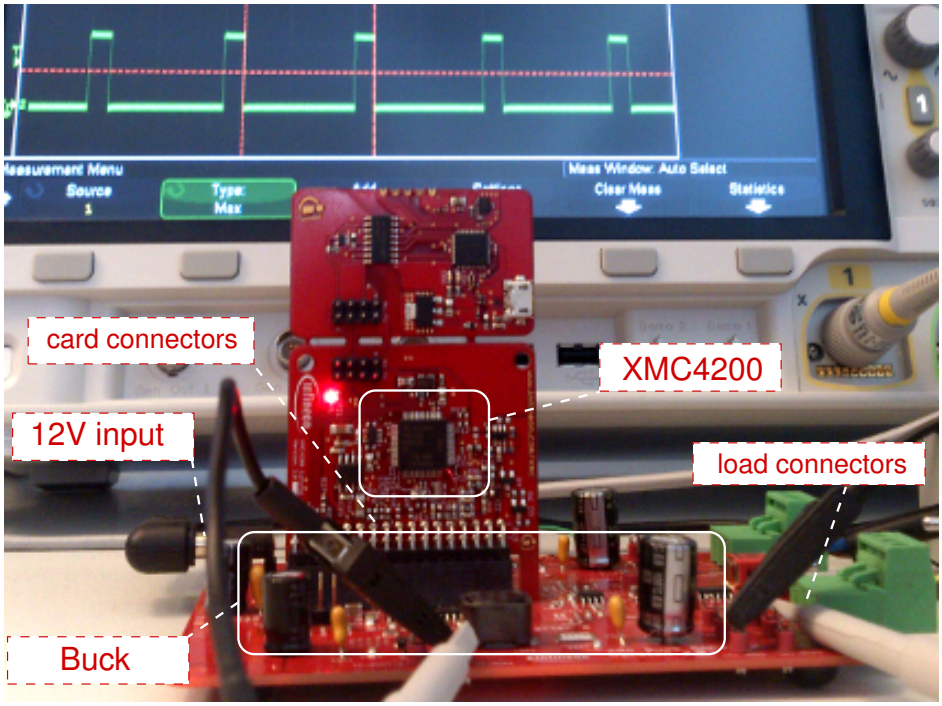


Figure 6. Buck converter and XMC prototype boards.

which is defined by this loop. Therefore, the performance of the output voltage control law, namely the settling speed and the resolution of the duty-cycle value, is reflected directly on the dead-time optimization algorithm.

Firstly, the ADC measures the output voltage and converts it into a 12-bit value. This is fed to a PI controller that outputs a new duty cycle, a decimal value. The duty cycle is then written to the registers, with possible loss of precision, depending on the timer resolution. This loop is executed every 20 μs. In each iteration, the average duty cycle $D[n]$ is calculated using an exponential moving average filter

$$D[n] = D[n-1] + \frac{1}{M} \cdot \big(d[n] - D[n-1]\big) \tag{16}$$

where $d[n]$ is the current duty-cycle value and M is a weighting factor given to the most recent samples – a large

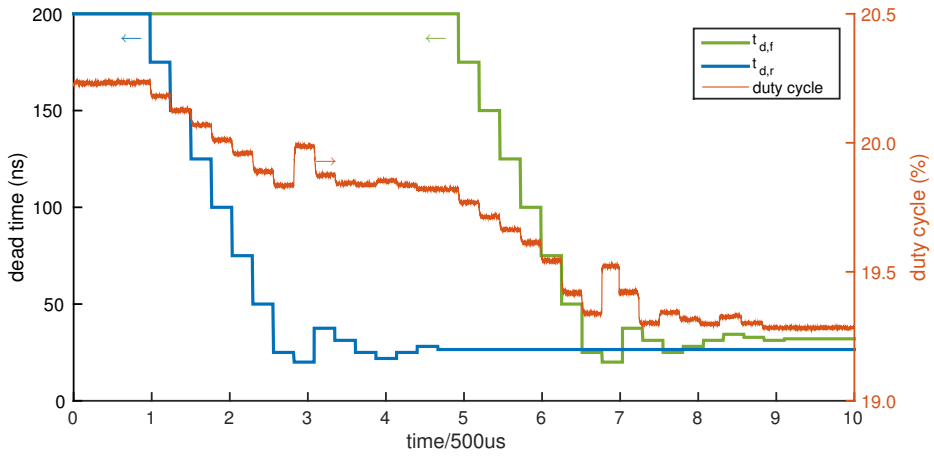


Figure 7. The results of the dead time optimization algorithm, running at slow speed.

M means a smoother but slower filtering, while a small value implies a noisier but faster response [13]. In the next subsection, the usefulness of this value will become clearer.

3.2. Dead-time optimization algorithm

The dead-time optimization algorithm should only be executed when a change in duty cycle is detected, because for a certain load there is only one optimal dead time ($t_{\mathrm{d,opt}}$). This load change is indicated by a variation in the average duty cycle. When the transient stops, the algorithm is triggered and the optimization can take place.

The algorithm is executed a total of two times, i.e. one for the rising edge dead time and one for the falling-edge dead time. The dead time is initially set to 200 ns and is decreased with a step Δt_{d}. In every iteration, a delay allows the duty cycle to settle after the dead-time variation. Then, the gradient is calculated and compared to determine in which region the current dead time is, i.e.

$$\mathrm{sign}(\Delta D) = \mathrm{sign}(\Delta t_{\mathrm{d}}) \quad \Rightarrow \quad t_{\mathrm{d}} < t_{\mathrm{d,opt}} \quad \Rightarrow \text{ diode conduction} \tag{17}$$

$$\mathrm{sign}(\Delta D) \neq \mathrm{sign}(\Delta t_{\mathrm{d}}) \quad \Rightarrow \quad t_{\mathrm{d}} > t_{\mathrm{d,opt}} \quad \Rightarrow \text{ shoot-through region} \tag{18}$$

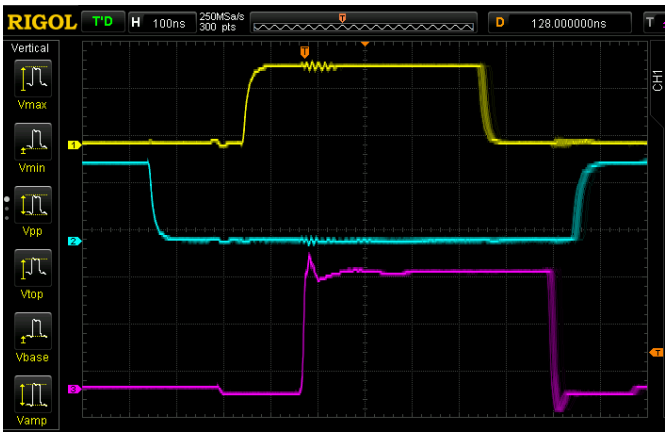
When the border between regions is crossed, a finer search is initiated by inverting the direction and decreasing the dead-time step. This is repeated until the stop condition $\Delta D < \varepsilon$ is fulfilled, where ε is related to the minimum duty-cycle variation imposed by hardware limits early addressed. For protection purposes, despite of the existence of current limiting circuitry, a minimum dead time constrain is included in the algorithm to avoid too high currents in the shoot-through region.

3.3. Results

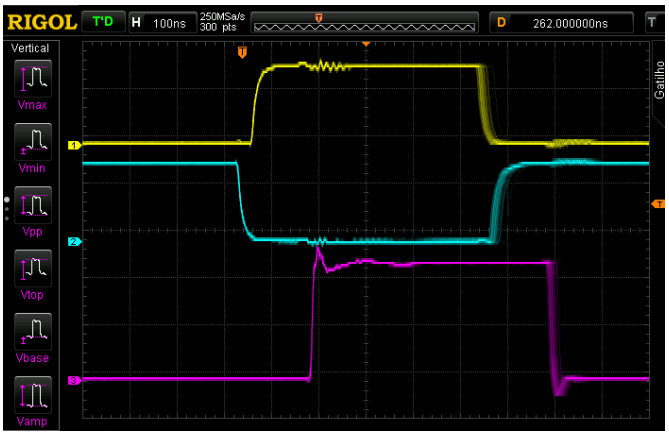
In order to obtain the data from the microcontroller and illustrate the duty-cycle minimization algorithm running, a first version has been employed at slow-speed operation. Fig. 7 shows the evolution of the duty-cycle optimization and respective rising and falling edge dead times. The duty cycle decreases $\sim$1 %, while both dead times start from 200 ns and converge to around $t_{\mathrm{d,r}} = 26.5$ ns and $t_{\mathrm{d,f}} = 32.0$ ns. First $t_{\mathrm{d,r}}$ is processed and only then $t_{\mathrm{d,f}}$ is optimized. It can be noticed that the duty-cycle peaks, which indicate the instants when the algorithm enters the short circuit region, are small and do not pose risk to the hardware.

The algorithm was then tested at $1/T_s = 320$ kHz with two different resolutions in the PWM, a low resolution of 8 bits and 12.5 ns, and the high resolution of 14.3 bits and 150 ps. The same ADC has been used in both cases (12 bits and $V_{\mathrm{ref}} = 3.3$ V). In terms of resources, referring to Fig. 3, the high resolution is closer to a null φ, i.e. $\varphi \simeq 3.84 \times 10^{-3}$ and $\varphi \simeq -1.76 \times 10^{-5}$, respectively for low and high resolutions. The optimum value achieved for low-resolution dead time is 25 ns, both for $t_{\mathrm{d,r}}$ and $t_{\mathrm{d,f}}$. An equal value for the two cases denotes the timer limitation, because of a positive valued φ. On the other hand, in the high resolution optimization the dead times converge to different values, even though superior to the low resolution case.

The initial dead time is set at 200 ns, which is about 80 and 20 times the turn-on and turn-off times of the power switches, respectively. In these conditions the losses are 368.6 mW on the body diode. Fig. 8 depicts prototype measurements with and without the optimization procedure. It is possible to observe the body diode conduction



(a)



(b)

Figure 8. Control switch (yellow, 1), synchronous switch (cyan, 2) and switching node voltage (magenta, 3) – (a) fixed dead time of 200 ns and (b) with the optimization algorithm.

(Fig. 8a), i.e. the negative voltage drops close to the switching node transitions, which is completely eliminated with dead time optimization (Fig. 8b). Table 1 summarizes the results that were obtained for the two versions. The measurement of the power dissipation at the body diode eliminated by the algorithm ($P_{\text{elim,measure}}$) has been predicted with relative accuracy ($P_{\text{elim,theory}}$) with our simplistic analysis. The absolute and incremental efficiency of the converter ($\eta_{\text{converter}}$ and $\Delta\eta_{\text{converter}}$, respectively) has been measured as well as the impact on overall efficiency of the converter and microcontroller (Δ_{system}), denoting also significant improvements. Lastly, the temperatures were also measured for both the synchronous and control switch. On the fixed dead time implementation, at 200 ns, the package ambient temperatures were 43.5 °C and 42.5 °C, whereas at optimal dead time, when the losses are minimal, the temperatures of the MOSFET packages were the lowest, at 40 and 41 °C in low and high resolution implementations, respectively. When entering the short circuit region, both temperatures increased about 4 °C.

4. CONCLUSION

This work presents a study on the influence of timer and ADC resolutions in the dead-time optimization of buck converters. An analysis of body diode losses and respective minimization by means of digital control has been presented. This analysis includes the hardware limitations of a sensorless algorithm for minimizing the duty-cycle of digital PWM signals. In spite of the low complexity and reduced computation requirements of the similar sensorless algorithms, most solutions make use of ICs or FPGAs for the implementation of the digital control. The present approach is completely implemented in a microcontroller unit. The designed algorithm demonstrated about 5 % efficiency improvement over a fixed dead-time solution and 1 % improvements from using low- to high-resolution PWM signals. These results are significant and may influence the decision of choosing a controller with this kind of resources for the design of a power supply.

Table 1. Experimental results using low- and high-resolution PWM.

Parameter	Resolution		Units
	low	high	
N_{ADC}	12	12	bits
N_{timer}	8	14.3	bits
$t_{\text{d,r,opt}}$	25	27.5	ns
$t_{\text{d,f,opt}}$	25	31.3	ns
$P_{\text{elim,theory}}$	76.5	99.6	%
$P_{\text{elim,measure}}$	72	98.6	%
$\Delta\eta_{\text{system}}$	2.5	3.6	%
$\Delta\eta_{\text{converter}}$	3.6	4.9	%
$\eta_{\text{converter}}$	95.1	96.1	%

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