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Development of Digital Controller for DC-DC Buck Converter

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ABSTRACT

This paper presents a design & implementation of 3P3Z (3-pole 3-zero) digital controller based on DSC (Digital Signal Controller) for low voltage synchronous Buck Converter. The proposed control involves one voltage control loop. Analog Type-3 controller is designed for Buck Converter using standard frequency response techniques.Type-3 analog controller transforms to 3P3Z controller in discrete domain.Matlab/Simulink model of the Buck Converter with digital controller is developed. Simualtion results for steady state response and load transient response is tested using the model.

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1. INTRODUCTION

The objective of a control system is to make a physical system behave in a useful fashion, causing its output to track a desired reference input even in the presence of noise, modeling error & disturbances. In the control system one of the main components is the controller, which generates the appropriate control signal for the physical system performance. Type-3 controller is one of the most common types of feedback controllers that are used in DC-DC converters [1].

Traditionally regulation of the output voltage of DC-DC converter has been achieved through the use of analog control techniques. Analog control system operates in real time and can have a high bandwidth. In addition the voltage regulation for an analog system is theoretically infinite. However an analog system is usually composed of discrete hardware that must be modified to change controller gains or algorithms. In addition the implementation of advanced control algorithms require an excessive number of components whereas the complexity of a digital control system is contained mostly in software. Digital processors also have the advantage of being less susceptible to ageing & environmental or parameter variations.

The implementation of 3P3Z (3-pole3-zero) digital controller using DSC (Digital Signal Controller) requires only one input channel with analog to digital conversion capabilities if voltage mode control is used. This input channel captures the signal of signal of output voltage. Further two PWM outputs are needed for switch control. These requirements are available in many low cost digital devices and hence the true challenge is to accomplish the control aims with an acceptable processing time. Thus it is worth to point out that information losses caused by quantization, output resolution, acquisition times & processing times can be accentuated by limitations in a low cost digital implementation.

This paper presents a simple methodology for design and implementation of digital controller for DC-DC Converter using Matlab/Simulink. The design approach starts with modelling and simulation of the controlled system of synchronous buck converter in Matlab/Simulink. The structure in use implements Type-

3 control laws in discrete time system. So the controller is formulated in the continuous-time domain and controller equations are discretized to implement the controller as computational algorithm.

2. CLOSED LOOP CONTROL SYSTEM

Figure 1 shows the block diagram of a typical digital control system. A digital system operates on the samples of the sensed plant output. ADC is for sampling output voltage, DPWM is for generating driver signal according to corresponding control laws. The compensator is for generating the control signal y(n) by compensating the error signal e(n). The input & output of a digital controller are related by a linear difference equation such as:

$$\sum_{i=0}^{k} b_i y((n-i)T_s) = \sum_{j=0}^{m} a_j e((n-j)T_s) \quad (1)$$

$$e(nT_s) = V_{ref} - V_{out}(nT_s), \quad (2)$$

T_s is the sampling frequency.

In the design of digital controller, two techniques are generally applied. The first is digital redesign, where any zero-order hold & samplers in the control loop & do a preliminary design in s domain. The design is then converted to a discrete time by same approximation technique to yield a discrete time compensator. The second method is to convert the continuous time plant with zero-order hold & samplers to a discrete plant using some approximation technique. Once the discrete time approximation of the plant is available, the discrete time compensator is designed directly in z domain. Digital redesign approach is used here to design the controller for Buck Converter.

3. 3P3Z CONTROL ALGORITHM

For digital 3P3Z controller with sampling period T_s, the following digital 3P3Z control algorithm can be obtained by transforming the type-3 controller to discrete time using bilinear transformation [2]. The respective digital compensator is given by:

$$G_c(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2} + A_3 z^{-3}}{1 + B_1 z^{-1} + B_2 z^{-2} + B_3 z^{-3}} \quad (3)$$

Consequently the discrete time-domain equation for the output of the compensator is obtained as:

$$y(n) = -B_3 y(n-3) - B_2 y(n-2) - B_1 y(n-1) + A_3 e(n-3) + A_2 e(n-2) + A_1 e(n-1) + A_0 e(n) \quad (4)$$

Where e (n-3),e(n-2).e(n-1),e(n) are the error signals of the n^{th}, $(n-1)^{th}$, $(n-2)^{th}$& $(n-3)^{th}$ sample respectively. y(n-3),y(n-2),y(n-1) is the duty cycle command stored from previous cycles, y(n) is the current duty cycle command which is the controller output for n^{th} sample. For the dsPIC DSC implementation of architecture, the controller co-efficient A_0,A_1, A_2, A_3, B_1, B_2, B_3 uses fixed values & are determined offline from the well-designed controller to be discussed in next section

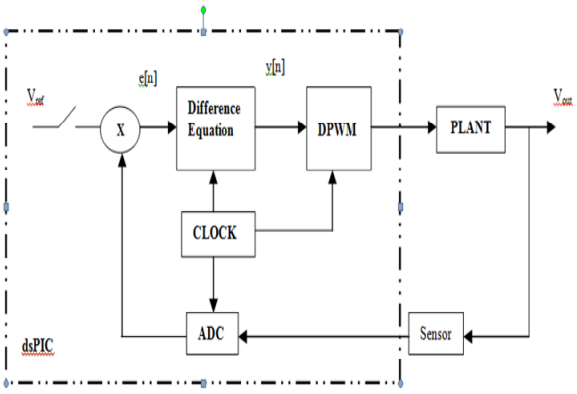

Figure 1. Typical digital control system block diagram

4. 3P3Z CONTROLLER DESIGN

To design the 3P3Z controller for synchronous buck converter; a linearized model of the plant is developed to obtain the plant model G_{sys}.

4.1. Power stage model $G_{vd}(s)$

For the general buck converter, the small signal control to output transfer function $G_{vd}(s)$ is given by [3].

$$G_{vd}(s) = \frac{V_i(sr_cC+1)}{\left[s^2LC\left(\frac{R+r_c}{R}\right)+s\left(r_cC\left(\frac{R+r_c}{R}\right)+\frac{L}{R}+r_LC\right)+\frac{R+r_L}{R}\right]} \quad (5)$$

The following parameters are considered for the model.
V_i=9V, R=5Ω, V_0=5V±0.5%, r_c=25mΩ, r_L=38mΩ, L=10µH, C=300µF.Switching frequency $f_s = 400KHz$ and sampling frequency $f_{sampl} = 133KHz$. With the specified parameter $G_{vd}(s)$ is given by:

$$G_{vd} = \frac{9(1+7.5\times10^{-5}s)}{10\times10^{-6}s^2+2.1\times10^{-5}s+1} \quad (6)$$

4.2. Controller model $G_{cs}(s)$

The system transfer function $G_{vd}(s)$ has two complex conjugate poles and one zero introduced by capacitor esr. A type 3 contoller is usually required to compensate the system.

$$G_c(s) = G_{co}\left(\frac{1+\frac{s}{\omega_{z1}}}{s}\right)\left(\frac{1+\frac{s}{\omega_{z2}}}{1+\frac{s}{\omega_{p2}}}\right)\left(\frac{1}{1+\frac{s}{\omega_{p1}}}\right) \quad (7)$$

Equation (7) shows a type3 controller, it's a combination of PI compensator, Lead compensator and an extra pole ω_{p1} which is used to compensate capacitor esr zero.A type 3 controller has the advantages of a lead and lag compensator. At low frequencies, the compensator integrates the error signal, leading to very high low frequency loop gain and accurate regulation of output voltage. At high frequency the compensator introduces phase lead into the loop gain.

4.2.1. Controller design

First design step for a digital controller is selecting the appropriate sampling frequency. For low switching frequencies sampling frequency is same as switching frequencies, but as we go for high switching frequencies it may not be possible to sample the output every PWM cycle because of processing time constraints. In this case sampling frequency is taken as 1/3rd of switching frequency which is 133 KHz. This ensures that duty is updated once in every 3 PWM cycles. The plant transfer function given in equation (6) is used to design a Type-3 controller. The following design criteria must satisfy.

- The gain at low frequency should be high enough to minimize the steady state error. The cross over frequency of the closed loop system should be lower than one third of the sampling frequency [4].
- The phase margin of the compensated system should be above 45^0[5].

Next step is to compensate the capacitor esr zero by placing a pole exactly on the zero. Capacitor esr zero enhances high frequency gain and it needs to be compensated. Figure (2a) shows the bode plot of capacitor esr compensated system and Figure (2b) shows the step response. Table 1 shows the comparison between obtained specification and the desired specification.

Time domain specifications like overshoot, settling time and steady state error are dependent on closed loop damping factor Ɛ. Equation (8) shows the relation between phase margin(ϕ) and closed loop damping factor[3] where $Q = \frac{1}{2\varepsilon}$.

$$\phi = \tan^{-1}\sqrt{\frac{1+\sqrt{1+4Q^2}}{2Q^2}} \quad (8)$$

Overshoot is a critical design parameter, for 10% overshoot damping factor Ɛ=0.6, thus the required phase margin is 59^0. Here the phase margin is fixed to 70^0 to obtain an overshoot less than 10%. Once the phase margin is fixed next step is select the gain cross over frequency (f_{gc}). it must be way below the Nyquist rate. Typically between 1/6th to 1/10th of sampling frequency, here f_{gc} is taken as 15 KHz.

4.2.2. Design of lead compensator.

From the phase plot in Figure 2a it can be observed that phase at 15KHz is -176^0. Once the gain cross over frequcny is fixed to 15KHz the phase margin will come down to 4^0 from 10^0.The required phase margin is 70^0 plus a margin of 5^0 to compensate any lag that occur in later stage of design. Thus the lead compensator must provide a phase lead of $\Theta = 70^0 + 5^0 - 4^0 = 71^0$ at frequency $f = 15KHz$. Zero of lead compensator must be placed at f_{z1} and pole at f_{p1}.The pole and zero position can be calculated using equation (9) and (10), where $\Theta = 71^0$.

$$f_{z1} = f_{gc}\sqrt{\frac{1-\sin\theta}{1+\sin\theta}} \quad (9)$$

$$f_{p1} = f_{gc}\sqrt{\frac{1+\sin\theta}{1-\sin\theta}} \quad (10)$$

Table 1

Parameter	Capacitor esr compensated sytem specification	Desired Specifaction
Gain over frequency (f_{cr})	7.3KHz	15KHz
Phase Margin (ϕ)	10.3^0	70^0
Settling time	1.1ms	600µs
Final value	4.22V	5V
Overshoot	78.8%	<10%

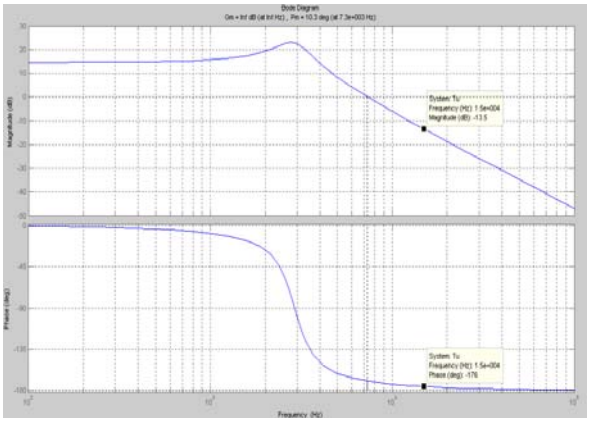

Figure 2a. Bode plot capacitor esr compensated system

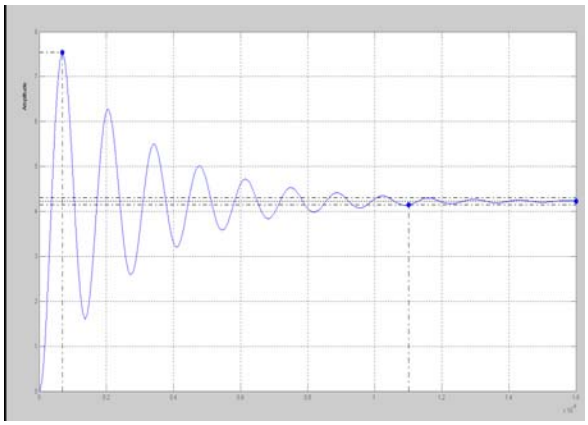

Figure 2b. Step response of capacitor esr compensated system

The zero is placed at 2.9 KHz and pole at 77.2 KHz. The lead compensator transfer function thus obtained is shown in equation (11).

$$G_{lead}(s) = 0.91956\left(\frac{1+\frac{s}{15815}}{1+\frac{s}{484817}}\right) \quad (11)$$

The frequency response and step response of the system after adding the lead compensator is depicted in Figure (3a) and (3b) respectively. Gain cross over frequcency and phase margin is as per the design requirements. Step response shows that overshoot has come down to 21% and settling time has improved to 133µs. From the frequency response it seen that low frequcny gain is only 14dB. For good rejection of low frequency noise and better regulation the low frequency gain must be 40dB or greater.

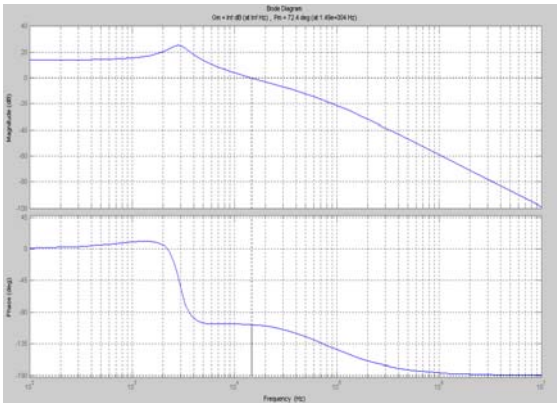

Figure 3a. Frequency response with lead compensator

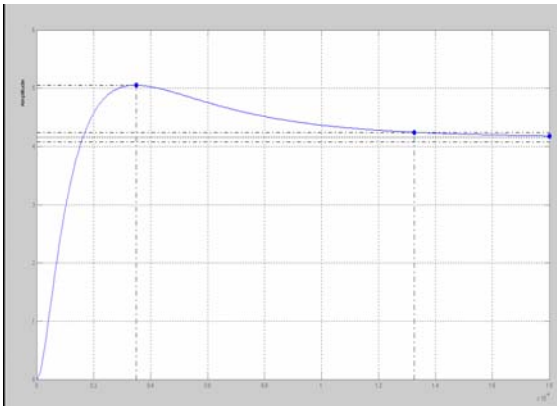

Figure 3b. Step response woth lead compensator

Low frequency gain can be improved by adding a PI compensator.While adding a PI compensator two aspects needs to be taken care, the cross over frequency f_{gc}must not shift from 15KHz, the phase margin must not come below 70^0as PI will introduce phase lag. The zero of PI compensator is arbitarly taken as $f_{z1} = \frac{f_{gc}}{10}$. Equation (12) shows the PI compensator

$$G_{pi}(s) = 4000\left(\frac{1+\frac{s}{42412}}{s}\right) \quad (12)$$

By combining the PI and lead compensator type 3 controller transfer function is given by equation (13)

$$G_{c3}(s) = \frac{4149\left(1+\frac{s}{42412}\right)\left(1+\frac{s}{15815}\right)}{s\left(1+\frac{s}{484817}\right)\left(1+\frac{s}{15815}\right)} \quad (13)$$

The frequency response and step response for the designed type-3 controller is shown in Figure 4a and 4b respectively. The system paremeters of the compensated system and the desired specification is depicted in Table-2. The compensated system meets the desired specifications.

Once the s-domain transfer function is available it can be converted to z-domain using bilinear transformation. The discrete time transfer function is given by equation (14). A 3pole-2zero transfer function in s-domain transfers to 3-pole-3-zero in the z-domain which is known as 3p3z controller.

$$G_c(z) = \frac{0.998 - 1.808z^{-1} - 1.081z^{-2} + 1.818z^{-3}}{1 - 1.041z^{-1} - 0.05604z^{-2} + 0.09683z^{-3}} \quad (14)$$

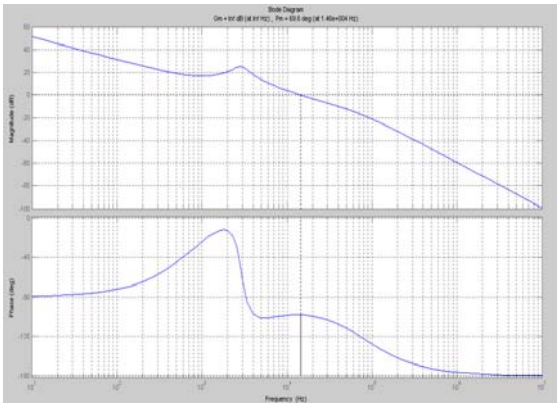

Figure 4a. Bode Plot for Buck converter with Type-3 controller

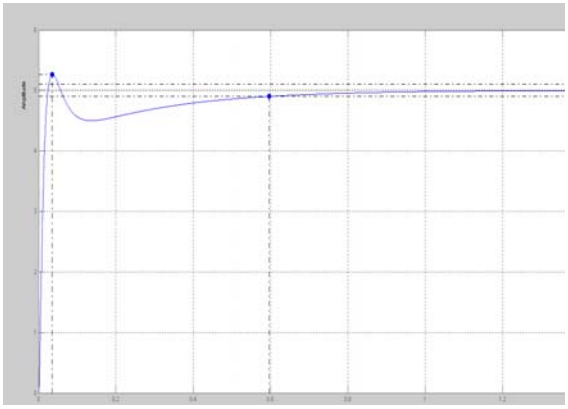

Figure 4b. Step response for Buck Converter type-3 controller

Table-2

Parameter	Compensated system specification	Desired specification
Gain over frequency (f_{co})	14.6 KHz	15KHz
Phase Margin (ϕ)	69.6^0	70^0
Settling time	596µs	600µs
Final value	5V	5V
Overshoot	5.25%	<10%

5. SIMULATION AND RESULTS

This section describes the control circuit and the power stage and how the overall system can be modelled using Simulink. After that it present and discusses the obtained results.

5.1. Digital controller model

Figure 5 shows the Simulink model of buck converter in steady state. The model is developed using steady state inductor voltage equation and capacitor current equation. Closed loop buck converter with digital controller is implemented as shown in Figure 6. Usually a Digital Signal Controller (DSC) is used digital controller need to to be realized in hardware. A DSC will have in built ADC to digitize the output from the system, a DSP engine to implement the control law and DPWM block to generate the desired PWM with duty controlled as per control law [6]. Figure 6 shows how the entire sytem can be modelled in Simulink. This model enables us to verify the controller performance before going for actual hardware testing.

The specification of dsPIC33F DSC from Microchip Technology is taken to model the controller. The output voltage of the buck converter is scaled down to 3V by the sensor network. This is required as the ADC voltage range is 0 to 3.3V this is because Digital Signal Controllers typically use 3.3V supply The 10-bit ADC is modelled using zero-order hold, A/D quantizer, A/D limiter blocks.3P3Z controller is implemented with transfer function block. The 16-bit DPWM module is modelled using DPWM quantizer and DPWM limiter blocks. DPWM limiter restricts the duty between 75% and 10% preventing fully on and fully off condition of the Mosfet. The transport delay block models the time between sampling the error signal and updating the duty cycle command which is approximately 3µs. A pulsating load is incorporated to test the load transient behavior.

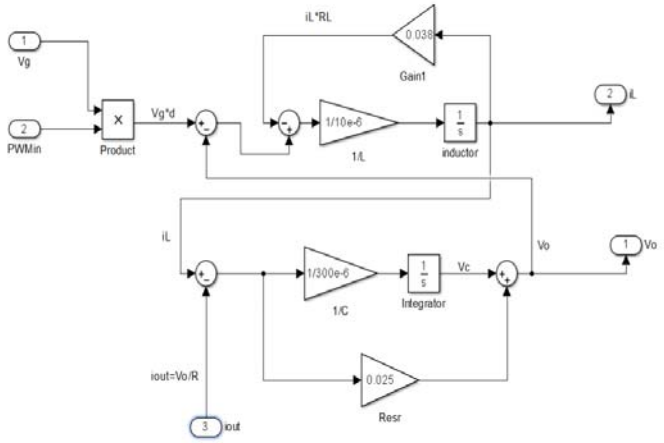

Figure 5. Steady state model of Buck Converter

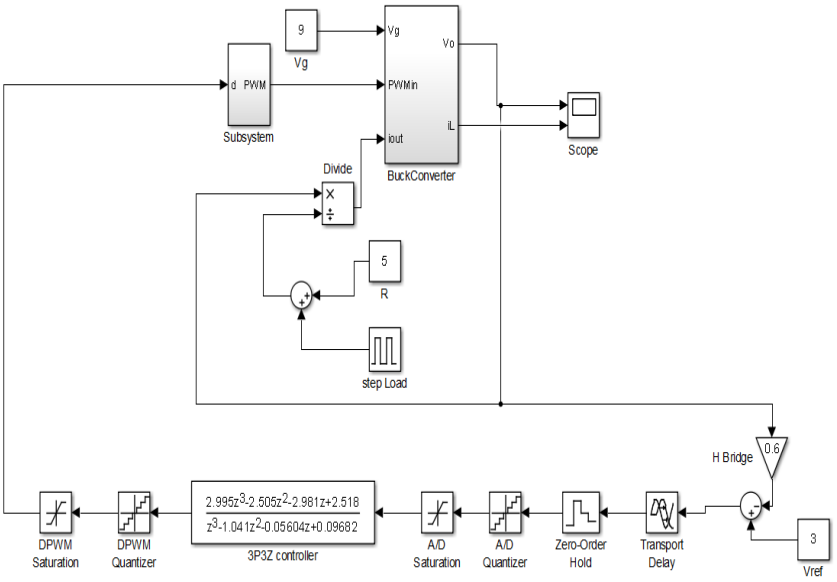

Figure 6.Closed loop model of Buck Converter

5.2. Simulation Results

The controller effevtiveness is tested using a load transient. When there is sudden change in load the ouput will have a have an overshoot or voltage droop. The sytem must then revcover smoothly to its steady sate value [7]. The recovery time is dependent on the bandwidth of the controller which is inverse of f_{GC} which is around 66µs. Figure 6 shows the load transient response obtained using Simulink model for the load current changes from 0.1A to 1A and 1A to 0.1A respectively. It can be observed that the load transient take about 30µs to complete which is within the expected value 66µs.

The start-up transient is shown in Figure 8. It is observed that output voltage settles to 5V in around 800µs. A 13% output voltage overshoot is present which can be reduced by incorporating soft start. Simulation results are favorable for actual hardware testing.

The simulation results show that the controller is efficient. The ouput voltage is well regulated at 5V. The response is fast when subjected to disturtbance.

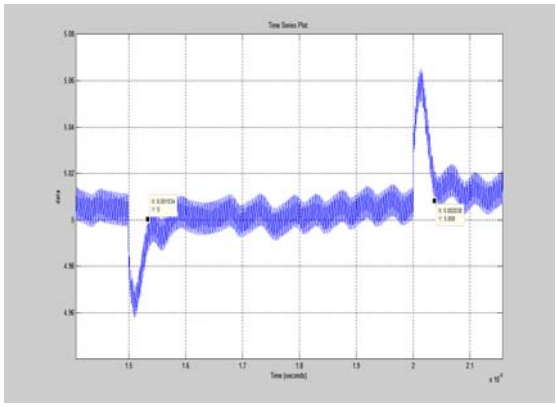

Figure 7. Load transient response obtained with Simulink model

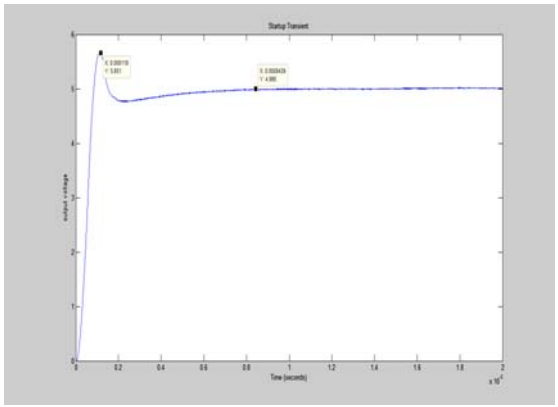

Figure 8. Start-up transient obtained with Simulink model

6. CONCLUSIONS

This paper describes complete design and implementattion of a digital controller for buck converter. A design example based on a synchronous buck converter operating at the switching frequency of 400 KHz is presented. The controller design is based on direct digital design approach and standard frequency domain design techniques. Simulation results are shown to validate the design approach.The developed Simulink model can be used to model any DSC as the specifications change with the vendors. Further work needs to be done to implement the converter logic using a digital signal controller and test a prototype Buck Converter with same specification.

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