International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 6, No. 4, December 2015, pp. 906~918
ISSN: 2088-8694

Implementation of Space Vector Modulator for Cascaded H-Bridge Multilevel Inverters

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Article Info

Article history:

Received Jul 26, 2015
Revised Oct 30, 2015
Accepted Nov 16, 2015

Keyword:

Cascaded h-bridge
CHMI
Multilevel inverter
Space vector modulation
Three levels inverter

ABSTRACT

The Space Vector Modulation (SVM) technique has gained wide acceptance for many AC drive applications, due to a higher DC bus voltage utilization (higher output voltage when compared with the SPWM), lower harmonic distortions and easy digital realization. In recent years, the SVM technique was extensively adopted in multilevel inverters since it offers greater numbers of switching vectors for obtaining further improvements of AC drive performances. However, the use of multilevel inverters associated with SVM increases the complexity of control algorithm (or computational burden), in obtaining proper switching sequences and vectors. The complexity of SVM computation causes a microcontroller or digital signal processor (DSP) to execute the computation at a larger sampling time. This consequently may produce errors in computation and hence degrades the control performances of AC motor drives. This paper presents a developement of SVM modulator for three-level Cascaded H-Bridge Multilevel Inverter (CHMI) using a hybrid controller approach, i.e. with combination between the DS1104 Controller Board and FPGA. In such way, the computational burden can be minimized as the SVM tasks are distributed into two parts, in which every part is executed by a single controller. This allows the generation of switching gates performed by FPGA at the minimum sampling time $DT_2 = 540\,ns$ to obtain precise desired output voltages, as can be verified via simulation and experimental results.

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1. INTRODUCTION

The Space Vector PWM (or known as SVM) is one of the most popular PWM techniques because of a higher output voltage and flexible to be implemented in advanced vector control of AC motors [1-3]. Technically, it was reported that the SVM is the most favorable modulation technique among PWM scheme due to several advantages, higher output voltage, reducing harmonic ripple and able to optimized the switching sequence [4]. Besides that, this modulation scheme also offer in optimizing the used of dc voltage link utilization which means it can increase the ration of output magnitude voltage.

In general, the implementation of SVM involve with the used of DSP board and required sector identification which brings into the formations of rotating space vector diagram. [5]. In the three phase system, there are six fractions in the space vector diagram spinning 360° which each has equally divided by 60°. This space vector diagram is a transformation from a balance of three phase quantities into two phase

system of α-β reference frame [4]. The SVM main operation is to used the nearest three vector recognition of the reference voltage and determined the corresponding on-time using the principles of volt second equivalent [6]

A multilevel inverter offers greater number of voltage vectors as compared to eight vectors for a two-level inverter. Figure 1 illustrates the space vector diagrams for Sector I, in a two-level inverter and three-level inverter. The space vector diagrams can be used to compare the implementation of SVM in two-level and three-level inverters. As compared to two-level space vector diagram, the sector in three-level inverter is divided into four identical smaller triangles (i.e. Δ_0, Δ_1, Δ_2 and Δ_3). To reduce THD (or dv/dt) and switching losses in multilevel inverter (i.e. three-level), it is necessary to switching vectors which are the nearest to the reference vector $\bar{v}_s^*$. Hence, three-level SVM switch the vectors $\bar{v}_2$, $\bar{v}_7$ and $\bar{v}_{14}$ for a given reference vector.

The calculation of on-duration in multilevel SVM is quite complicated and different for various triangles due to small triangles in the space vector diagram of three-level inverter in Fig.1 do not exactly imitate the geometry of a sector of two-level inverter. In two-level SVM, the calculation of on-duration is straightforward which is valid for every sector. However, the three-level SVM needs to modify the reference vector with new origin point to apply the two-level based SVM for calculating on-duration. As shown by Figure 1 (b), the modified reference vector $\bar{v}_s^{*\prime}$ with vector $\bar{v}_2$ as origin point is determined such that the calculation of on-duration is similar to that of two-level based SVM. The calculation becomes complicated if the reference voltage vector $\bar{v}_s^*$ lies in triangle Δ_2, where the orientation of triangle is different among others; as can be seen the triangles Δ_0, Δ_1 and Δ_3 have the same orientation with a single triangle or Sector I in two-level SVM, as shown in Fig.1. The complexity increases as number of level of inverter becomes higher, e.g. in five-level inverter, there are six triangles among sixteen triangles, that have different orientation.

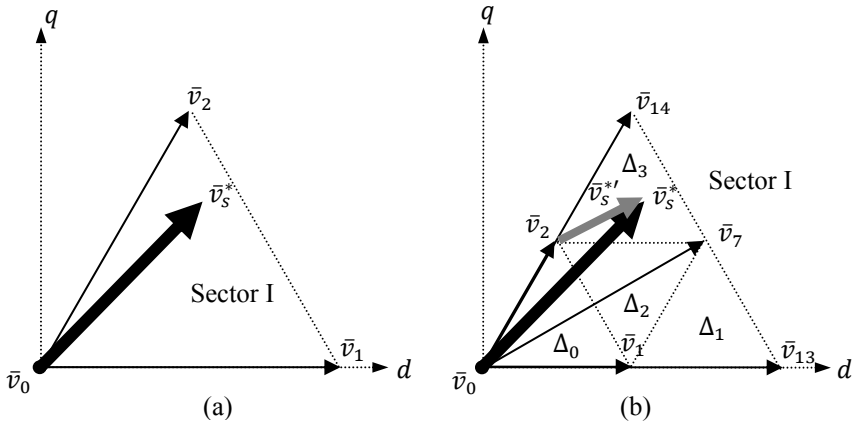

Figure 1. Comparison Between (a) Two-Level Space Vector Diagram and (b) Three-Level Space Vector Diagram, e.g. for Sector I.

The implementation of SVM for multilevel inverters require some important parts which are as follows; (1) detection of sector si, (2) detection of triangle Δ_j, (3) calculation of on-duration for switching the nearest vectors, and (4) determination the switching sequence for every switching period.

As found in literature, there are two common methods to calculate the on-durations. The first method is to detect the triangle and solve three simultaneous equations of the triangle to determine the on-times as suggested in [7]. The second method is to detect the triangle and use particular on-duration equations stored in a lookup table for this triangle, as proposed in [8]. Both of these methods however require complex computations as the number of level increases.

Alternatively, the calculation of on-duration can be obtained using general algorithms [9] and [10]. Specifically, [9] uses a Euclidean vector system with several matrix transformation, provided that it does not provide a systematic approach for real time SVM implementation. On the other way, [10] calculated on-duration and obtained switching states by means of coordinate system, where the axes are 60 degrees apart. However, the 60 degrees transformation leads to the complexity since the voltage reference is commonly defined in the orthogonal coordinate system.

Recently, a simple SVM algorithm for multilevel inverters based on standard two-level SVM was proposed in [11]. The two-level based SVM concept is initiated by [12-14], however, the calculation of on-duration is based on origin modification and 60 degrees coordinate transformation, which cannot be extended in implementing SVM for higher levels, i.e. L greater than three. Unlike the former methods, the

implementation of SVM proposed in [11] that includes the detection of sector and triangle, and calculation of on-duration were derived geometrically and systematically which suitable for any level of inverter.

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2. TOPOLOGY OF THREE-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

The smallest number of level for Cascaded H-bridge Multilevel Inverter (CHMI) is three levels. Figure 2 shows a topology circuit of 3-level CHMI, which consists of three full bridge inverters (or known as H-bridge). Each bridge consists of two legs, 4 power switches, i.e. IGBTs and an identical isolated DC voltage. The isolated DC voltage for three-level CHMI is designated as V_{dc3}. The first leg of each bridge is connected to its phase or winding of a three-phase induction motor, while another leg is shorten as a common point which referred to as a neutral point, N. In any H-bridge inverter, it can produce three states of output voltage, i.e. $+V_{dc3}$, 0 or -V_{dc3}, as given in (1).

$$v_{xn} = (S_{x1} - S_{x2}).V_{dc3} \tag{1}$$

Where S_{x1} and S_{x2} are the respective switching states for the upper switches of the first and second legs of the x-phase H-bridge inverter. Note that the switching of upper and lower switches in the same leg must be complimentary to each other to avoid short circuit conditions.

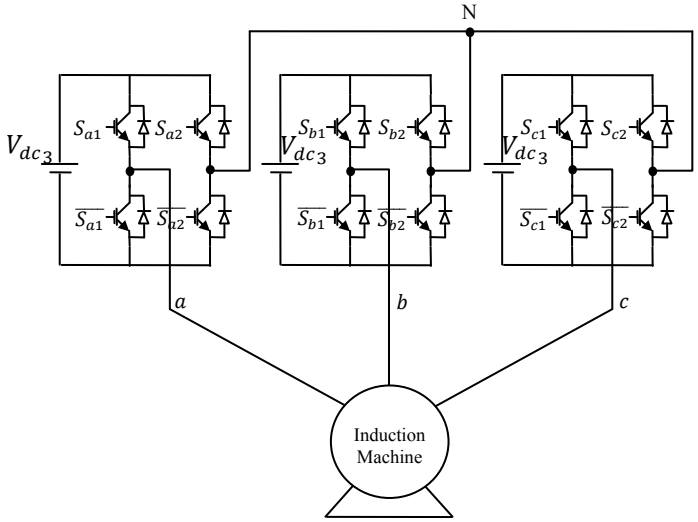

Figure 2. Topology Circuit of Three-Level Cascaded H-Bridge Multilevel Inverter

3. SPACE VECTOR MODULATION

3.1. Mapping Vector

Compare with the two-level inverter basic concept, the three-phase quantities of stator voltage vector can be expressed into a space voltage vector form by substituting the basic algotithm of two levels phase stator voltages with equation (1), the space voltage vector can also be written in terms of switching states and DC link voltage. Then it can be express into d- and q-axis components of stator voltage, as follows:

$$v_{sd} = \frac{V_{DC3}}{3}[2(S_{a1} - S_{a2}) - (S_{b1} - S_{b2}) - (S_{c1} - S_{c2})] \tag{2}$$

$$v_{sq} = \frac{1}{\sqrt{3}}V_{dc3}[(S_{b1} - S_{b2}) - (S_{c1} - S_{c2})] \tag{3}$$

Fig. 3 shows voltage vectors available in the three-level CHMI. All voltage vectors are mapped on the d- and q-axis plane by applying every switching state possibility in (2) and (3). From this figure, the mapping of voltage vectors forms six sectors, where each sector contains four small of triangulars and the voltage vectors can be categorized into four groups as follows: 1) long amplitude of voltage vectors, i.e. $\bar{v}_{13}$, $\bar{v}_{14}$,…, $\bar{v}_{18}$, 2) medium amplitude of voltage vectors, i.e. $\bar{v}_7$, $\bar{v}_8$,…, $\bar{v}_{12}$, 3) short amplitude of voltage vectors i.e. $\bar{v}_1$, $\bar{v}_2$,…, $\bar{v}_6$, and 4) zero voltage vector, i.e. $\bar{v}_0$. It should be noted that each long or medium voltage

vector has only a single of switching states, however, the number of switching states increases as the amplitude of vector reduces toward the origin of the plane.

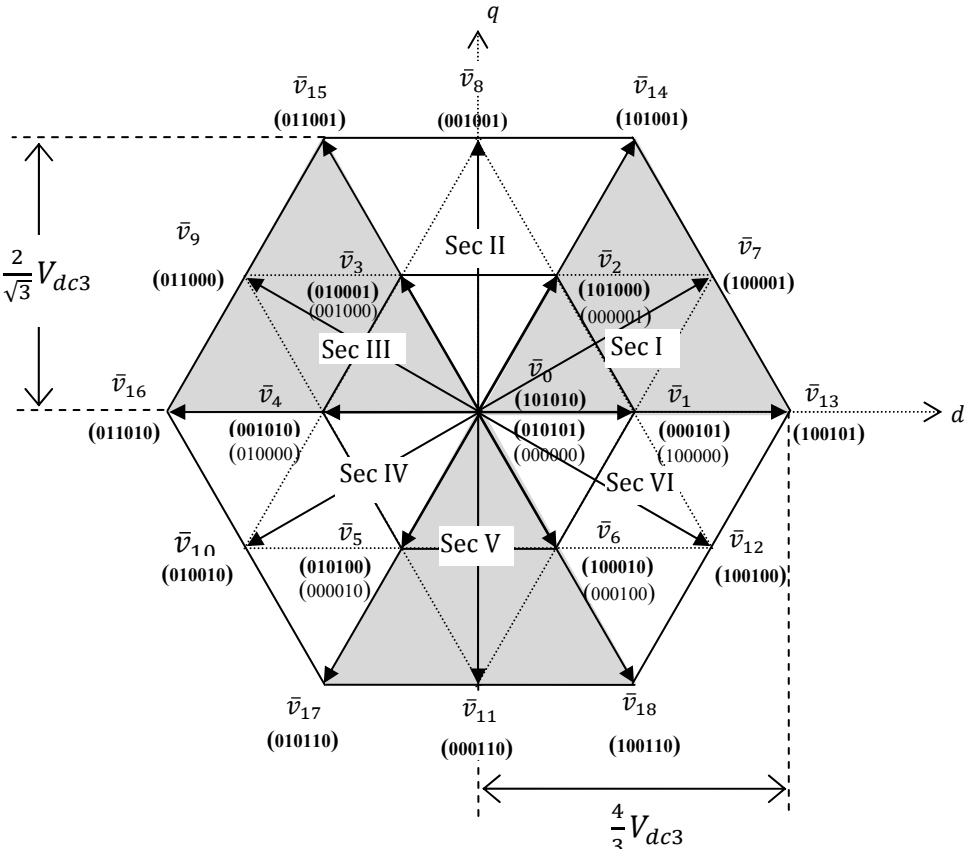

Figure 3. Voltage Vectors in the Three-Level CHMI Obtained in Equantions (2) and (3) for Every Switching State Possibility ($S_{a1}S_{a2}S_{b1}S_{b2}S_{c1}S_{c2}$)

3.2. Determination of Sector and Triangle

From Figure 3, it can be noticed that the mapping of active vectors forms a hexagonal boundary, in which the hexagonal can be equally divided into six sectors. This means the difference between the two angles of adjacent active voltage vectors is 60^0. It should be noted that the space voltage vector can also be expressed into a polar form, as below:

$$\bar{v}_s^* = v_s^* \angle \theta_s \tag{4}$$

Taking into account that the unit of θ_s is expressed in radian which varies between 0 and $\pm\pi$ rad. The involvement of negative value in θ_s variation complicates the calculation. Therefore, a small modification is made using a modulus technique, such that the equivalent variation obtained between 0° and 360°. The following equations need the transformation of θ_s in degrees and the modulus operation to have the positive value variations, i.e. m. The six sectors can be easily determined by substituting the positive variations m into (5), this yields:

$$si = floor\left(\frac{m}{60}\right) + 1 \tag{5}$$

With the increasement number of level, the termination of sector for multilevel need to deals with the existence of small segment of triangles (i.e. Δ_j, where j=0, 1, 2 or 3) inside each sector for calculating on-duration of voltage vectors wihich its similar to the two-level based SVM [11]. In such way, the definition of reference voltage vector is based at which triangle the vector is located, where the calculation of on-duration of voltage vectors in a triangle is treated the same way as the vectors in a sector for two-level based SVM. To obtain Δ_j, at first, the angle within a sector θ_r needs to be obtained using (6).

$$\theta_r = rem(m, 60^0) \quad (6)$$

Then, let the identification of triangle is made by considering the sector at which the reference voltage vector is located. Based on the α- and β-axis plane, the components of reference voltage vector can be written as:

$$v_{s\alpha}^* = v_s^* \cos(\theta_r) \quad (7)$$
$$v_{s\beta}^* = v_s^* \sin(\theta_r) \quad (8)$$

Alternatively, the equivalent voltage vector $\bar{v}_{so}^*$ based on α_o- and β_o-axis plane in a triangle is defined (as illustrated in zoomed images in Figure 4(b) and (c)), hence the components of the vector can be calculated as:

$$\bar{v}_{so}^* = v_{\alpha o}^* + j v_{\beta o}^* \quad (9)$$

From the vector diagrams shown in Figure 4, it can be noticed that the definition of reference voltage vector within a small triangle for triangle Δ_0, Δ_1 and Δ_3 is similar to that defined in Sector I for the case of two-level based SVM. Geometrically, the triangle Δ_j (for j=0, 1 or 3) and the vector components $v_{\alpha o}^*$ and $v_{\beta o}^*$ can be calculated using the following equations [11]:

$$v_{\alpha o}^* = v_{s\alpha}^* - \left(k_1 - \frac{k_2}{2}\right)\frac{2V_{dc3}}{3} \quad (10)$$
$$v_{\beta o}^* = v_{s\beta}^* - k_2 \frac{V_{dc3}}{\sqrt{3}} \quad (11)$$
$$\Delta_j = {k_1}^2 + 2k_2 \quad (12)$$

where k_1 and k_2 are obtained using (13) and (14):

$$k_1 = int\left[\frac{3}{2V_{dc3}}\left(v_{s\alpha}^* + \frac{v_{s\beta}^*}{\sqrt{3}}\right)\right] \quad (13)$$
$$k_2 = int\left[\sqrt{3}\frac{v_{s\beta}^*}{V_{dc3}}\right] \quad (14)$$

On the other hand, the definition of reference voltage vector within a small triangle for triangleΔ_2 is similar to that defined in Sector IV for the case of two-level based SVM. It can be proved geometrically that the triangle Δ_2 and the vector components $v_{\alpha o}^*$ and $v_{\beta o}^*$ can be computed using (15), (16) and (17), respectively [11].

$$v_{\alpha o}^* = \frac{V_{dc3}}{3}(1 + 2k_1 - k_2) - v_{s\alpha}^* \quad (15)$$
$$v_{\beta o}^* = \frac{V_{dc3}}{\sqrt{3}}(1 + k_2) - v_{s\beta}^* \quad (16)$$
$$\Delta_j = {k_1}^2 + 2k_2 + 1 \quad (17)$$

In Fig.4(a), k_1 equation is represented by the vertical line which inclines at 120° to α axis. The result of this equation will only produce two states, either k1= 0 or k1= 1. If k1=0, the reference vector is in the region of Δ_1. Indicate a blue colored parallel line between upper and below triangle to separated Δ_3 from the rest. This line is referrer as k_2 has a distance value of $2/\sqrt{3}$ from α plane. Refer to previous Figure 2, the value of $2/\sqrt{3}$ is a height of every small triangle from the based to the tips of triangle. To identify which equations should be used in determining the triangle and vector components, it is necessary to evaluate the condition below [11]:

$$v_{\beta i}^* \leq \sqrt{3} v_{\alpha i}^* \quad (18)$$

where $v_{\beta i}^*$ and $v_{\alpha i}^*$ are obtained using (19) and (20).

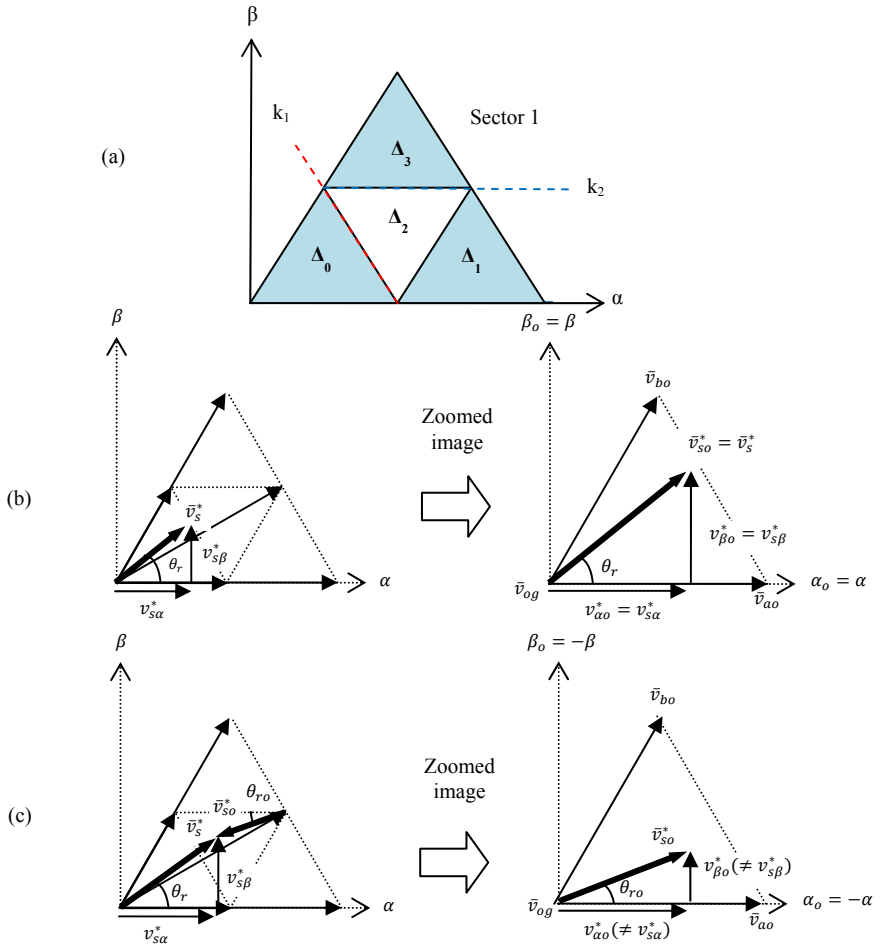

Figure 4. Definition of Reference Voltage Vector of Triangle (Δ_0 and Δ_2)

$$v_{\beta i}^{*} = \frac{3}{2V_{dc3}} v_{s\beta}^{*} - k_2 \frac{\sqrt{3}}{2} \tag{19}$$

$$v_{\alpha i}^{*} = \sqrt{3}\left(\frac{3v_{s\alpha}^{*}}{2V_{dc3}} - k_1 + \frac{k_2}{2}\right) \tag{20}$$

From (18), if the condition is satisfied, hence the triangle Δ_j (for j=0, 1 or 3) and the vector components $v_{\alpha o}^{*}$ and $v_{\beta o}^{*}$ can be calculated using (10), (11) and (12). But, if the condition is not satisfied, the triangle Δ_2 and the vector components $v_{\alpha o}^{*}$ and $v_{\beta o}^{*}$ can be obtained using (15), (16) and (17).

3.3. Calculation of On-Duration for Switching Vectors

The general representation of vector diagrams as shown in Figure 4 (b) and Figure 4 (c) is necessary for calculating the on-duration of application for each vector, $\bar{v}_{ao}$, $\bar{v}_{bo}$ and $\bar{v}_{og}$. In general, the calculation of on-duration can be obtained by considering the vector diagram ia applicable for any triangle in any sector. The on durations for switching two adjacent voltage vectors of $\bar{v}_{so}^{*}$ are calculated by the following equations [11]:

$$t_{ao} = \frac{3T}{2V_{dc3}}\left(v_{\alpha o}{}^{*} - \frac{1}{\sqrt{3}} v_{\beta o}{}^{*}\right) \tag{21}$$

$$t_{bo} = \frac{\sqrt{3}\, v_{\beta o}{}^{*} \cdot T}{V_{dc3}} \tag{22}$$

It should be noted that the switching period, is the total summation of on-durations for applying two adjacent voltage vectors and a vector which is defined as origin point to state the $\bar{v}_{so}^{*}$, i.e; $\bar{v}_{ao}$, $\bar{v}_{bo}$ and $\bar{v}_{og}$. Hence, the on-duration for applying the vector (as the origin point, as shown in Figure 4) can be simply obtained as:

$$t_{og} = T - (t_{ao} + t_{bo}) \tag{23}$$

3.4. Calculation of Duty Ratios

Major consideration in generating proper switching states (or PWM signals) is to provide high degrees of accuracy and linearity to obtain desired output voltages. At this stage, appropriate pulse width of pre-switching states (S_{sa}, S_{sb}, and S_{sc}) for each phase are generated based on the comparison between their respective duty ratio and the triangular waveform, as illustrated in Figure 4. Note that the pre-switching states are defined to determine the on-durations of voltage vectors which are valid for every sector as well as triangle.

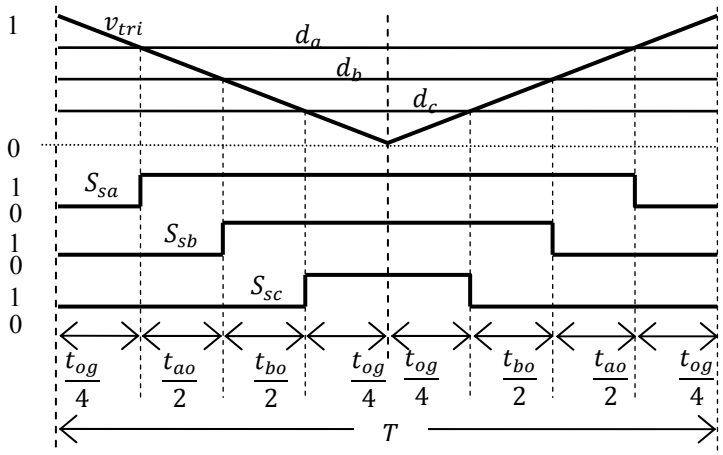

Figure 5. Generation of Pre-Switching States

Based on the definition of on-duration marked in Figure 5, the duty ratios, i.e. d_a, d_b and d_c for each phase in terms of on-durations in the case of three-level CHMI can be calculated using the following equations:

$$d_a = \frac{T - 2\left(\frac{t_{og}}{4}\right)}{T} \tag{24}$$

$$d_b = \frac{T - 2\left(\frac{t_{og}}{4} + \frac{t_{ao}}{2}\right)}{T} \tag{25}$$

$$d_c = \frac{T - 2\left(\frac{t_{og}}{4} + \frac{t_{ao}}{2} + \frac{t_{bo}}{2}\right)}{T} \tag{26}$$

3.5. Generation of Switching States

The switching operations of twelve IGBTs in the three-level CHMI are driven by the switching status, $S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c1}$ and S_{c2} (and also their respective complimented status $\bar{S}_{a1}, \bar{S}_{a2}, \bar{S}_{b1}, \bar{S}_{b2}, \bar{S}_{c1}$ and $\bar{S}_{c2}$) which are generated from a look-up table. The look-up table requires information of number of sector, triangle and pre-switching states. The switching status in the look-up table is mapped such that the switching vector for every sector as well as triangle satisfies the criteria and the switching sequence. It should be taking into account that the information of pre-switching states (S_{sa}, S_{sb}, and S_{sc}) will determine six switching states to drive upper switching devices for each leg of three H-bridge inverters (while the lower switching devices are driven by the complimented states).

4. DESCRIPTION OF EXPERIMENTAL SETUP

This section describes the tasks of circuits or components employed to set up the experimental platform for verifying the effectiveness of SVM control algorithm for three-level inverters. From Figure 6, it can be noticed that two controller boards are utilized to perform the tasks of SVM control algorithm. The reason of using two controller boards is that to minimize the computational burden of the main controller board which is DS1104 R&D Controller Board.

In implementing the SVM, its tasks are distributed into two parts, in which each part is performed by a single controller board. In doing so, the burden of calculation can be minimized; this in turn allows the computation in the main controller board performed at high sampling frequency.

4.1. DS1104 R&D Controller Board

The DS1104 R&D Controller Board is known as the most powerful controller board which is widely used in industry and university for developing system and rapid control prototyping. The major tasks of SVM algorithm are executed using the DS1104, which include:

- Determination of sector si, triangle Δ_j, vector components within a sector or triangle $v^*_{\alpha o}$ and $v^*_{\beta o}$.
- Calculation of on-duration t_{ao} and t_{bo}
- Calculation of duty ratios d_a, d_b and d_c

All tasks listed above are implemented using MATLAB-Simulink block diagram with special Real-Time Interface (RTI) Input/Output blocks. From Fig.6, the DS1104 R&D Controller Board provides information of sector si (3-bit), triangle Δ_j (4-bit) and pre-switching states S_{sa}, S_{sb} and S_{sc} in digital output form. In this case the decimal numbers of information are converted into Gray Code to prevent spurious output by allowing only one bit of binary digit changes for two successive values.

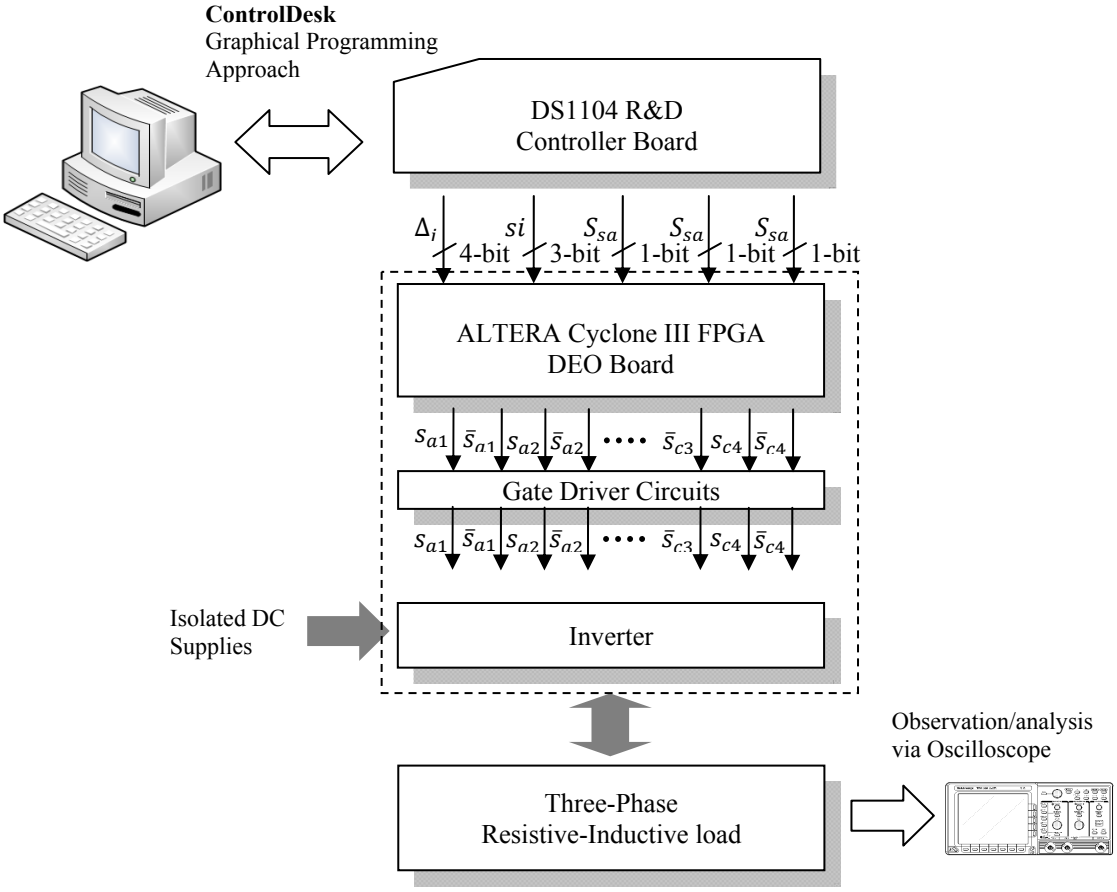

Figure 6. Experimental Setup

4.2. Altera FPGA DEO Controller Board

The Altera Field Programmable Gate Arrays (FPGA) DEO Controller Board is known to have high-speed clock which is superior to execute logical or digital operation. From Figure 6, it can be seen that the FPGA receives information of sectorssi (3-bit), triangle Δ_j (4-bit) and pre-switching states S_{sa}, S_{sb} and S_{sc} in digital Gray code. The FPGA is responsible to perform the task of selection of appropriate switching states based on the information received.

In practice, it is compulsory to provide blanking time for upper and lower IGBTs switching operation to avoid short circuit conditions. The blanking time is set approximately at $2\,\mu s$ by selecting appropriate threshold value to be compared with counters, implemented in FPGA. For convenience, the operation of blanking time generation for one leg of any or x-phase is described, with the aid of the block diagram and timing diagram, as illustrated in Figs. 7 and 8, respectively.

From Figure 7, it can be noticed that the signal S_x is the switching state for x-phase which is obtained from the voltage vectors selection table, as mentioned above. The block of MOD18 is assigned to divide the general clock frequency of FPGA $33.33MHz$ by 18, hence the new clock frequency becomes 1.85 MHz (or the new period 540 ns). The new clock frequency signal is designated as h as shown in Figure 7. The new clock frequency signal h is used to count up the upper counter (or the lower counter) by 1 for every 540 ns when S_x is active high (or active low), otherwise both counters will be reset to zero. Note the outputs of upper and lower counter are designated by the respective signals a and d. By comparing signals a and d with a constant value of 4, the blanking time is approximated to 2 μs. Increasing or decreasing the constant value of 4 will enlarge or reduce the blanking time, respectively. Note that, the signals s_x and $\bar{s}_x$ are for the upper and lower IGBTs of a leg of x-phase of VSI. The blanking time generator is duplicated for the other phases and legs to perform the same effect. Then the outputs of switching states from the blanking time generator are then fed to the gate driver circuits.

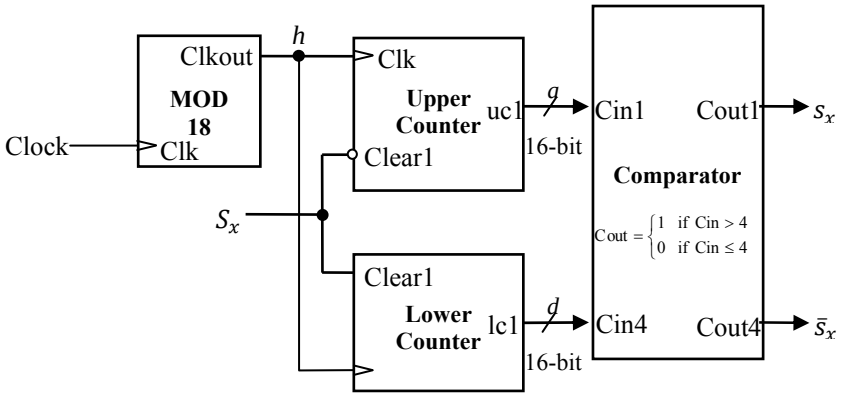

Figure 7. Block Diagram of Blanking Time Generation for x-Phase and Any Leg

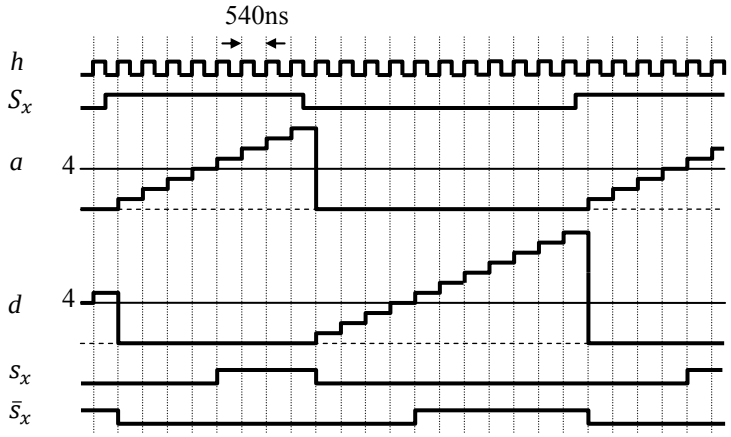

Figure 8. Timing Diagram of Blanking Time Generation for x-Phase and Any Leg

4.3. Power Inverter and Gate Driver Circuits

Figure 9 depicts a gate driver and power inverter circuits which are used to produce desired output voltages. The purposes of using gate driver circuits are to provide isolation between the electronic control circuits and power inverter circuits and to provide sufficient power amplification for switching IGBTs. It can be noticed from Figure 9, there are six units of H-Bridge inverter circuits to establish five-level CHMI. Each H-Bridge inverter circuit is supplied by an isolated DC voltage supply. From this figure, it also shows that the FPGA controller board and I/O interface DS1104 card.

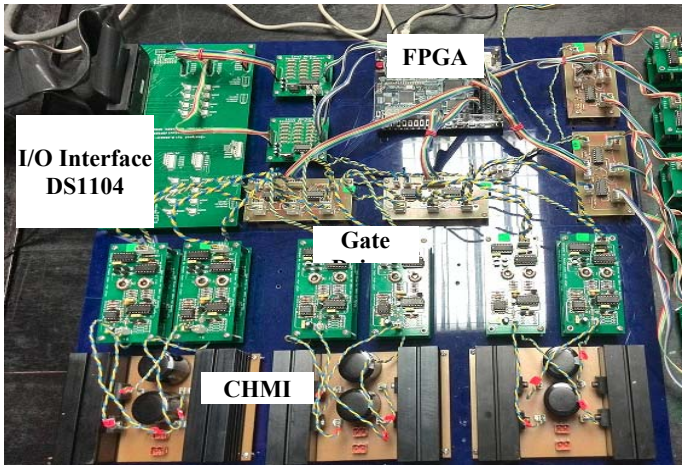

Figure 9. Photograph of FPGA, Gate Driver Circuits and Cascaded H-Bridge Multilevel Inverter (CHMI)

4.4. Three-Phase and Series Connected Resistive and Inductive Loads

A three-phase and series connected resistive and inductive load is employed for analyzing the performance of SVM for two-level, three-level and five-level of inverters. The load is represented by a load reactor model MV 1101 from TERCO, where its specification and rated condition are given in Table 1.

Table 1. Load Reactor Parameters

Parameters	Value
Rated Reactive Power	2.5kVAr
Frequancy	50-60Hz
Rated Voltage	380V Y, 220V Y/Δ
Rated step regulation	287.81mH , 28.082 Ω

5. RESULT ANALYSIS OF TOTAL HARMONIC DISTORTION (THD) OF OUTPUT VOLTAGE

This section evaluates the total harmonic distortions (THD) of output voltage and the accuracy of fundamental output voltage V_1 of three-level inverters. The evaluation is based on the simulation results (i.e. the values of THD and fundamental output voltage are obtained using Fast Fourier Transforms (FFT) analysis), as well as comparison with the experimental results.

The evaluation on THD of output voltage and the accuracy of fundamental output voltage V_1 resulted in every level of inverter is also carried out at different modulation indices, $M_i = 0.3$ and 0.9. The simulation results obtained from the evaluation are demonstrated in Figs. 10. From these figures, it can be observed that the experimental results are in close agreements with the simulation results. Specifically, the patterns of wave shape and frequency spectrum of output voltages in the experimental results are similar to that obtained in the simulation results.

The similarities between simulation and experimental results, allow the results of THD and fundamental output voltage obtained via simulation to be assumed similar with that of experimental results with the error between the simulation and calculated values is insignificant and approximately less than 1 %.

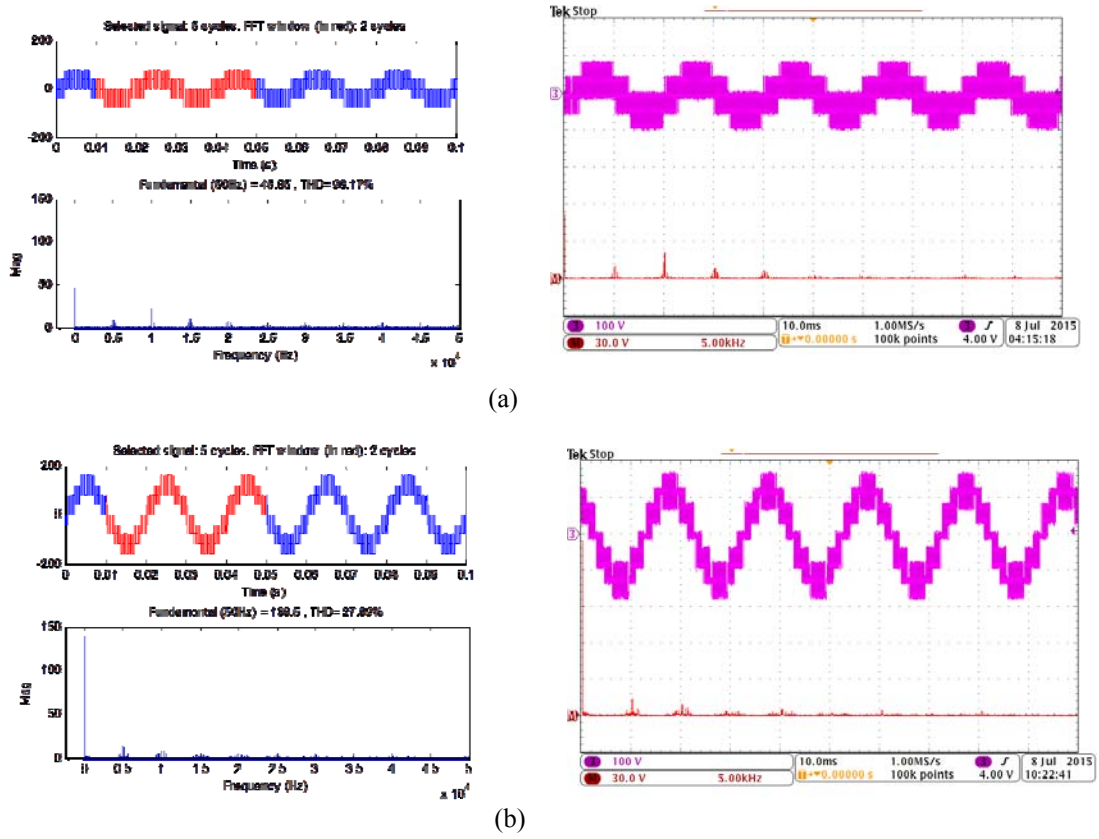

Figure 10: Simulation and Experimental Results of Phase Voltage and its Frequency Spectrum when Modulation Index (a) $M_i = 0.3$ and (b) $M_i = 0.9$

6. CONCLUSION

This paper presented a technique to implementation the space vector modulator scheme for multilevel inverters. The designs structure is built to minimize the mathematic algorithms in order to ease the implementation in hardware. The scheme contains simple althorithm to interpret the on duration and duty ratio which it all based on the two levels SVM. The implementation required less memory and can be computationally fast. The scheme can perform very well for any reference vector with any modulation index and can easily be extended to any levels. The simulation result with FFT analysis and experiment result has verified the proposed SVM development.

ACKNOWLEDGEMENTS

The authors would like thanks the Ministry of Education Malaysia (KPM) and Universiti Teknikal Malaysia Melaka (UTeM) for providing the research grant FRGS/2013/FKE/TK02/02/1/F00159 for this research.

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