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Asymmetrical Cascaded Multi Level Inverter using Control Freedom Pulse width Modulation Techniques

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ABSTRACT

In this paper, the suggested topologies are gained by cascading a full bridge inverter with dissimilar DC sources. This topology has several new patterns adopting the fixed switching frequency, multicarrier control freedom degree with mixture conceptions are established and simulated for the preferred three-phase cascaded multilevel inverter. In outstanding switching arrangement terminations, there are convinced degrees of freedom to produce the nine level AC output voltages with terminated switching positions for producing altered output voltages. These investigations focus on asymmetrical cascaded multilevel inverter engaging with carrier overlapping pulse width modulation (PWM) topologies. These topologies offer less amount of harmonics present in the output voltage and superior root mean square (RMS) values of the output voltages associated with the traditional sinusoidal pulse width modulation. This research studies carries with it MATLAB/SIMULINK based simulation and experimental results obtained using appropriated prototype to prove the validity of the proposed concept.

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1. INTRODUCTION

The cascaded half bridge multilevel inverter combined a several units of single phase half bridge power cells. The importance of this configuration is recognized to some characteristics required in other inverter topologies [1, 2]. This topology compromises a good prospect for the growth of the number of levels with decreased total harmonic distortion and switching losses. Asymmetrical type cascaded half bridge inverters demonstration great efficiency up to 90% at the supply frequency [3, 4]. In [5], the optimum arrangements for this topology are examined for several objectives such as less number of power semiconductor switches and input DC voltage sources and lowest standing voltage on the power semiconductor switches for generating the supreme output voltage levels [5]. The Neutral A single phase seven level Asymmetrical Multilevel Inverter fed resistive load using carrier overlap PWM technique with different reference [6], it is a modular improve allowing presented converter topologies, particularly the five-level active neutral point clamping, to create an improved number of levels (in this case 9 level) and, thus, a high-quality output with a very narrow amount of extra switches while keeping the switching frequency at a level headed.

A new scheme of line-voltage total harmonic distortion calculation gives estimated answers, because high-order harmonics are unnoticed. In this work, an analytical algebraic scheme based on formulates the line-voltage with total harmonic distortion of multilevel inverters with uneven DC sources is accessible. These schemes are general and relevant to the each number level [7]. A new approach on the cascaded multilevel inverter analysis a carrier based discontinuous pulse width modulation scheme.

The separation of the offset into the major and supplementary components shows the use for analysis of pulse width modulation manage a characteristics of multilevel inverters [8]. Technology of a hybrid modulation scheme present combination of fundamental frequency modulation and multilevel sinusoidal-modulation scheme, and are planned for performance of the famous alternative phase opposition disposition control, phase shifted control, carrier based space vectormodulation control, and single carrier sinusoidal modulation control [9]. The two level and three level neutral point clamped inverter by using SVPWM Technique with Photovoltaic Cell is used as input source [10]. The carrier phase shifted SPWM equipment is implemented in the cascaded multilevel inverter to decreaseharmonic content available in output voltage wave and current wave, in the interim, a novel style of bypassmanage technique is projected to collect all the energy in feedback system and return it into the energy to feedback unit [11]. The recognized fractal arrangement is utilized to recommend a generalized algorithm for SVPWM production for two legged five level multilevel inverters [12]. The assessment of carrier arrangement based bipolar PWM techonolgy of trinary nine level multilevel inverters with various PWM technologies [13].

This paper proposes a novel three phase, Nine-level inverter topologies with a Trinary-DC sources. The suggested topologies are gained by cascading a full bridge inverter with uneven DC sources. These topologies have several new patterns adopting the fixed switching frequency, multicarrier control freedom degree with mixture conceptions are established and simulated for the preferred three-phase cascaded multilevel inverter.

2. PROPOSED TRINARY MULTILEVEL INVERTER

The three-phase multilevel inverter is being used for a large number of industrial applications due to their capability of high-power accompanying with lesser output harmonics and lesser switching losses. Multilevel inverter has grown into an active and applied resolution for increasing output power and decreasing total harmonics distortion of AC load system. The proposed Trinary cascaded multilevel inverter contains two full bridges with dissimilar voltage sources. The first full bridge contains the DC source of $1V_{DC}$ and the second full bridge contains the DC source $3V_{DC}$ as presented in Figure 1.

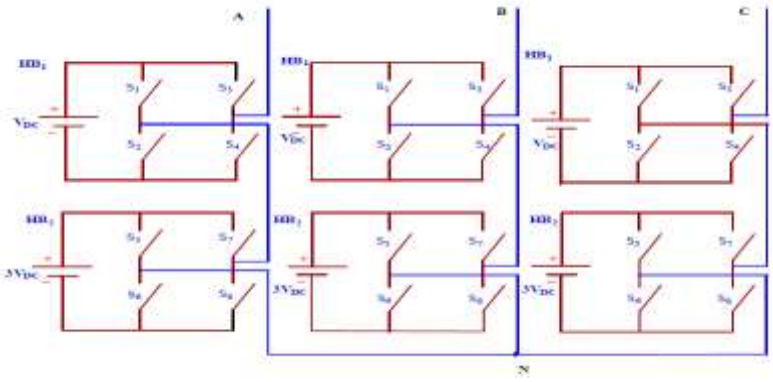

Figure 1. The Proposed Trinary Cascaded Multilevel Inverter

Each DC source is connected to a proposed three phase inverter. Each inverter produces a three dissimilar output voltage levels, such as positive, zero and negative levels by different groupings of the four power semiconductor switches S_1, S_2, S_3 and S_4. Whenever the switches, S_1 and S_4 is turned ON, then the output voltage is positive level (+Ve); whenever the switches S_2 and S_3 is turned ON, then the output voltage is negative level (-Ve); whenever either pair of switches (S_1 and S_2) or (S_3 and S_4) is turned ON, then the output voltage will be at zero level (0). Then the output voltage of first bridge can be made equal to the $-1V_{DC}$, 0, or $1V_{DC}$, correspondingly the output voltage of second bridge can be made equal to the $-3V_{DC}$, 0, or$3V_{DC}$ by turning ON and turning OFF its power semiconductor switches properly. Consequently, the output voltage of the inverter values for $-4V_{DC}$, $-3V_{DC}$, $-2V_{DC}$, $-1V_{DC}$, 0, $4V_{DC}$, $3V_{DC}$, $2V_{DC}$, $1V_{DC}$, can be planned, as represented in Figure 1 and table 1 represents the switching sequence of proposed multilevel inverter. The lower inverter (HB_2) produces a necessary output voltage with three levels, and then the upper inverter (HB_1)

adding or subtracting one level from the fundamental output voltage wave to produce Level ped waves. Here, then the final output voltage levels becomes the summing of each terminal voltage of cascaded H bridge, and Then the output voltage of the load is given in (1a) and (1b)

$$V_{out}=V_{HB1}+V_{HB2} \quad (1a)$$

(Or)

The output voltage of the first bridge is indicated by Vdc and the second full bridge is indicated by 3Vdc. Then the output voltage of the load is

$$V_{out}=V_{DC}+3V_{DC} \quad (1b)$$

In the proposed inverter circuit topologies, if *m* number of cascaded H bridge segment has unequal DC sources in order of the power of 3, a predictable output voltage levels are given as

$$V_m = 3^m, m = 1, 2, 3.....$$

Table 1. Output Voltage Level and Their Switching Sequence of Proposed MLI

Output Voltage Level V_{out}	Switching Sequence of Proposed MLI							
	First Half Bridge (HB1)				Second Half Bridge (HB2)			
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$4V_{DC}$	On	Off	Off	On	On	Off	Off	On
$3V_{DC}$	Off	On	Off	On	On	Off	Off	On
$2V_{DC}$	Off	On	On	Off	On	Off	Off	On
$1V_{DC}$	On	Off	Off	On	Off	On	Off	On
0	Off	On	Off	On	Off	On	Off	On
$-1V_{DC}$	Off	On	On	Off	Off	On	Off	On
$-2V_{DC}$	On	Off	Off	On	Off	On	On	Off
$-3V_{DC}$	Off	On	Off	On	Off	On	On	Off
$-4V_{DC}$	Off	On	On	Off	Off	On	On	Off

3. CARRIER OVERLAPPING PULSE WIDTH MODULATION TECHNIQUES

In this research, sinusoidal reference signals with several overlapping triangular carriers are selected to produce a preferred output voltage. Then the purpose of every inverter is to modify a DC input voltage into a nearby AC output voltage with preferred magnitude and frequency which can be attained by using a number of modulation schemes. Then the proposed multilevel inverter needs N-1 triangular carriers producing a nine level output voltage. As far as the certain reference wave is disturbed, there is also several control freedom containing frequency, amplitude, phase angle of the modulating signals and as in three phase proposed circuits, to insert zero sequence signal to the modulating signals. Then, multilevel carrier based pulse width modulation techniques offer many control freedom.

These control freedom arrangements combined with the simple topologies of the multilevel inverters produce an output voltage with the help of multilevel carrier based pulse width modulation approaches. This research offers four carrier overlapping pulse width modulation techniques that employs the control freedom of a vertical offsets amongst carrier. The following carrier overlapping techniques are used: Sub harmonic pulse width modulation scheme (SHPWM), Phase disposition scheme with carrier overlapping pulse width modulation (COPWM-1), Phase opposition disposition scheme along with carrier overlapping pulse width modulation (COPWM-2), alternate phase opposition disposition along with carrier overlapping pulse width modulation (COPWM-3). The above four schemes are employed in this work.

The N-level inverter (using N-1 carriers with the equal frequency of f_c and equal peak-to-peak amplitude of AC) is predisposed such that the bands they occupy overlapping with each other; the overlapping vertical detachments concerning each carrier are $A_c/2$.

3.1. Sub Harmonics Pulse Width Modulation

In Sub harmonics pulse width modulation schemes, all the triangular carriers are in phase with each other. For an N-level inverter using bipolar switching multicarrier pulse width modulation techniques, (N-1) carriers have same frequency f_c and same peak-to-peak amplitude A_c. Then the reference waveform has amplitude of A_m and frequency of f_m and it is centered about the zero level. Then the reference wave is always compared with each of the triangular carrier signals. When the reference wave is more than the triangular carrier signal, the active devices equivalent to that carrier signals are switched ON. Otherwise, the devices switched OFF. Then the sub harmonics pulse width modulation scheme yields only odd harmonics order for odd m_f; and yields odd and even order harmonics for even m_f. Figure 2 shows the pulse generation and carrier arrangement for sub harmonics pulse width modulation scheme for m_a = 0.85 and m_f = 2000HZ.

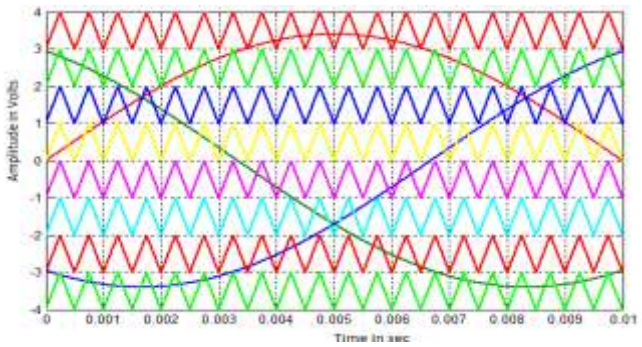

Figure 2. Carrier and reference wave arrangement of a SHPWM control (m_a=0.85 and m_f = 2000 hz)

3.2. Carrier Overlapping In Phase Disposition Pulse Width Modulation System

The vertical offset of carriers for a nine level Trinary DC source multilevel inverter with carrier overlapping in phase disposition pulse width modulation techniques are illustrated in Figure 3. In this topology, all the eight carriers are overlapped with each other and the reference sinusoidal waveform is placed at the central point of the eight carriers.

3.3. Carrier Overlapping Phase Opposition Disposition Pulse Width Modulation System

The carriers for a nine level Trinary-DC source, multilevel inverter with carrieroverlapping phase opposition disposition pulse width modulation techniques are illustrated in Figure 4. In this topology, all the carriers are divided uniformly into two groups according to the positive/negative standard levels. These two groups are opposite and 180° out of phase width those below the zero values.180° out of phase with each other while maintenance in phase within the group phase opposition disposition pulse width modulation topology.

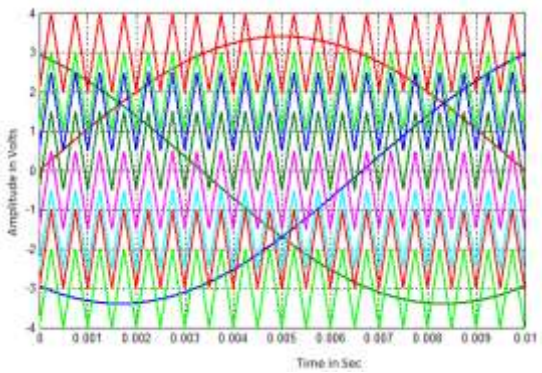

Figure 3. Carrier and reference wave arrangement of a COIPD PWM control (ma=0.85 and mf = 2000 hz)

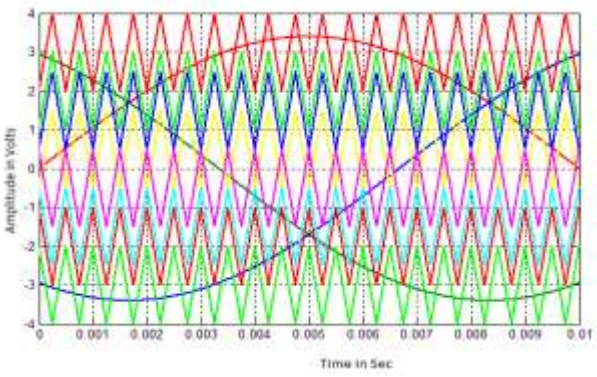

Figure 4. Carrier and Reference Wave Arrangement of a COPOD PWM Control (m_a=0.85 and m_f = 2000 hz)

3.4. Carrier overlapping Alternate Phase Opposition Disposition Pulse Width Modulation system

The carriers for a nine level Trinary DC source multilevel inverter with carrieroverlapping alternate phase opposition disposition pulse width modulation techniques are illustrated in Figure 5. In this topology, the carriers are 180◦ alternate phase displace from each other. It may be recognized as pulse width modulation with amplitude overlapping, and neighbouring phases are interleaved carriers.

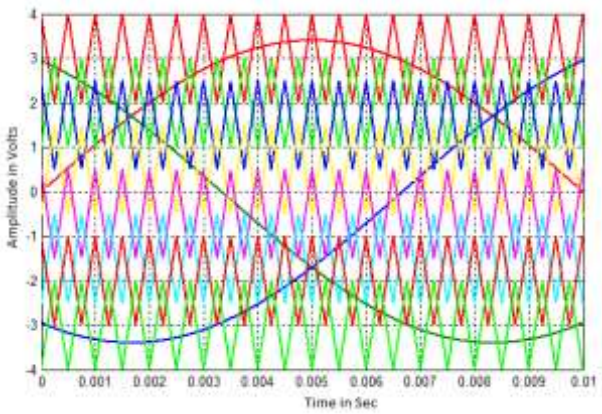

Figure 5. Carrier and reference wave arrangement of a COAPOD PWM control (m_a= 0.85 and m_f =2000 hz)

4. SIMULATION RESULTS

A novel three-phase, Nine-level inverter topologies with a Trinary - DC sources are offered. The three phase nine level cascaded multilevel inverters with Trinary - DC sources are modeled in SIMULINK using power systems block set is shown in Figure 6. The three phase inverter it has the 120 degree phase shift with each phase. Simulations are performed for a choice of ma assorted from 0.8 to 1 and the resultant %THD is measured using the FFT blocks and their values are exposed in Table 2. Table 3 displays the fundamental VRMS of inverter output voltage for similar values of modulation indices. Figure 7-11 shows the simulation output voltage and FFT plot of a nine level cascaded multilevel inverter with Trinary DC source, and their appropriate harmonic order of a spectrum with bipolar pulse width modulation technology, but for only one sample of the modulation index. For modulation indices (ma=0.85) it is observed from the Figures (8, 9, 10 and 11) the harmonic energy level is governing in: Figure 8 represent the harmonic energy level in sub harmonics PWM techniques shows 40th order of harmonic. Figure 9 represents the harmonic energy level in PD PWM technique shows 40th order of harmonic.

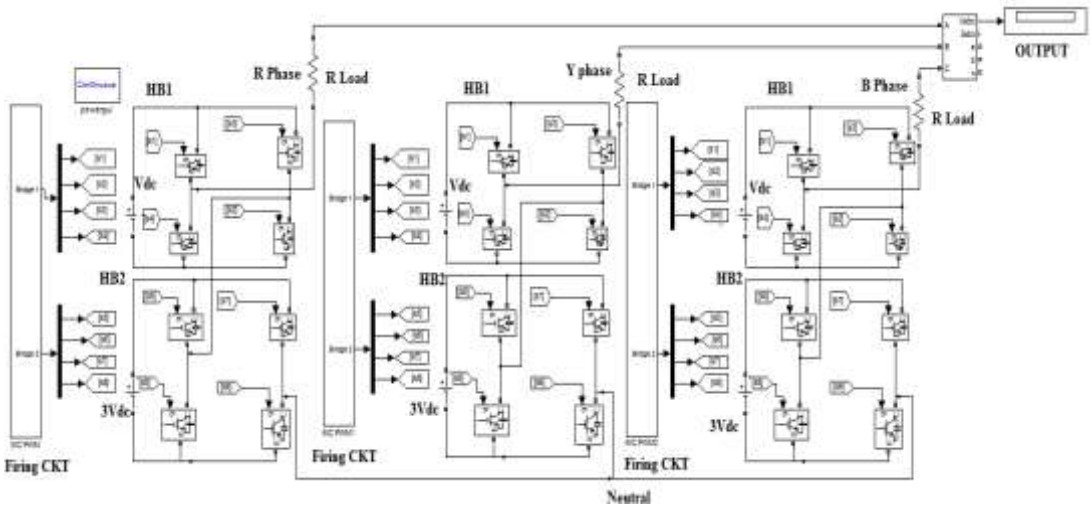

Figure 6. Simulink model of Trinary DC source three phase multilevel inverter

Figure 10 represents the harmonic energy level in POD PWM technique shows 38th, 40th order of harmonic. Figure 11 represents the harmonic energy level in APOD PWM technique shows 29th, 31st, 39th order of harmonic. Simulations are performed for various values of m_a ranges from 0.8 to 1 and the results are obtained by using following parameter such as V_{DC} = 25V , $3V_{DC}$ = 75V, load resistance is 100Ω, carrier frequency f_c is 2000Hz and modulation frequency $f_m$is 50Hz.

Figure 12 represent the THD contrast of COIPD, COPOD, COAPOD and SHPWM pulse width modulation techniques no more than one pulse modulation techniques such as SHPWM (Sub Harmonics Pulse Width Modulation) it hold minimum quantity of harmonic distortion. Figure 13 represent the V_{RMS} contrast of COIPD, COPOD, COAPOD and SHPWM pulse width modulation techniques no more than one pulse modulation techniques such as COP (Carrier overlapping Phase Opposition Disposition) it hold maximum quantity of fundamental RMS output voltage.

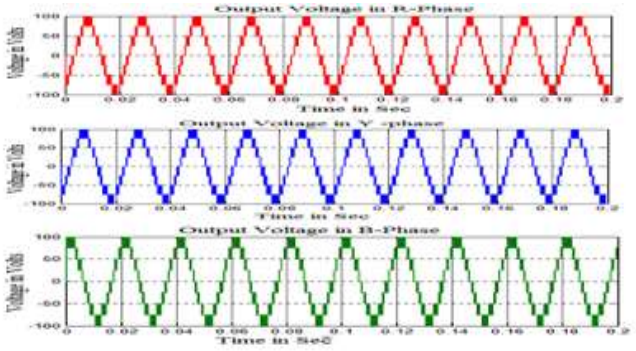

Figure 7. Output Voltages Generated by Control Freedom PWM Control with Sinusoidal Reference

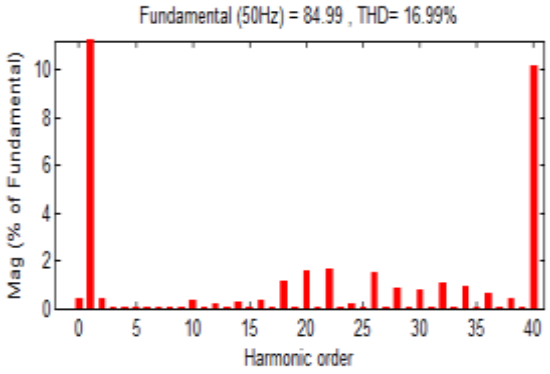

Figure 8. FFT Plot for a Output Voltage of Sub Harmonics PWM Control with Sinusoidal Reference

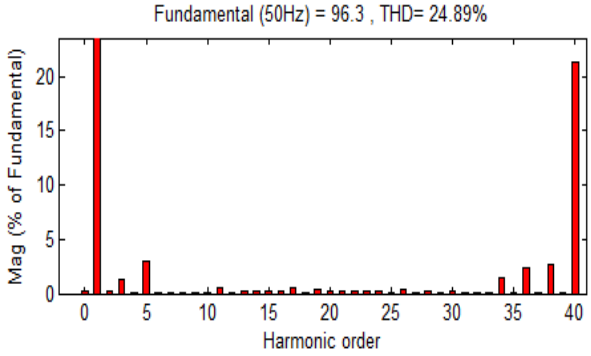

Figure 9. FFT Plot for Output Voltages Of Carrier Overlapping in Phase Disposition PWM control with Sinusoidal Reference

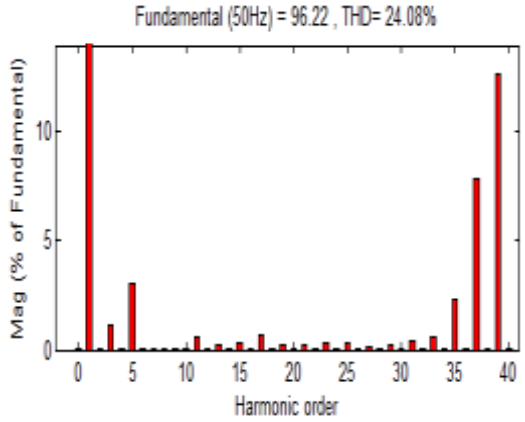

Figure 10. FFT Plot For Output Voltage of Carrier Overlapping Phase Opposition Disposition PWM Control with Sinusoidal Reference

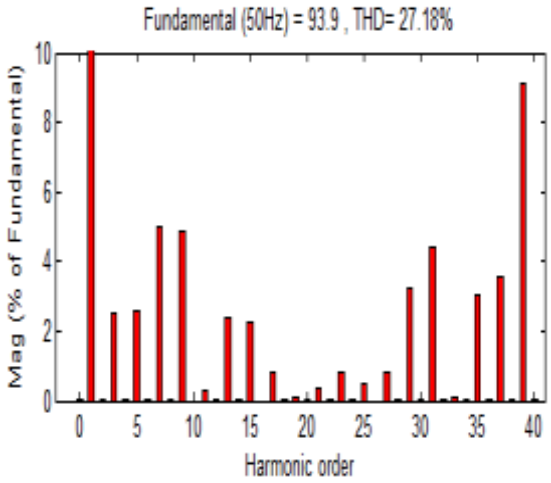

Figure 11. FFT Plot for Output Voltage of Carrier Overlapping Alternate Phase Opposition Disposition PWM Control with Sinusoidal Reference

Table 2. % THD for Different Kind of Modulation

m_a	Sine Reference			
	SHPWM	COIPD	COPOD	COAPOD
1	13.75	20.67	20.02	22.02
0.95	15.59	22.02	21.41	23.67
0.9	16.78	23.48	22.88	25.36
0.85	16.99	24.89	24.08	27.18
0.8	17.13	26.62	25.76	29.52

Table 3. Fundamental RMS Voltage for Different Kind of Modulation Indices

V_{rms}	M_a				
	1	0.95	0.9	0.85	0.8
SHPWM	70.71	67.16	63.65	60.09	56.59
COIPD	75.62	73.26	70.75	68.09	65.21
COPOD	75.67	73.31	70.73	68.04	65.19
COAPOD	74.4	71.78	69.24	66.12	63.15

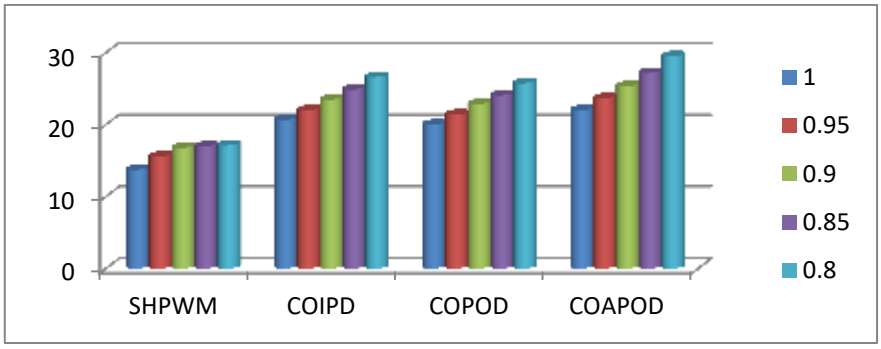

Figure 12. Carrier Overlapping Technique %THD V_s Modulation Indices

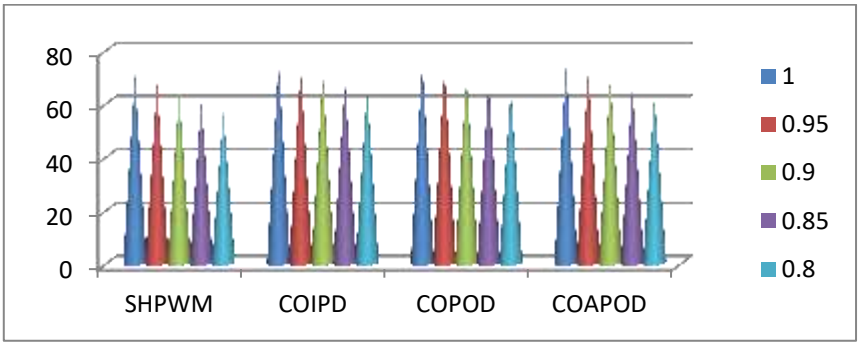

Figure 13. Carrier Overlapping Techniques Fundamental Vrms V_s Modulation Indices

5. HARDWARE TEST BOARD AND RESULTS

Experimentally the research authenticates the proposed nine level cascaded multilevel inverter and prototype model of single phase nine level Trinary-DC source cascaded multilevel inverter has been developed by using IGBTs as switching devices. In this research the hardware test board is implemented by using the PIC microcontroller PIC16F877. The hardware implementation for nine level cascaded multilevel inverter is as shown in Figure 14. The input voltage for cascaded H-Bridge circuit is $1V_{DC}$ and $3V_{DC}$ Volt. The output voltage waveforms of nine level single phase cascaded trinary multilevel inverter shown in Figure 15.

Figure 14. Complete Set of Nine Level Single Phase Cascaded Trinary Multilevel Inverter by Using Multicarrier PWM Techniques

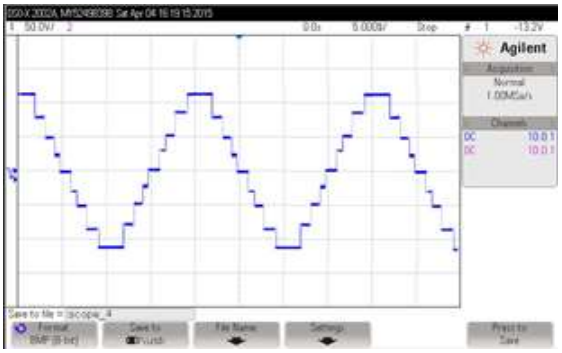

Figure 15. Output Voltage Waveforms of Nine Level Single Phase Cascaded Trinary Multilevel inverter by Using Multicarrier PWM Techniques

6. CONCLUSION

Three-phase asymmetrical cascaded multilevel inverter with control freedom pulse width modulation techniques has been developed. This topology has established that the newly adopted control freedom techniques such as sub harmonics pulse width modulation techniques produce a lesser value of total harmonic distortion and carrier overlapping phase opposition disposition method develop a higher value of fundamental V_{RMS} voltage. Finally, the simulation and research laboratory tests (prototype model) are achieved to show the strength of the proposed three-phase asymmetrical cascaded multilevel inverter. After that foot level in the three-phase asymmetrical cascaded multilevel inverter testing is carried out with help of three-phase induction motor drive using predictable speed and torque control.

REFERENCES

[1] M. Malinowski., et al., "A survey on cascaded multilevel inverters", *IEEE Trans. Ind. Electron*., vol. 57, pp. 2197–2206, 2010.

[2] C. Kiruthika, et al., "*Implementation of digital control strategy for asymmetric cascaded multilevel inverter*", International Conference on Computing, Electronics and Electrical Technologies (ICCEET), pp. 295–300, 2012.

[3] K. Radha Sree, et al*., "Asymmetric cascaded multilevel inverter for electric vehicles'*. International Conference on Advances in Engineering, Science and Management (ICAESM), pp. 758–763, 2012.

[4] Khoucha, F., et al., "A comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives", *IEEE Trans. Ind.Electron*., vol. 26, pp. 64–72, 2011.

[5] E. Babaei, "Optimal Topologies for Cascaded Sub- Multilevel Converters", *Journal of Power Electronics*, Vol. 10, No. 3, pp. 251-261, 2010.

[6] R. Johnson Uthayakuma., et al., "A Carrier Overlapping PWM Technique for Seven Level Asymmetrical Multilevel Inverter with various References", *IOSR Journal of Engineering*, vol. 2, no. 6, pp. 1301-1307, 2012.

[7] N. Farokhnia, et al., "Calculating the Formula of Line-Voltage THD in Multilevel Inverter With Unequal DC Sources", *IEEE Transactions On Industrial Electronics*, vol.58, no. 8, pp. 3359–3372, 2011.

[8] N. Nguyen, et al., "An Optimized Discontinuous PWM Method to Minimize Switching Loss for Multilevel Inverters", *IEEE Transactions On Industrial Electronics*, vol. 58, no. 9, pp. 3958–3966, 2011.

[9] C. Govindaraju, et al., "Efficient Sequential Switching Hybrid-Modulation Techniques for Cascaded Multilevel Inverters". *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1639–1648, 2011.

[10] Shantanu Chatterjee, "A Multilevel Inverter Based on SVPWM Technique for Photovoltaic Application," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 3, no. 1, pp. 62 -73, 2013.

[11] Wang Pan, et al., "Research on a New Type of Energy Feedback Cascade Multilevel Inverter System", *TELKOMNIKA*, Vol.11, no.1, pp. 494-502, 2013.

[12] DevisreeSasi, et al., **"**Generalized SVPWM Algorithm for Two Legged Three Phase Multilevel Inverter", *International Journal of Power Electronics and Drive System (IJPEDS)*, Vol.3, no.3, pp. 279-286, 2013.

[13] D. Periyaazhagar et al*.,"*Comparative study on three phase cascaded inverter for various bipolar PWM techniques,"*Int. J. Modelling, Identification and Control*, Vol. X, No. Y, 200x in press.

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