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Investigation of the Common Mode Voltage for a Neutral-Point-Clamped Multilevel Inverter Drive and its Innovative Elimination through SVPWM Switching-State Redundancy

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ABSTRACT

The purpose of this paper is to provide a comprehensive Investigations and its control on the common mode Voltage (CMV) of the three-phase three-level neutral-point diode-clamped (NPC) multilevel inverter (MLI). A widespread space-vector pulse width modulation (SVPWM) technique to mitigate the perpetual problem of the NPC-MLI, the CMV, proposed. The proposed scheme is an effectual blend of nearest three vector (NTV) and selected three vector (STV) techniques. This scheme is capable to reduce the CMV without compromise the inverter output voltage and Total harmonics distraction (THD). CMV reduction achieved less than +Vdc/6 using the proposed vector selection procedure. The theoretical Investigations, the MATLAB software based computer simulation and Field Programmable Gate Array (FPGA) supported hardware corroboration have shown the superiority of the proposed technique over the conventional SVPWM schemes.

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1. INTRODUCTION

Recently, multilevel inverters (MLIs) have gained a lot of attention in the field of medium & high power applications [1]. Many pulse width modulation (PWM) techniques proposed in the literature [2] to control the MLIs. However, all PWM produces alternating common-mode voltages (CMVs) that create substantial problems in power drives. The alternating CMVs create significant common-mode current (CMC) leakage called as bearing current (ib), which may cause premature motor bearing failures [3-4]. CMV divided into two types of approaches: 1) full elimination (FE) and 2) partial elimination (PE) of CMV.

There have been a number of techniques suggested for FE CMV and EMI eliminations. However, few of them have addressed the CMV directly and successfully [5-7]. However, PE method is still having lost challenging for further reduction of CMV. Hence, the researcher gears in this field to give the substantial. A solution to the CMV problem is to use passive filters [8-9] to reduce the CMV/CMC. The solution is to revise the PWM control strategy for the inverter to reduce the CMV have been reported for both carrier-based and SVM schemes [10-12], First, Kim et al. [7] propose PE by using carrier PWM for a three-level NPC-MLI. Due to the non-nearest vectors, the THD produced by this scheme is higher than conventional method. Mohan M.Range *et al* [13] has been compared CMV generation with Various SPWM methods like PD,POD,APOD verses various reductions, however the further reduction have not consider this paper. C.Bharatiraja, *et al.* [12] proposed a scheme whereby the minimal CMV sequence voltage for each level made Vdc/6 using PD and POD PWM schemes. However further elimination not noticed in this paper.

In this paper, the Investigation has done against CMV over SVPWM switching technique for an for three level diode clamped multilevel inverter (DCMLI).Next,It is proposed two techniques is explored to eliminate CMV further by selecting appropriate switching states using SV PWM. The switching selection for the state vector to for the proposed PEs developed in FPGA-IP core and implemented for three-level inverter. The simulation and experimental results provided to validate the implementation of five-level diode clamped inverter.

2. INVESTIGATIONS OF CMV FOR NPC-MLI=

2.1. Calculations of CMV

The instantaneous summation of all the three phase voltages at output of the inverter is non-zero, an average voltage in a neutral point with respect to ground create so called common mode voltage (CMV) [10].

$$V_{com}=1/3\ (s_a+s_b+s_c\ ) \quad (1)$$

The electrostatic induced bearing voltage, V_b is the appearance of the stator CMV at the neutral point and it radiates the noise over the bearings via the machine capacitances. This V_b is the main cause of the motor bearing current (i_b), which leads to damage the bearing system and hence decrease the lifespan of the bearing. Generally, the solutions to reduce this phenomenon are based on the motor design consideration (to decrease the effective capacitive couplings in the first step of the design, CMV/CMC eliminatingfilters and the CMV reduction by using MLI topology and proper PWM techniques [6], [12]., Bearing voltage V_b is expressed as

$$V_b=BVR\cdot V_{com} \quad (2)$$

where, BVR = Bearing voltage ratio, Vcom= common mode voltage

$$V_b = \frac{c\omega s}{c_b+c_{rs}+c\omega s} \times Vcom \quad (3)$$

Capacitor bearing current,

$$i_b = c_b \cdot \frac{dV_b}{dt} \quad (4)$$

The CM current formed by a superposition of current pulses i_{ag}, i_{bg} and i_{cg}, generated in the inverter-fed ac machine, when the line-to-ground voltages vug, vvgandvwgswitched between the two levels $+½V_{dc}$. On the assumption of balanced three-phase power supply and the line-to-neutral impedances per phase Z_{ph}, the CMV corresponds to voltage difference between stator neutral and electrical ground or dc bus midpoint. Where V_{aN}, V_{bN} & V_{cN} are motor terminal phase voltages wth respect toto neutral. R_m and L_m are per phase equivalent resistance and leakage inductance of motor respectively. The stator neutral, 'N' point to ground, 'G' voltage can be expressed as

$$V_{an} = v_{aG} - v_{nG} = R_m I_a + L_m \frac{di_a}{dt} + e_a \quad (5)$$

$$V_{bn} = v_{bG} - v_{nG} = R_m I_b + L_m \frac{di_b}{dt} + e_b \quad (6)$$

$$V_{cn} = v_{cG} - v_{nG} = R_m I_c + L_m \frac{di_c}{dt} + e_c \quad (7)$$

From eq (5) – (7) and three phase balanced system $i_a + i_b + i_c = 0$; $e_a + e_b + e_c = 0$,

$$V_{NG} = \frac{1}{3}[V_{aG} + V_{bG} + V_{cG}] = V_{com} = \frac{1}{3}\sum_{z=a}^{c} V_{nG} \quad (8)$$

$$CMV= V_{com} = V_{NG} = \int \frac{\sum_{z=a}^{c} i_{zG}\, dt}{c\ 3\ c\omega s} \quad (9)$$

Bearing voltage

$$V_b = BVR \cdot \frac{1}{3\omega sc} \int_{Z=a}^{c} i_{zG}\, dt \quad (10)$$

The CMV is responsible for i_b and EDM [4]. EDM creates localize delegated temperature of the race and results in molten pits and fluting. The bearing current is also responsible for degradation of oil quality and premature failure of bearing. Capacitive bearing Current:

$$i_b = c_b \cdot \frac{dV_b}{dt} \quad (11)$$

$$i_b = BVR \cdot c_b \frac{dVnG}{dt} \quad (12)$$

Circulating bearing current: this current flow from the stator winding to fram capacitance $C_{ws.}$

$$V_b = BVR \cdot \frac{1}{3\omega sc} \int_{Z=a}^{c} i_{zG}\, dt \quad (13)$$

Henceforth, the reduction in $V_{com}$is much required to avoid discharge currents, reduce capacitive and circulating currents and Low frequency of dV_{com}/ dt occurrences.

3. ANALYSIS OF CMV DEPEND UPON SWITCHING STATES

3.1. SVPWM Schemes for Three Level MLI

The SVPWM gives the target output sinusoidal voltage by using a rotating vector having a constant amplitude and frequency. The constant reference voltage vector V*, defined by$V^*=|V^*|*e^{j\omega t}$.The vector is identified as a point of complex space (α, β), and the harmonics can be eliminated and fundamental voltages obtained are better. Figure 1 shows the three -phase three- level space vector diagram, which consists of 6 sectors (S_i), 19 voltage vectors, 27 switching states and each sector contains four inner triangles [15]. The voltage vectors classified into four types; large vector (LV), medium vector (MV), small vector (SV) and zero vector (ZV).They are six LVs {[1-1-1], [11-1], [-11-1], [-111], [-1-11], [1-11]}; six medium vectors-{[10-1], [01-1], [-110], [-101], [0-11], [1-10]}; and six short vectors. The rotating reference vector, V* can lie in any of the Each short vector is having two switching states-{([100]&[0-1-1]),([110]&[00-1]),([010]&[-10-1]),([011]&[-100]),([001]& [-1-10]), ([101]&[0-10])}; One ZV, which is having three switching states-{[000], [111], [-1-1-1]}.sectors and particularly in one among the four sub-triangles in the sector. If the reference vector lies in 1stsector of Δ1,1 sub triangle, then S_{V1}, S_{V2} and M_{V1} vectors can be used to synthesize the sampled reference voltage vector V* [18].

$$V^*\delta_{SV1} + V^*\delta_{SV2} + V^*\delta_{MV1} = V^* \quad (14)$$

$$\delta_{SV1} + \delta_{SV2} + \delta_{MV1} = \delta \quad (15)$$

δ_{S1}, δ_{S2} and δ_{M1} are the calculated duty cycles of the switching vectors.

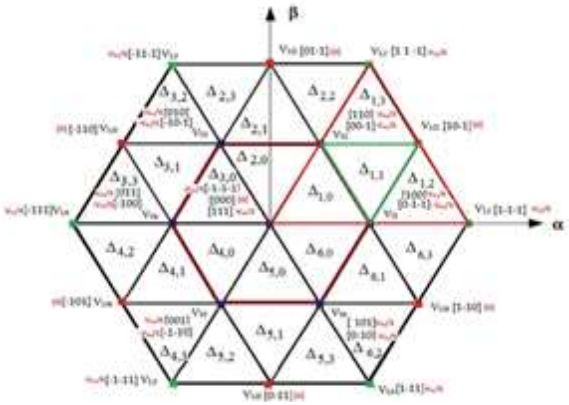


Figure 1. SVPWM switching vector diagram for 3phase-3 level NPC-MLI.

3.2. Influence of Vector Selection in CMV

The PWM based conventional inverter/MLI is the series connected switching devices connected with input dc bus voltage. Its controlled by due to simultaneously switching of the series connected device, motor terminal voltage shifts from $-V_{dc}$to $+V_{dc}$ and vice versa at high switching frequency of switching devices through PWM, accordingly the inverters generates high dv/dt and V_{com}. Using the switching function S_x, x =a, b, c of inverter and dc bus voltage, voltage at neutral point can be expressed as

$$V_{rG} = \frac{1}{3}\sum_{x=a}^{c} V_{xG} \tag{16}$$

For 3 level DCMLI with dc bus voltage Vdc, the voltage across each capacitor is $V_{dc/2}$. Thus, the voltage stress on the each switch will be $V_{dc/2}$. The pole voltage V_x ($V_{dc/2}$, 0.-$V_{dc/2}$) and it corresponding switching state switching function (sx) are given as follows

$$V_{xG} = V_{dc}\left[s_x - \frac{1}{2}\right] \tag{17}$$

$$s_x = 1$$

$$V_{com} = V_{nG} = \frac{V_{dc}}{3}\sum_{x=a}^{c} s_x - \frac{V_{dc}}{2} \tag{18}$$

$$V_s = \frac{2}{3}(s_a + s_b e^{j(2\pi/3)} + s_c e^{-j(2\pi/3)}) \times \frac{V_{dc}}{2} \tag{19}$$

CMV corresponding to the switching state expressed as

$$V_{com} = \frac{1}{3}(s_a + s_b + s_c)\frac{V_{dc}}{2} \tag{20}$$

When 3 level MLI operated through SVPWM technique, the LVs and MVs are uniquely determined by switching state, conversely the magnitudes of Vcom is $\pm V_{dc/6}$ and 0 respectively. SVs generate $\pm V_{dc/3}$ and $\pm V_{dc/6}$. ZVs have 3 switching states and their CMVs are Zero and $\pm V_{dc/2}$.For Example, to obtain the CMV produced by any one ZV [-1-1-1] eq (20) can be used, that is$V(com([-1-1-1]))=1/3\cdot(-3)\cdot V_{dc/2}= -V_{dc/2}$.SV [0-1-1] in sector-1 is generating $V_{com}([0\text{-}1\text{-}1]))=1/3\cdot(-2)\cdot V_{dc/2}=-V_{dc/3}$and MV [10-1] in sector CMV is producing $V_{com}([1\text{-}0\text{-}1]))=1/3\cdot(0)\cdot V_{dc/2}=0$.In the same fashion, the CMV values caused by all 27 switching states are summarized as $\pm V_{dc/2}$, 0, $\pm V_{dc/3}$, $\pm V_{dc/6}$. Hence, based on the above comprehensive investigation, 12 switching states that produced $\pm V_{dc/6}$, 7 states produce zero CMV, 6 states produces $\pm V_{dc/3}$ and 2 states produce $\pm V_{dc/2}$. Sector S-1 considered for discussion in Figure 1. It consists of four sub-triangles (Δ_0-Δ_3).In Δ_0, due to the participation ZVs and SVs with redundant state, the resultant CMV is $\pm V_{dc/2}$. When reference toils in sub-triangle Δ_1, 4-SVs and one MV makes $\pm V_{dc/3}$, $\pm V_{dc/6}$, and the same way Δ_2 and Δ_3 produce $-V_{dc/3}$, $+V_{dc/6}$ and $-V_{dc/3}$, $+V_{dc/6}$ respectively. Thus the maximum CMV in sector-1 is $\pm V_{dc/3}$. The same manner CMV is produced in the rest of the sector as well, thus for 27 vectors, Vcom are illustrated in Figure 1.

The ability of multilevel inverter is that when increasing the level, a multi-stepped voltage prevents motor failure by reducing CMV with any PWM schemes. In the partial elimination, the CMV can be $\pm V_{dc/6}$. In other hand, even 3 level without increasing the level by choosing proper switching, the CMV can be reduced up to $\pm V_{dc/3}$(n-1) for n-level inverter, while the 3-level inverter allows the reduced CMV of magnitude up to reduced partially and fully.

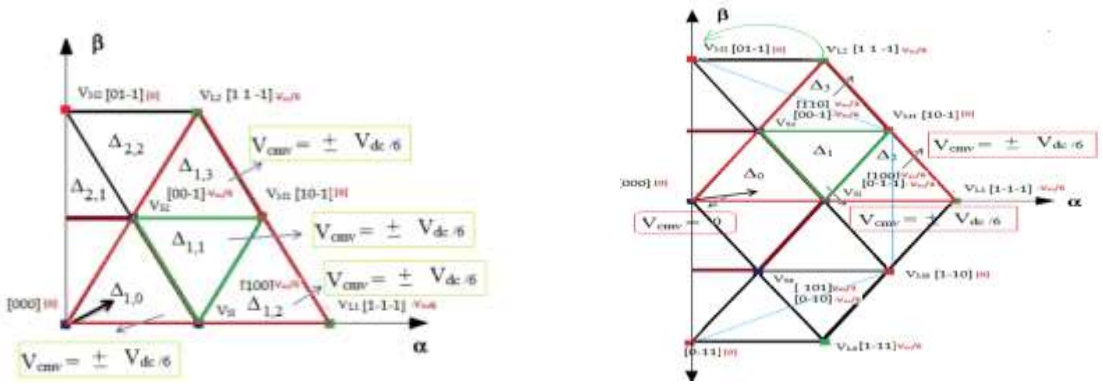
4. PROPOSED VECTOR SELECTION ALGORITHMS FOR PE OF CMV

The proposed vector selection based SVPWM schemes are classified into two types based on the usage of LV as 1. PE with LV (SVPWM-1), 2. PE without LV (SVPWM-2)

4.1. PE with LV (SVPWM-1)

In the proposed SVPWM scheme the CMV is reduced upto±Vdc/6 with 90 % of the output voltage, which are greater than the existing PE methods [13] .In the SVPWM each switching states produce the different values of the CMV.CMV is mostly influenced by the some of ZV and SV. For e.g. zero vector [000] produceCMV zero but another ZVs [111] & [-1-1-1] produces CMV as ±Vdc/2. In the proposed scheme the states, which producing the CMV as ±Vdc/2, ±Vdc/3 can be eliminated by the selected switching state, Hence the CMV reduced up to ±Vdc/6 as shown in Figure 1. In the proposed SVPWM scheme out of

27 switching states only 19 states are used to achieve reduced CMV as ±Vdc/6. With respect to the Figure 2.a, the Vrefis located in the sector 1 in the triangle Δ1,0. At normal operation the switching pulse generated for triangle Δ1, 0 is consist of 3- ZVs (000, 111, -1-1-1), and 4-SVs (100, 00-1, 110, 00-1). As a result the CMV is between ±Vdc/2 to ±Vdc/3.while using the proposed scheme to the triangle Δ1,0uses only one ZV(000) and 2-SVs(100, 00-1) , as a outcome the CMV value is reduced between 0 to ±Vdc/6. The Figure 2.b shows proposed SVPWM Switching Pulse for Sector 1 in triangle Δ1, 0 due to that CMV is reduced up to ±Vdc/6. The selected SVPWM switching scheme for Sector -1 (sub triangle switching state from Δ1,0 to Δ1,4) for the PE is shown in Table -1.In additional to that the proposed selection uses simple mathematical calculations to compute the duty cycle of the different switching as shown in equation (15).



(a) (b)

Figure 2.a. switching vector diagram for 3 level NPC-MLI, b. modes of operation in sector-1 and their CMV

4.2. PE without LV (SVPWM-2)

The CMV is mostly depends upon the sum of ZVs &LVs. For e.g. out of 3 ZVs, one ZV [000] produce zero CMV and another two ZVs [111] & [-1-1-1] produces CMV as $\pm V_{dc/2.}$ There by choosing the proper switching states in the SVPWM scheme the CMV reduced. In the existing PE scheme the states, which producing the CMV as $\pm V_{dc/2}$, $\pm V_{dc/3}$ eliminated without using the redundancy techniques [6]. In the conventional PE. When the reference vector comes under the triangles ($\Delta_{1,3}$, $\Delta_{2,3}$, $\Delta_{3,3}$, $\Delta_{4,3}\Delta_{5,3}\Delta_{6,3}$) one of the vertices of these triangle constitutes of LV as shown in the Figure 2.a. In the proposed scheme the V_{ref} is made shifted to 30^0 and instead of using LVs (11-1), (-11-1), (-111), (-1-11), (1-11) & (1-1-1) the scheme uses the nearest MVs of the corresponding LVs.In the conventional PE method all, the four triangles in a sector are equilateral triangles whereas in the proposed scheme, two triangles are equilateral and the remaining two are Isosceles triangles. In the conventional partial elimination, when the reference vector located in sector, triangle $\Delta_{1,3}$ the switching pulse generated for this triangle will constitute of one small vector V_{S2} (00-1),one MV V_{M1}(10-1) and one large vector V_{L2}(11-1).

Table 1. CMV elimination triangle switching state

	Sector	Switching States In Conventional SVM	Switching States in PE	Switching States in PE Without LV
1	ZV	[000](0) [111](V_{dc}/2) [-1-1-1](-V_{dc}/2)	[000](0)	[000](0)
	SV	[100](V_{dc}/6) [0-1-1](-V_{dc}/3)	[100](V_{dc}/6)	[100](V_{dc}/6)
		[110](V_{dc}/3) [00-1](-V_{dc}/6)	[00-1](-V_{dc}/6)	[00-1](-V_{dc}/6)
	MV	[10-1](0)	[10-1](0)	[10-1](0)
	LV	[1-1-1](-V_{dc}/6)	[1-1-1](-V_{dc}/6)	-

These vectors will produce a CMV of $\pm V_{dc/6}$. Where as in the proposed PE scheme, instead of switching the V_{L2} (11-1) the nearest MV V_{M2}(01-1) is used and the CMV is reduces to-$V_{dc/6}$. Inthe same manner, the reference vector is in $\Delta_{1,2}$ instead of switching the LV V_{L1} the nearest MV V_{M6} is used and the

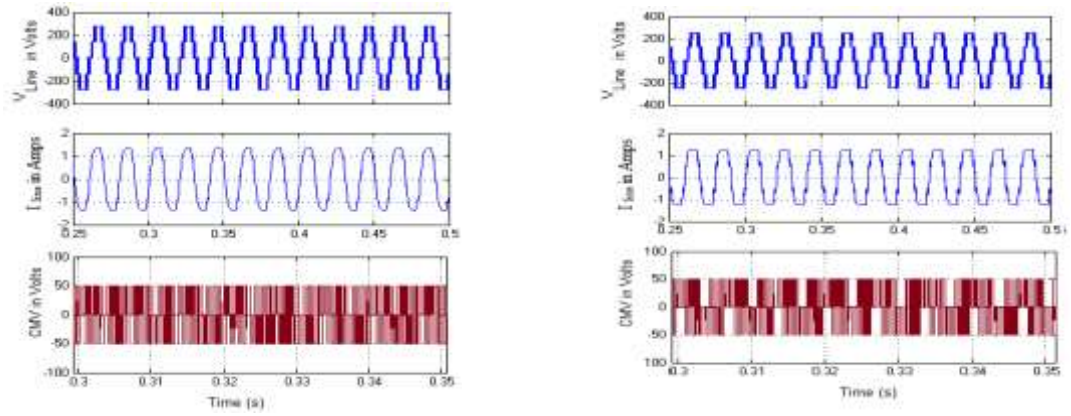
CMV is reduced to $\pm V_{dc/6}$. As the Resultant, the proposed SVM scheme those LVs not allowed to participate in the switching sequence. Finally compare to the existing PE scheme, the recommended SVM scheme reduces the CMV created by all LVs. As the result, the proposed partial elimination scheme only produces 3 times $\pm V_{dc/6}$ & 3 times-$V_{dc/6}$ (produced by SVs),whereas in the conventional partial elimination produces 6 times $\pm V_{dc/6}$ & 6 times-$V_{dc/6}$ (produced by both LVs & SVs) [17].

5. SIMULATION AND EXPERIMENTAL RESULTS

5.1. Simulation Result

The performance of the proposed CMV elimination algorithm based SVM has been investigated and simulateed by MATLAB 11.b/SIMULINK with 12switch NPC-MLI, DC-link voltage of 200V, two 100µF capacitors, 5kHZ switching frequency and a 4 -pole,50Hz,1420 rpm, 1-HP squirrel cage 3-phase induction motor drive (IMD). The switching frequency and modulation indexes is selected for the all investigation are 5 kHz and m_a= 0.907.

First, the investigation begins with conventional SVPWM scheme at 0.9 modulation index; the CMV is about 84V. Hence using Eq. (3), the CMC value of 3.7% computed. Following, the test has been done for proposed SVPWM-1 and SVPWM-2. Figure 3 (a) & (b) show the CMV resulted from the SVPWM-1 and SVPWM-2.Here, for the SVPWM-1 the CMV and inverter output voltage is observed as 38.5 V &223.3V respectively, which is 33 % less than reported existing schemes [7] Therefore, SVPWM-1 scheme reduced the CMV without tumbling output voltage of the inverter. Finally, the study has done for proposed SVPWM-2 scheme which is swhon in Figure 3.b. Here, the scheme escaping the LV contribution. Henceforth the CMV reduced to 37.3V, which is 2.76 % less than proposed SVPWM-1 scheme and 34% below the conventional scheme. As the result, CMC decreases from 15. Amps (rms), to 1.4 Amps (rms), without a significant increase in THD. The CMC measurement for conventional SVPWM-1 (without elimination), SVPWM-1 (elimination with LV) and SVPWM-2 (elimination without LV) shown in Figure 4. Based on this, it is undershoot that the SVPWM-2 gives less CMC compare to other methods.



(a) (b)

Figure 3. Simulation results: (a).V_{Line}, CMV and CMC for SVPWM-1, (b). V_{Line}, CMV and CMC for SVPWM-2

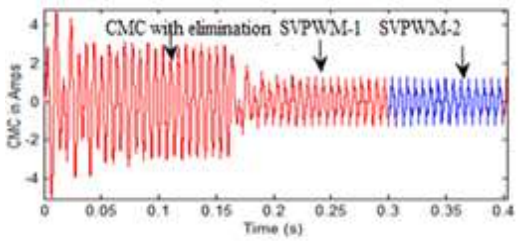


Figure 4. Simulation results: CMC measurement in Conventional SVPWM-1 (without elimination), SVPWM-1 (elimination with LV) and SVPWM-2 (elimination without LV)

5.2. Experimental Result

The proposed SVPWM-1 and SVPWM-2 schemes is programmed in Verilog Hardware Descriptive Language (VHDL) code and synthesized in minimum computational load using SPARTAN -III-3AN-XC3S400 FPGA family board. This board separately designed for a high performance power-electronics controller with more than 1000 MIPS [14]. In the proposed PWM scheme, the dead bands of the inverter legs are properly tuned as 4.2µs. The SVM modulator duty-ratio information is calculated in Figure 5.b and pulse is generated through FPGA, which derives the control signals for the 12 pulse inverter switches NPC-MLI. The SVPWM-1 and SVPWM-2 switching sequences mapped by using the 2D-look up table (LUT). The algorithm tested experimentally on a 3-level NPC-MLI laboratory prototype inverter fed ASD with the same specification considered for simulation study. This prototype laboratory setup shown in Figure 5.a.The corroborating Experimental results are captured using 6 channels YOKOGAWA digital signal oscilloscope (DSO) and the switching pulses are captured using 2 channels Agilent technologies DSO. Noted that the previously mentioned tests executed without any common-mode (CM) filter in order to observe the CM signature of these PWM schemes. The results of CMV and common-mode current (CMC) measured utilizing a tong tester. In the beginning, the investigation is carried out with conventional SVM scheme in LM index as ma=0.907 and the resulting CMV is observed about 83.63V ($\pm V_{dc/3}$) and the i_b through the test ASD is measured as 2.45 A (rms) by using a tong tester in the motor shaft are shown in Figure 5.

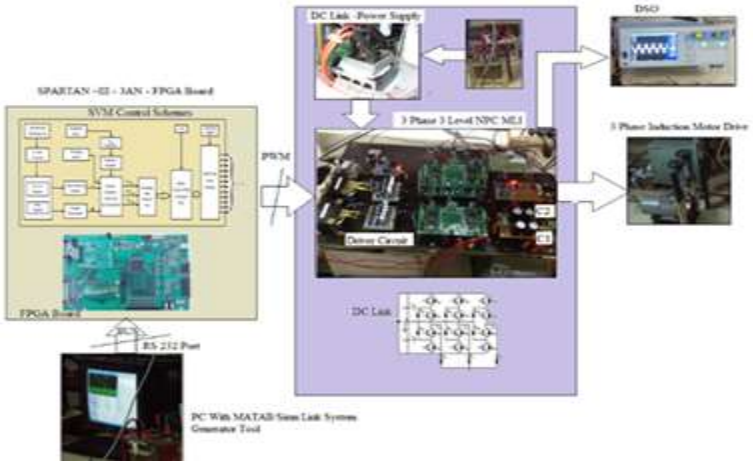
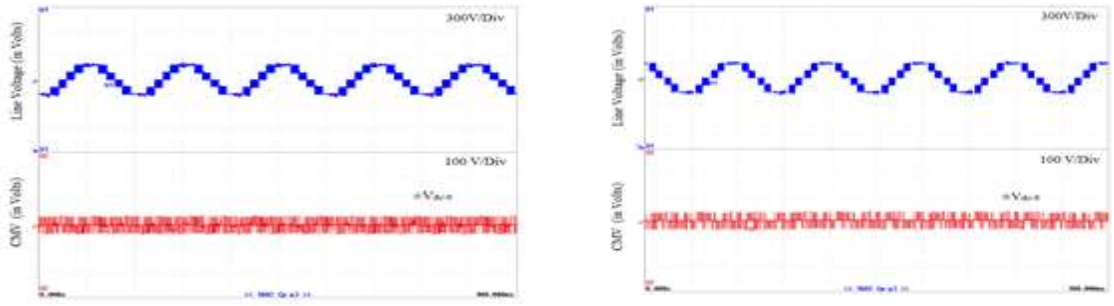


Figure 5. Experimental set up - SVM based 3 level inverter using FPGA SPARTENIII

The Figure 6.a and 6.b show the V_{line} and CMV of proposed SVPWM-1 scheme, which compromises the reduced CMV of 38.73 with V_{line} of 222.71V (rms). Here, it is observed that with reduced CMV the V_{line} is 7 % higher than existing scheme [6]. Figure 6.b shows the experimentalVline and CMV of the proposed SVPWM-2 scheme.At this point the CMV (37.3V) is significantly reduced to 2.3% further as compared to existing PE schemes and SVPWM-1, as the result CMC decreases as same as simulation, without a significant increase in THD.



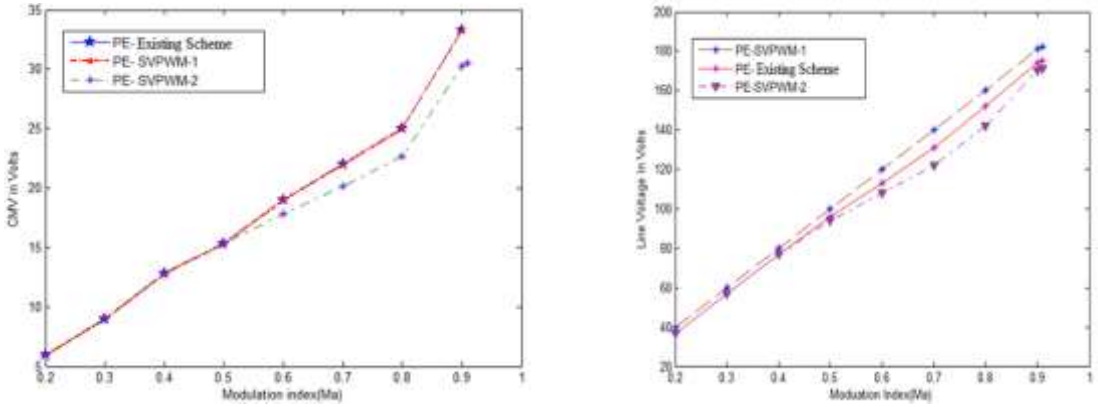
(a) (b)

Figure 6. Experimental results: (a). V_{Line} and CMV for SVPWM-1, (b). V_{Line} and CMV for SVPWM-2

As mentioned before, THD is relatively higher for isosceles triangles and its value being around 14.478%. Therefore, the proposed SVPWM-2 scheme is able to maintain CMV within a specified tolerance value with any modulation index and for wide load variation. Hence, large size CM filter are not required.

6. RESULT DISCUSSION

In Figure 7, the graph shows the CMV, Vline and THD performance of the proposed schemes with existing technique with respect to ma. Here, upto 0.5 m_a both proposed schemes have given the same performance. Moreover, after 0.5 m_a the proposed schemes shows their performance.



(a) (b)

Figure 7. Comparative analysis for SVPWM-1 and SVPWM-2 with existing PE (a) CMV vs m_a, (b) V_{line}vs m_a

It is observed that the proposed SVPWM-1 scheme CMV is reduced the upto$\pm V_{dc/6}$) with maximum inverter voltage. In SVPWM-2 absence of LV, the CMV further reduced up to 33.2V, which is 2.1% less than SVPWM-1.Hence, SVPWM-2 scheme is much suitable for ASD application like DTC, Vector control and Field oriented control based drives.

7. CONCLUSION

A SVPWM modulation approach for controlling the CMV voltage in the three-phase three-level NPC-MLI presented. The proposed SVPWM scheme reduces the CMV upto ±Vdc/6 V with over the full range of inverter output voltage, THD. Thus, the proposed scheme limits the CMV/CMCwhich is well below the as compared to existing methods .The scheme significantly reduces the size of the CMV filters and maintains the volt-sec balance throughout the working range. The experimental results corroborate the triumph of the proposed method.

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