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Hysteresis SVM for Coupled Inductor Z Source Diode Clamped 3-level Inverter based Grid Connected PV System

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ABSTRACT

Due to its advantages such as it can defeat problems such as leakage current and insertion of DC in the grid and provides low stress on power devices, Diode-clamped three-level inverter (DCTLI) is habitually used in transformerless photovoltaic (PV) connected to grid network. But it still has a problem of shoot-through which dwells in its legs, so its operation not reliable. Z source network is employed to permit operation without shoot through risk and improve its reliability. Coupled inductors are replaced the line transformers in to attain lower cost, reduced size, and improved its reliability and efficiency. Coupled inductor which avoids leakage current problem and losses. It employs coupled inductor z source diode clamped three level inverter (CI-Z-DC-TLI) to boost the voltage and further progress the consistency of the proposed system by avoiding the shoot through the problem. The proposed system assures that common-mode voltage and shoot-through risk is avoided. Moreover, controlling DC-TLI with Hysteresis SVM algorithm which improves output voltage and current control. Simulation and experimental results of this proposed system were analyzed using MATLAB environment and FPGA hardware.

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1. INTRODUCTION

Renewable energy is a vital source of free energy, in modern year's Photovoltaic cell (PV) has developed into very attractive because of the extreme reduction in the price of PV modules and also for it oblige less maintenance, is free from pollution and zero fuel cost [1]. The photovoltaic cell (PV) uses the energy from the sun directly to generate electricity which is free, the installation being its only significant cost. Multilevel inverters have gained more interest due to the limitations of conventional 2-level inverters when it comes to high power and voltage applications. They utilize an array of series of switches for power conversion. The distinctive multilevel inverter structure permits them to achieve high voltages with low harmonics without the use of any filtering device [2]. Multilevel inverters also make it easy to the use of renewable energy sources such as PV, wind, fuel cell. Among the various types of multilevel inverters, diode-clamped three level topology is mostly established when the need of transformerless PV system arises because it can defeat problems such as leakage current and insertion of DC on the grid [3]. The shoot through problem also exists in 3-level diode-clamped which decreases the system reliability. Z source network is utilized to overcome shoot through the problem and to improve the reliability of diode-clamped inverter [4]. Z source network is a unique impedance network connection of two capacitors and two inductors in an X shape, which is used to boost the output voltage [5].

Transformerless coupled inductor z source diode clamped multilevel inverter (CI-Z-DC-TLI) evades the usage of the transformer for connecting the inverter to the grid system [6]. While using a transformer, the

leakage current increases, and distortion of grid current. A system without a transformer will be cheaper in cost, smaller in size, and lighter in weight than the system with line transformers. Coupled inductors are used to replace line transformers so as to attain lower cost, compact shape and improve reliability and efficiency of the system [8]. The transformer creates the path for the leakage current between the PV array and the grid [9]. Therefore, DC-TLI is used to prevent the leakage current. The proposed system uses hysteresis space vector modulation (HSVM) as the control technique. HSVM controls the current in a circular hysteresis area to perform the balancing of dc voltage [10].

This proposed system makes use of coupled inductor z source diode clamped three level inverter (CI-Z-DC-TLI) with the PV array as the input of the proposed system; coupled inductors are used to reduce the cost and losses. The z source network boosts the output voltage and further improves the reliability of the system by preventing the shoot-through problem.

2. PV ARRAY AND MPPT ALGORITHM

Photovoltaic array energy can be directly rehabilitated into electric energy using a device known as Photovoltaic cell. Light energy is converted into electrical energy using a process called as the "photovoltaic effect". PV cells are made up of primarily two semi-conductor layers, viz; a P-layer which consists of the positive charge and an n-layer which consist of negative charge. The PV cell's output voltage depends on the sunlight intensity, temperature, efficiency and size of the panel. The PV array is simply a combination of many PV cells in series or parallel connection to produce an output voltage and current [11].

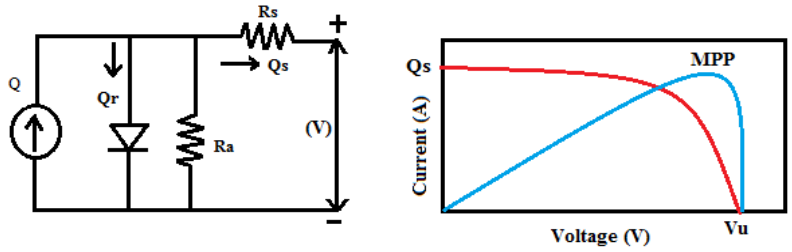
$$\boldsymbol{Q} = \boldsymbol{Q_S} - \boldsymbol{Q_r}\mathrm{Q_R} \tag{1}$$

$$\mathrm{Q_r} = \mathrm{Q_0}(\mathrm{e}^{\frac{\mathrm{qV_p}}{\mathrm{hT}}} - 1)1) \tag{2}$$

Where h is the Boltzmann's constant, ϕs is short circuit current, q is the electron charge, ϕo is the reserve saturation current, T is the junction temperature, Vp is the voltage across the diode and ϕr is the diode current. Therefore substituting equation (1) in (2), we have,

$$\phi = \phi_S - \phi_O\left(\mathrm{e}^{\frac{\mathrm{qV_p}}{\mathrm{hT}}} - 1\right) - 1) \tag{3}$$

Since the source is non-linear, PV panel's efficiency is extremely low and hence to increase the efficiency operating point of the panel is shifted to the maximum power point (MPP) [12]. Maximum power point tracker (MPPT) is used to track the maximum power from the PV panel.



(a) (b)

Figure 1. (a) PV Model and (b) I-V Characteristics

2.1. MPPT Algorithm

The competence of the solar panel can be enhanced when MPPT is used to extract maximum power coming from the PV panel. The PV output depends on the environmental factors which vary from sunrise to sunset. To achieve maximum efficiency of the panel we make the group to operation at MPP [13], [14]. From the maximum transfer theorem; in a circuit, the output power is maximum when the source side impedance matches the load side impedance [15]. The simplest and most used method to ensure that the PV panel is operating at MPP is perturb and observe (P & 0) algorithm. A perturbation was made from the PV panel the voltage and current are obtained to calculate the output power [16]. The previous power and ΔP is compared with calculated power. If the difference ΔP> 0, then the perturbation is continued in the direction but when

ΔP< 0 then the direction is reversed.

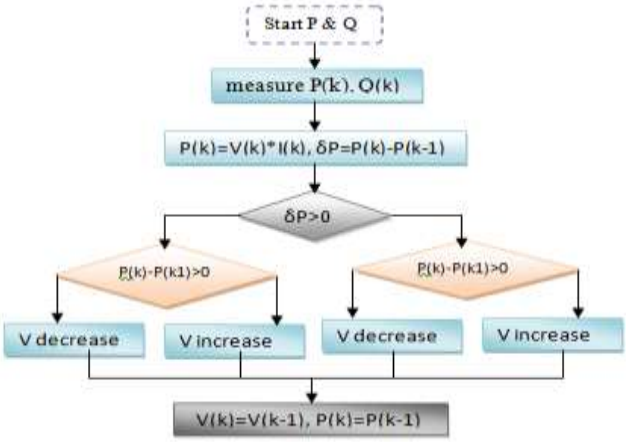


Figure 2. Flow Chart of Perturb & Observe Algorithm

3. DIODE CLAMPED THREE LEVEL INVERTER

Diode-clamped three level (DC-TLI) inverter has gained much interest in recent years and is widely accepted by researchers today [17]. Also known as NPC three level inverter is shown in Figure 3. Because of its topological advantages such as overcoming the problem of leakage current and preventing the insertion of DC currents into the grid, diode clamped three level inverter is broadly accepted in a transformerless system with PV connected to the grid network [18], [19].

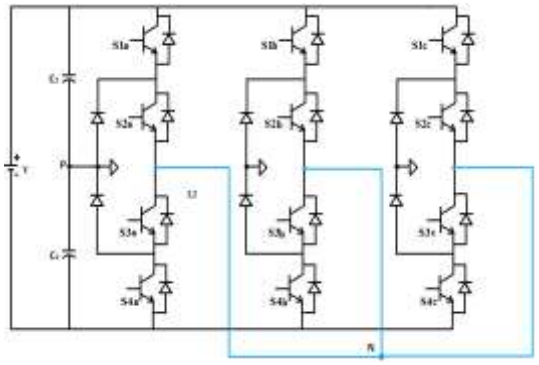


Figure 3. Three Level Diode-Clamped Inverter

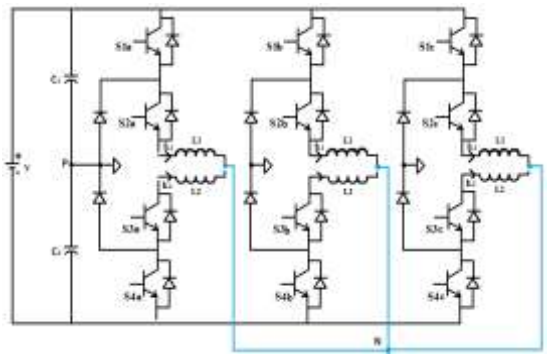


Figure 4. Coupled Inductor Based Diode Clamped

Diode-clamped inverter generates staircase voltage at its output with various DC voltage levels developed by DC split capacitors. If the number of required level is given as k, the number of capacitors needed across the DC bus are (k-1), power electronic switches per phase can be calculated as 2(k-1) and the number of diodes per phase will be given as 2(k-2). This formula is mostly standard for all the diode clamped multilevel inverters. From the design formula, three level inverter requires 2 capacitors, then 4 power switches and 2 clamping diodes per phase (leg). Each of the power switches has complimentary switch pair, when a switch is turned ON then its complimentary switch should be OFF.

3.1. Coupled Inductor Based Diode Clamped Inverter

In grid-connected PV systems line transformers are placed between the conversion stage and the grid. But transformers are costly, bulky, big n size and also reduce the efficiency of the system. To overcome these problems coupled inductors are used in proposed coupled inductor diode-clamped is shown in Figure 4.

4. COUPLED INDUCTOR Z SOURCE BASED DIODE-CLAMPED

It presents a coupled inductor z source three level inverter (CI-Z-DC-TLI) in the Figure 5. Where a unique impedance network of two capacitors and two inductors connected to form an X-shaped network. The impedance network is connected to the PV input and the diode clamped circuit, its main objective is to use the shoot through and boost the voltage. Shoot through is forbidden in traditional inverters but z source inverters make it possible for the shoot through to be used to boost the voltage. The elimination of a bulky transformer will make the size smaller and cheaper. Also the control of the system and THD will improve since no dead time is required.

The CI-Z-DC-TLI has fifteen switching states whereas the traditional inverters have 9 switching states i.e eight switching states and null states. However z source inverter has seven zero states also known as a shoot through states which occur when the load is shorted by the upper and the lower switches simultaneously. This can be generated either by any of the switches of phase A-leg or B-leg or C-leg, any two combination phase ABC legs or all three phase legs. The capability of z source to buck or boost the voltage depends on the zero switching periods (t1). The boost factor can be calculated from the switching times as

$$B_f = \frac{t}{t-t_1} = \frac{1}{1-2\frac{t}{t_1}} \geq 1.0 \quad (4)$$

The modulation index (M) and the switching period (To) can be related as

$$\frac{t_1}{t} = 1 - M \quad (5)$$

Relating equation (4) and equation (5), the relationship between the boost factor and the modulation index can be deduce as follows

$$B_f = \frac{1}{2M-1} \quad (6)$$

From the above expression, the output voltage of Z-DC-TLI is calculated based on the values of modulation index (M), zero switching period (To) and boost factor (B). Therefore modulation index (M) of less than 0.5 will yield buck operation and above 0.5, but less than 1.0 will yield boost operation.

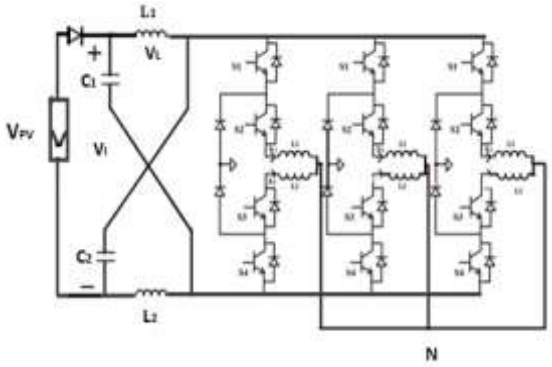


Figure 5. Coupled Inductor Z-DC-TLI

The operation of CI-Z-DC-TLI can be explained using two modes:
(i) Shoot through mode
(ii) Non shoot through mode

(i) Shoot through mode

Among the limitations of traditional inverters is the switches of the same phase leg cannot be turned on simultaneously i.e either upper and lower switches of one phase leg, two phase leg or all three phase legs. But in this mode, all the switches on a single phase leg can be ON without causing any damage to the semiconductor switches. The diode D will be reversed biased, the supply will be cut off and the operation can

be in seven different modes, when the four switches S1, S2, S3 and S4 in any of the three phase legs are ON [known as full shoot through state], or the three upper switches S1, S2 and S3 in any of the three phase legs are turned ON [known as upper shoot through state], or three lower switches S2, S3 and S4in any of the three phase leg are ON [called lower shoot through state]. During this mode, the inverter output terminals are shorted and zero output voltage goes to the load. Which only means the output voltage during shoot through is zero. The Table 1 below represents the shoot through modes of operation. Figure 6 shows the equivalent circuit for shoot through mode and the circuit can be analyzed,

$$V_L = V_C \quad (7)$$

$$V_I = 2V_C \quad (8)$$

$$V_O = 0 \quad (9)$$

Table 1. Shoot Through Modes of Operation

Modes	Leg 1	Leg 2	Leg 3
Mode 1	S1,S2 and S3 are ON while S4is OFF(upper shout through)	S1 is OFF then S2,S3 and S4 are ON (lower shoot through)	S1, S2 and S3 are ON while S4 is OFF(upper shoot through)
Mode 2	S1 is OFF then S2,S3 and S4 are ON(lower shoot through)	S1, S2, S3 are ON then S4 is OFF(upper shoot through)	S1 is OFF while S2, S3 and S4 are ON (lower shoot through)
Mode 3	S1, S2, S3 and S4 are ON (full shoot through)	S1 is OFF while S2, S3 and S4 are ON (lower shoot through)	S1, S2 and S3 are ON while S4 is OFF (upper shoot through)
Mode 4	S1, S2, S3 and S4 are all ON	S1, S2, S3 and S4 are all ON	S1, S2, and S3 are ON while S4

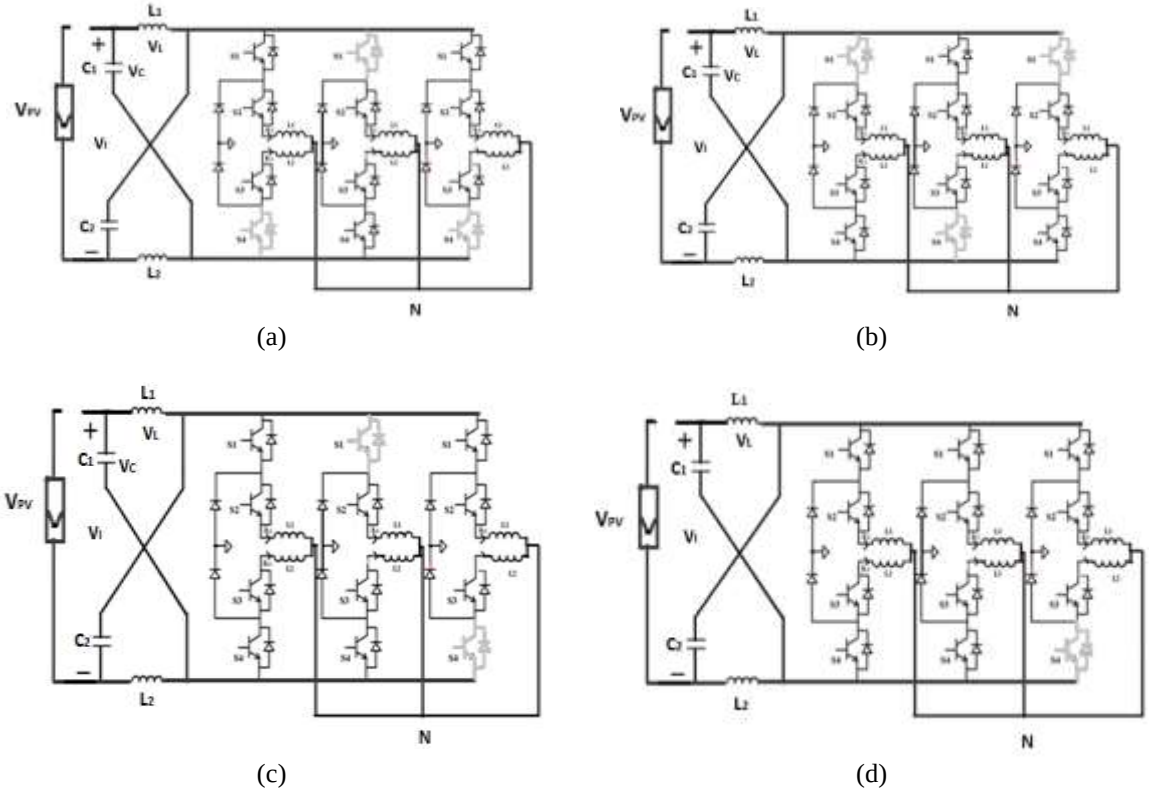


Figure 6. Shoot through Modes of Operations (a) {Ust, Lst, Ust} (b) {Lst, Ust, Lst} (c) {Fst, Lst, Fst} (d) {Fst, Fst, Ust}

(ii) Non shoot through mode

Operation in non-shoot through mode can be known as the buck operation. Where the Z-DC-TLI inverter operates as a typical diode clamped inverter where the output voltage is less than the input voltage.

The inverter will be having three different switching states, when the upper two switches are ON, when the lower two switches are gated ON and the internal two switches are turned ON

$$V_L = V_{PV} - V_C \quad (10)$$

$$V_I = V_C - V_L = 2V_C - V_O \quad (11)$$

Table 2. Non Shoot through Modes of Operation

Modes	Leg 1	Leg 2	Leg 3
Mode 1	S1 and S2 are ON then S3 and S4 are OFF	S1 and S2 are ON while S3 and S4 are OFF	S1 and S2 are ON while S2 and S4 are OFF
Mode 2	S1 and S2 are OFF while S3 and S4 are ON	S1 and S2 are OFF then S3 and S4 are ON	S1 and S2 are OFF then S3 and S4 are ON
Mode 3	S1 and S4 are OFF while S2 and S3 are ON	S1 and S4 are OFF while S2 and S3 are ON	S1 and S4 are OFF while S2 and S3 are ON
Mode 4	S1 and S2 are ON while S3 and S4 are OFF	S1 and S2 are OFF while S3 and S4 are ON	S1 and S2 are ON while S3 and S4 are OFF

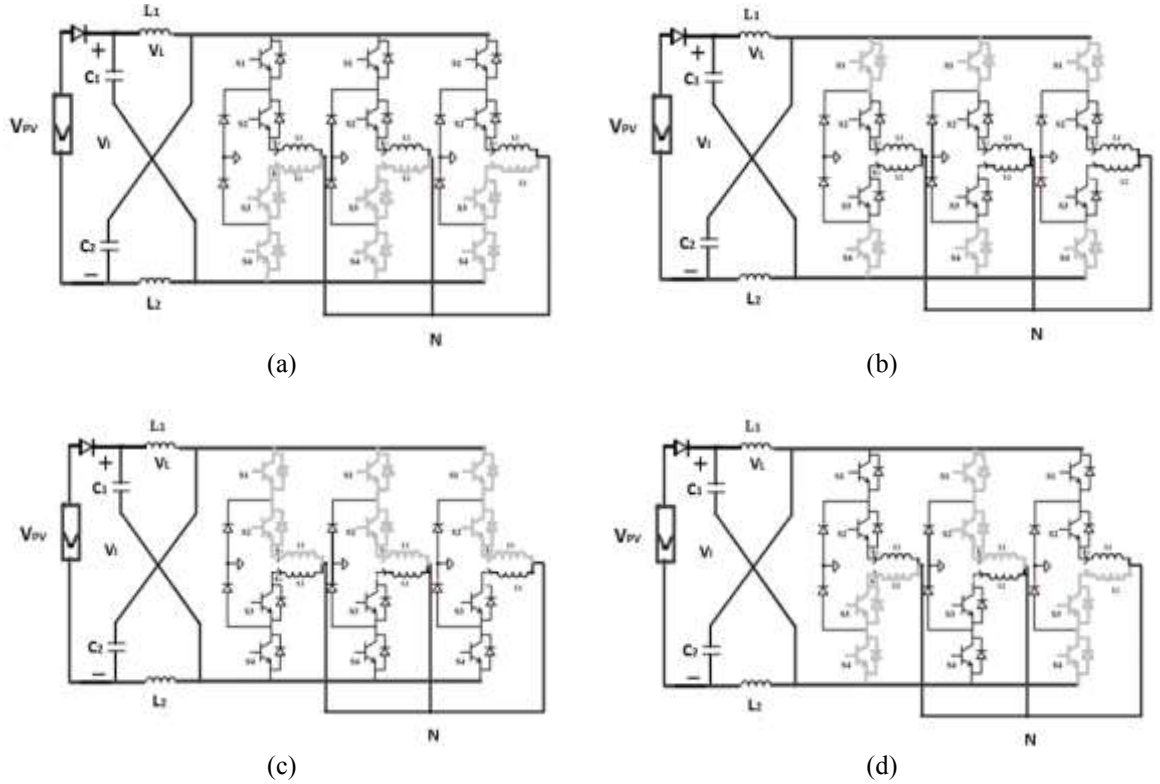


Figure 7. Non shoot through Modes of Operations (a) 111 (b) -1-1-1 (c) 000 (d) 1-11

5. HYSTERESIS SPACE VECTOR MODULATION

To ascertain that the operation of the multilevel inverter is perfect, the control system has two major tasks. The firstly correct voltage vector must be generated and secondly, the multilevel output waveform must be right. Also, the voltage across the two capacitors must be maintained. There are four blocks in the proposed Space vector current control. The first block is error calculation, second is area detection, third is sector detection, and fourth voltage-vector selection. However the main objective of proposed space vector current control is to maintain the present load current near the reference current inside the hysteresis limit. When balancing a 3 phase sinusoidal currents, the reference vector travel round along the origin. The system analysis can be carried out using α-β frame, and Figure 8 shows the transformed 3 hysteresis limit leads to 3 spherical areas.

The first area A-I is a circular boundary having a radius h_1. The second region is A-II is a circular boundary with radius h_2 and also enclosed by first circle with radius h_i and third circle with radius $h_1 + h_2$.

Then last region A-III is the circular boundary with radius $h_1 + h_2$. Firstly the values of the h_1 and $h_2$can be determine based on the reference current value and secondly on the efficient control dynamics used. If value h_1=0 is selected, this makes the switching frequency to increase when none of the zero voltage vectors are utilized. Furthermore, it makes the control of load current respond faster.

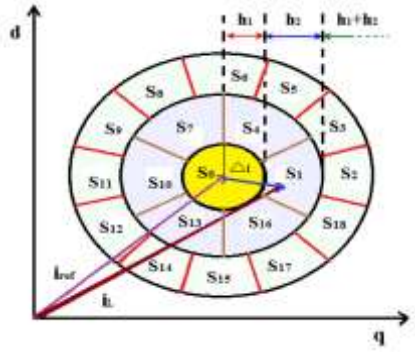


Figure 8. Error-vector tip location using hysteresis boundaries

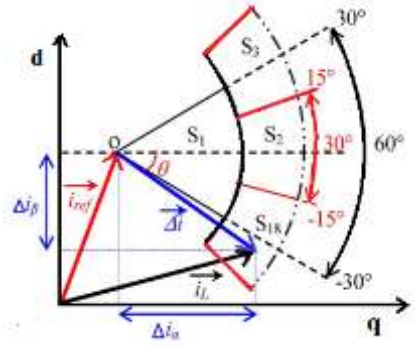


Figure 9. Angles between two adjacent sectors

Inductor current can be tracked accurately using hysteresis current control. Signals with high switching frequency must block and the inductor current must be zero, this only means the grid voltage will push the inductor current to zero. In hysteresis current control, the control method is nonlinear with high performance, stability is high also dynamic response is fast.

$$h = \frac{u_g(U_{pv}-2u_g)}{U_{pv}.L.f_s} \quad (12)$$

Where h represents hysteresis band. The two currents reference current $i_L$ref and the real current i_L can be simplified using vector components,

$$i_{Lref} = i_{Lref\alpha} + ji_{Lref\beta} \quad (13)$$

$$i_L = i_{L\alpha} + ji_{L\beta} \quad (14)$$

The error vector can be calculated as,

$$\Delta_i = i_L - i_{Lref} \quad (15)$$

It is expressed in the αβ reference frame as,

$$\Delta_i = \Delta_{i\alpha} + \Delta_{i\beta} \quad (16)$$

Areas A-I and A-II are surrounded by the hysteresis limith1 and (h_1+ h_2) respectively. However, the third area A-III with radius=(r > h_1+ h_2). Area A-I represents one sector, which is S0. Area A-II is subdivided into six sectors: S1, S4, S7, S10, S13, and S16. In Figure 9, two sequential sectors are separated apart by an angle of 60◦.

$$\theta_i = \tan\left(\frac{\Delta_{i\beta}}{\Delta_{i\alpha}}\right) \quad (17)$$

The location of the vector (Δ_i) head can be found within one among the sectors which can be based on the angle θ and area where is fall.

Table 3. Sector and Vector Representation in Various Areas

AREAS	SECTORS	VECTORS
Area 1	S_0	V_0,V_7,V_{14}
Area 2 (charge)	$S_1,S_4,S_7,S_{10},S_{13}, S_{16}$	V_1,V_2,V_3,V_4,V_5,V_6
Area 2 (discharge)	$S_1,S_4,S_7,S_{10},S_{13}, S_{16}$	$V_{21},V_{22},V_{23},V_{24},V_{25}, V_{26}$
Area 3	$S_2,S_3,S_5,S_6,S_8,S_9,S_{11},S_{12},S_{14},S_{15},S_{17}, S_{18}$	$V_8,V_9,V_{10},V_{11},V_{12},V_{13},$ $V_{15},V_{16},V_{17},V_{18},V_{19},V_{20}$

6. SIMULATION RESULT

Simulation of hysteresis SVM based transformerless coupled inductor z source DC-TLI grid connected Photovoltaic system was carried out using SIMULINK with the following parameters in Table 4. The projected system was simulated using MATLAB/SIMULINK is shown in Figure 10. The PV array output power of 747 W and MPPT was represented in Figure 11 and Figure 12 respectively. Figure 13 shows that the proposed system CI-Z-DC-TLI produces an output voltage of 566V which just displays the boosting capability of the Z-DC-TLI. In Figure 14 shows the comparison between the actual and reference current to generate gate pulses to NPC-TLI. CI-NPC-inverter output current for the proposed system is shown in Figure 15. Harmonic analysis for output voltage and current of CI-NPC-TLI shown in Figure 16. Coupled inductor currents value iL12 analyzed by adding iL1 (positive) and iL2 (negative). The current was improved to 55.79A as shown in Figure 15. For operating CI-NPC-TLI, gate pulses generating by using hysteresis SVM and sector identification for SVM and magnitude identification for sector selection shown in Figure 18 & 19 respectively.

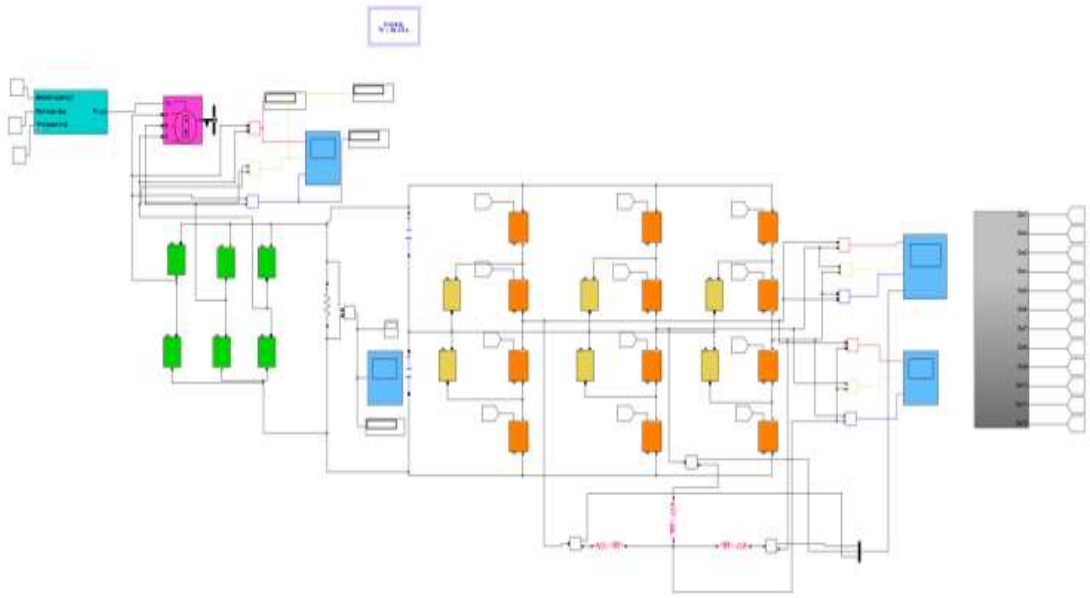


Figure 10. Simulation Diagram of Three Level z Source NPC

Table 4. Simulation Parameters

Parameters	Value
PV voltage	98V
Capacitors	270µF
Inductors	4mH
Switching Frequency	10Khz
Grid voltage	300V

Using the PV output as input to Z-DC-TLI, the proposed system is expected to be able to boost and improve the voltage and efficiency of the system.

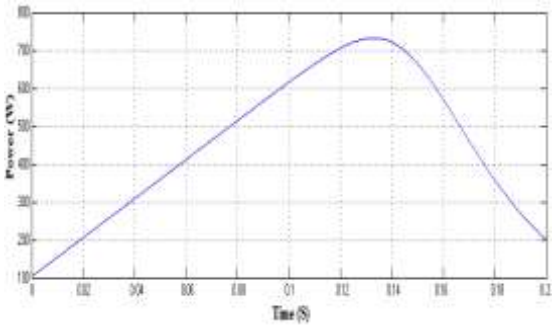


Figure 11. PV array Output Power

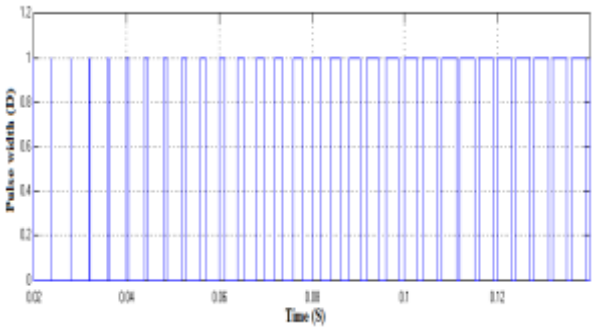


Figure 12. Output Pulses of MPPT

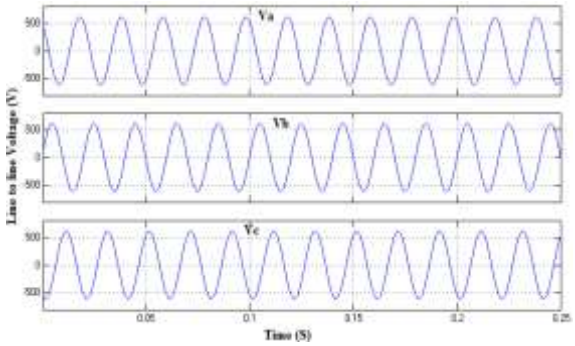


Figure 13. CI-Z-DC-TLI Output Waveform

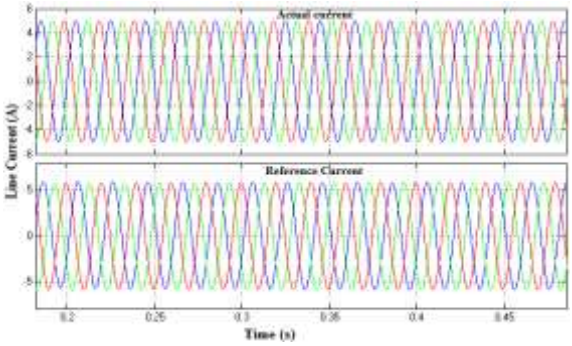


Figure 14. Comparison between Actual Current and Reference Current

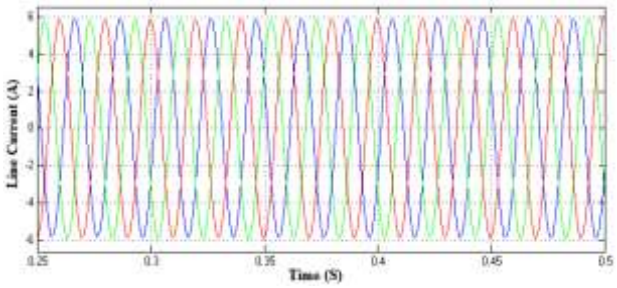
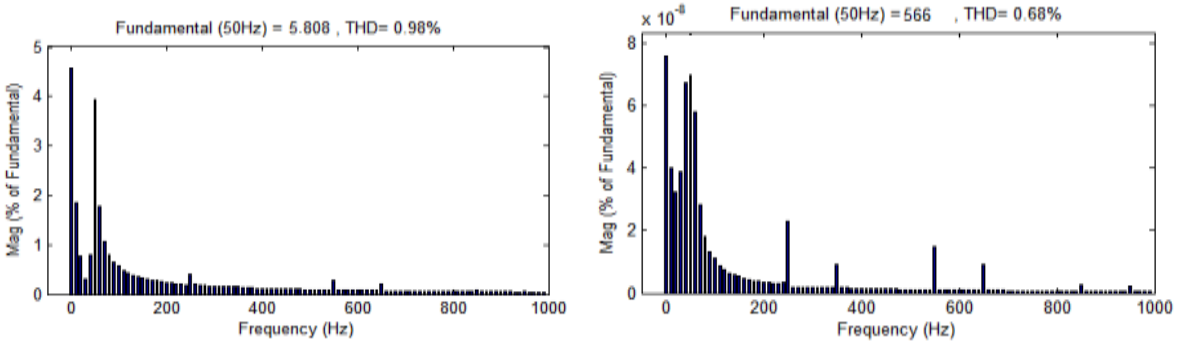


Figure 15. CI-NPC-inverter Output Current for the Proposed System



(a) (b)

Figure 16. Harmonic Spectrum Analysis for inverter (a) Output Current (b) Output Voltage

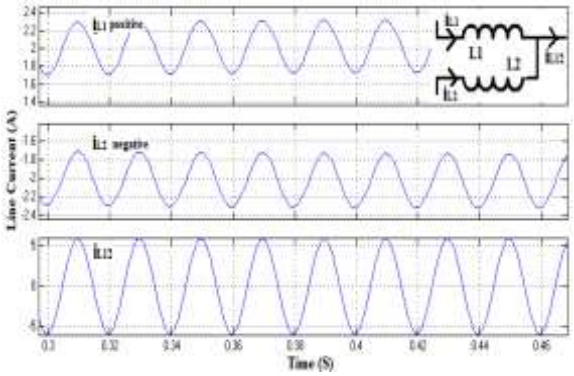


Figure 17. Coupled inductor currents value comparison

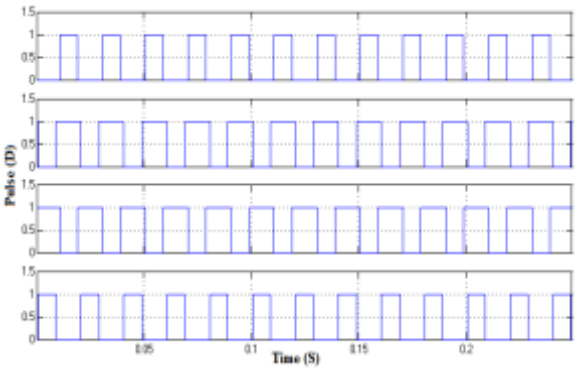


Figure 18. Gate pulses for inverter using SVM

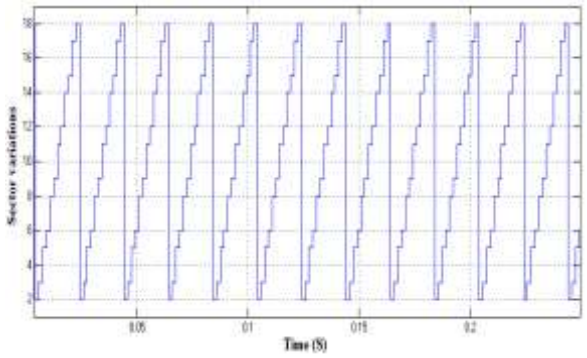


Figure 19. Sector Identification for SVM

7. EXPERIMENTAL RESULTS

An experimental step up carried out using the same simulation parameters were the diode clamped three level was connected using PV panel as the input to the multilevel inverter, a boost converter was used to boost the voltage to a desired voltage and the output was taken from DSO in Figure 21. AN IRF 840 MOSFET was used for the inverter legs switches and a DSPIC38F microcontroller fed with 5V dc voltage was used to implement SVPWM.

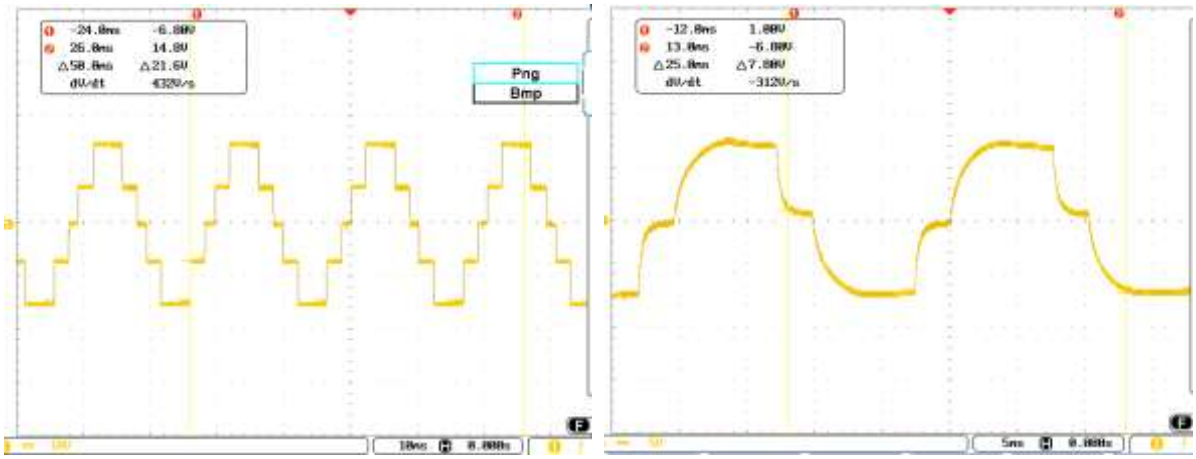


Figure 20. Output voltage of z source diode clamped 3-level inverter

Figure 21. Experimental setup of proposed system

8. CONCLUSION

The proposed system was implemented and simulated using FPGA controller and MATLAB environment, and it was observed that the overall efficiency and reliability of the system was improved by avoiding the shoot through risks. The Z-DC- TLI was able to boost the voltage using shoot through states which are forbidden in traditional inverters. Elimination of boost converter at the inverter output and the transformer from the proposed system reduces the cost, losses and improve its reliability. Its produces improved output voltage and better current control. And which avoids the capacitor balancing problem and common mode voltage of z-source diode clamped multilevel inverter.

a. From the proposed system the THD of output voltage is 0.0 % and for current is 1.24 %, which is less then IEEE standard value.
b. In future work, Hysteresis SVM will be replaced by 3-Dimensional Space Vector Modulation.

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