International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 7, No. 4, December 2016, pp. 1233~1239
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v7i4.pp1233-1239

Single-phase Multilevel Inverter with Simpler Basic Unit Cells for Photovoltaic Power Generation

M.S. Chye[1], J.A. Soo[2], Y.C. Tan[3], M. Aizuddin[4], S. Lee[5], M. Faddle[6], S.L. Ong[7], T. Sutikno[8], J.H. Leong[9]
[1-7,9]School of Electrical Systems Engineering, Universiti Malaysia Perlis (UniMAP), Perlis, Malaysia
[8]Department of Electrical Engineering, Universitas Ahmad Dahlan, Yogyakarta, Indonesia

Article Info

Article history:

Received Apr 7, 2016
Revised Nov 12, 2016
Accepted Nov 24, 2016

Keyword:

CHBMI
DSM
MLI
PV
THD

ABSTRACT

This paper presents a single-phase multilevel inverter (MLI) with simpler basic unit cells. The proposed MLI is able to operate in two modes, i.e. charge mode to charge the batteries, and inverter mode to supply AC power to load, and therefore, it is inherently suitable for photovoltaic (PV) power generation applications. The proposed MLI requires lower number of power MOSFETs and gate driver units, which will translate into higher cost saving and better system reliability. The power MOSFETs in the basic unit cells and H-bridge module are switched at near fundamental frequency, i.e. 100 Hz and 50 Hz, respectively, resulting in lower switching losses. For low total harmonic distortion (THD) operation, a deep scanning method is employed to calculate the switching angles of the MLI. The lowest THD obtained is 8.91% at modulation index of 0.82. The performance of the proposed MLI (9-level) has been simulated and evaluated experimentally. The simulation and experimental results are in good agreement and this confirms that the proposed MLI is able to produce an AC output voltage with low THD.

Corresponding Author:

J.H. Leong,
School of Electrical Systems Engineering,
Universiti Malaysia Perlis,
Pauh Putra Campus, 02600 Arau, Perlis, Malaysia.
Email : nick.unimap@gmail.com

1. INTRODUCTION

Electricity generation using fossil fuels such as coal, oil and natural gas has caused environmental deterioration [1]. Besides damaging the environment, these fossil fuel sources are limited and estimated to deplete before the next century [2]. Hence, electric power generation relying mainly on fossil fuels is expected to be unsustainable and insecure. To address this issue, various power generation techniques using renewable energy sources have been explored and developed recently. Among the renewable energy sources, solar energy is probably one of the most promising sources as it is clean, inexhaustible and widely available [3]. The solar energy can be harvested using photovoltaic (PV) modules. However, the direct current (DC) produced by the PV modules is incompatible with standard electrical appliances which are powered by alternating current (AC) [4]. Therefore, an inverter is required to convert the DC into AC. Many inverter topologies have been proposed in the past and multilevel inverter (MLI) is one of the preferred topologies [6]-[7].

In general, multilevel inverters can be classified into three major families that are diode-clamped, flying-capacitor and cascaded H-bridge [8]. The main drawback of diode-clamped multilevel inverter is the unequal capacitor voltages among the series connected capacitors, and hence, the difficulty in balancing the capacitor voltages poses a major design challenge for this topology. The flying capacitor topologies provide switch combination redundancy for balancing at different voltage levels. This feature allows the switching stresses to be equally distributed between the active switches [9]. However, this topology is bulky due to the

requirement of large number of storage electrolytic capacitors. As compared to flying capacitor topology, the conventional cascaded H-bridge multilevel inverter (CHBMI) does not require large number of storage capacitor [6]. Figure 1 shows the block diagram of a conventional single-phase CHBMI for standalone PV power generation. Each H-bridge requires a separate DC source and also an independent maximum power point tracking (MPPT) charge controller. The system requires a high number of components, and hence, it can be very bulky and costly. To address this issue, a single-phase multilevel inverter with simpler basic unit cells for standalone PV power generation is proposed in this paper.

2. PROPOSED TOPOLOGY

Figure 2 shows the proposed MLI in a PV power generation system. It consists of a PV module, a MPPT charge controller, a double-throw relay (DTR), *N* number of cascaded basic cells and an H-bridge module at the output, whilst each basic cell contains a power MOSFET, a diode, a single-throw relay (STR) and a storage battery as the DC source. The proposed topology can be configured to operate in two modes, i.e. the charge mode for charging the batteries and the inverter mode that produces an AC staircase output voltage. In the charging mode, the storage batteries of all basic cells are connected in parallel to the MPPT charge controller via the DTR as shown in Figure 3, and the energy produced by the PV module is stored in the batteries. During charging, the STRs and power MOSFETs in basic cells are in on state and in off state, respectively. Once the storage batteries are fully charged, the proposed topology can be configured as an inverter to produce AC power for standard electrical appliances. Figure 4 shows the equivalent circuit in inverter mode. In this mode, the MPPT charge controller is disconnected from the converter and all STRs are open. The power MOSFETs in each basic cells are switched on and off in a specific sequential pattern to produce a *N*-step staircase DC bus voltage waveform (V_{bus}) as shown in Figure 5(a). The peak voltage of NV_B can be achieved when *N* basic cells are activated. The staircase AC voltage waveform (V_{out}) shown in Figure 5(b) is produced by using the H-bridge module. During the positive half cycle from 0 to π, Q_1 and Q_4 are turned on, and during the negative half cycle, Q_2 and Q_3 are turned on which alternates the voltage polarity. The switching sequences during the inverter mode are summarized in Table 1. In the proposed topology, the power MOSFETs in the basic unit cells and H-bridge module are switched at 100 Hz and 50 Hz, respectively. Hence, the low switching frequency results in lower switching losses compared to conventional pulse width modulation (PWM) controlled inverters which operate at a much higher frequency than the fundamental AC frequency [10].

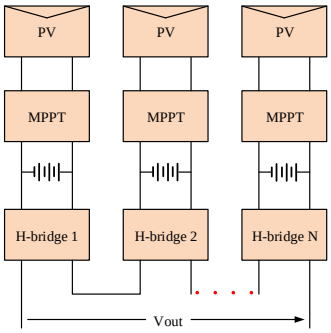


Figure 1. Block diagram of conventional single-phase CHBMI

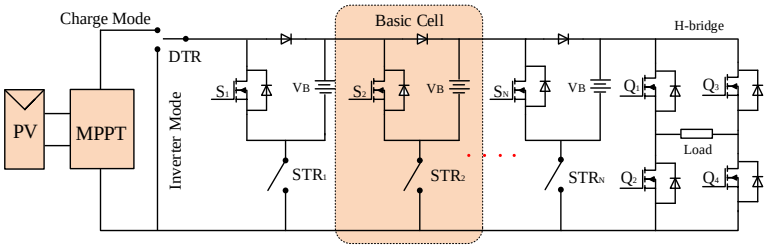


Figure 2. Schematic diagram of proposed multilevel inverter in PV power generation system

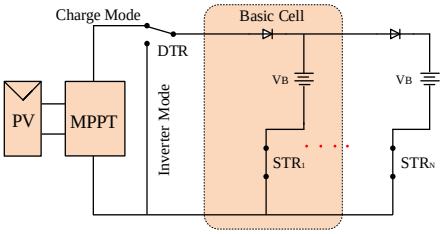


Figure 3. Equivalent circuit during charge mode

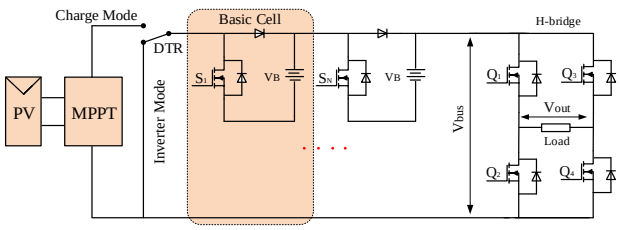
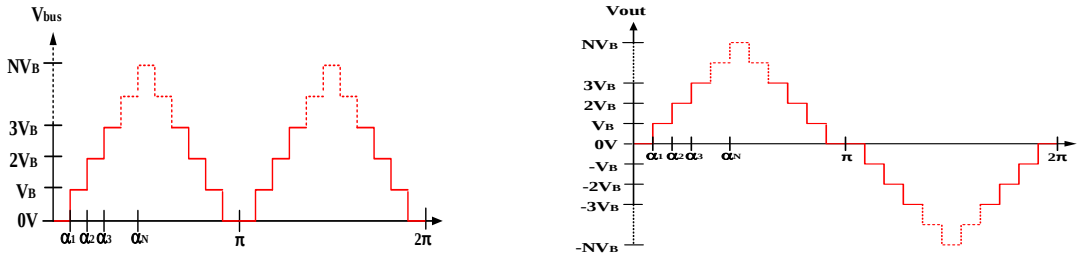


Figure 4. Equivalent circuit during inverter mode



(a) (b)

Figure 5. (a) DC bus voltage waveform and (b) output AC voltage waveform

Figure 6 shows the number of power MOSFETs required for conventional CHBMI and the proposed MLI. As the number of voltage level increases, the required number of power MOSFETs (and hence the required number of gate drivers) for the proposed MLI is significantly lower compared to that of CHBMI. For example a 15-level CHBMI requires 28 power switches, whilst a 15-level proposed MLI requires only 11 power switches.

Table 1. Switching States During Inverter Mode (9-Level Output Voltage)

Vout	S_1	S_2	S_3	S_4	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0	0	0	0
V_B	1	0	0	0	1	0	0	1
$2V_B$	1	1	0	0	1	0	0	1
$3V_B$	1	1	1	0	1	0	0	1
$4V_B$	1	1	1	1	1	0	0	1
$-V_B$	1	0	0	0	0	1	1	0
$-2V_B$	1	1	0	0	0	1	1	0
$-3V_B$	1	1	1	0	0	1	1	0
$-4V_B$	1	1	1	1	0	1	1	0

Note: "0" is OFF, "1" is ON

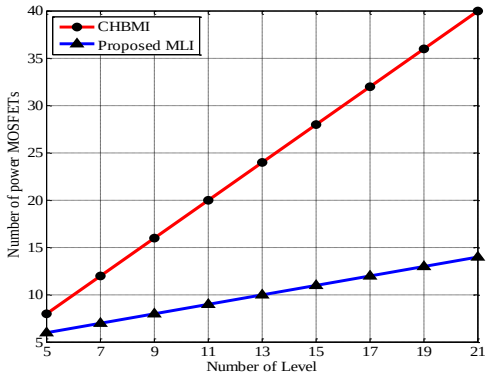


Figure 6. Comparison of number of power MOSFETs required for conventional CHBMI and proposed MLI

The number of the voltage level produced by the proposed MLI is given by

$$n = 2N + 1 \tag{1}$$

where N is the number of basic cells and the required number of power MOSFETs is given by

$$Number\ of\ MOSFETs = \frac{n-1}{2} + 4 \tag{2}$$

3. CALCULATION OF SWITCHING ANGLES

In designing a MLI, the switching angle has to be carefully selected to yield an output voltage waveform with low THD. Various switching angle derivation techniques have been proposed in the past, e.g. selective harmonic elimination, resultant theory, space-vector PWM, etc. [11]-[13]. In this paper, a deep scanning method (DSM) is applied to find the switching angles. By using MATLAB, the DSM algorithm scans nearly all possible switching angles from 0º to 90º. The modulation index (M_i) and THD of the output voltage waveform are calculated as follows:

$$M_i = \frac{\pi}{4}\frac{V_1}{V_{total}} \tag{3}$$

$$THD = \sqrt{\frac{\sum_{n=3,5,7...} V_n^2}{V_1^2}} \quad (4)$$

where V_1 is the fundamental voltage , V_{total} is the sum of all DC source voltages, and V_n is the amplitude of the *n*-th order voltage harmonic. Once the scanning is complete, the lowest THD and the respective set of switching angles at different modulation indexes are extracted from the scanning results. Figure 7 shows the THD versus modulation index from M_i = 0.2 to 0.9. The lowest THD, i.e. 8.91%, is at M_i = 0.82, which can be achieved using switching angles of θ_1 = 7º, θ_2 = 21º, θ_3 = 36º and θ_4 = 56º.

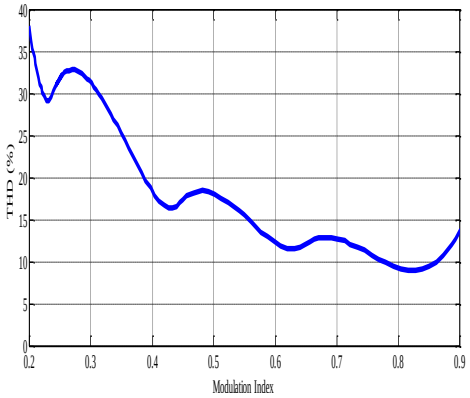


Figure 7. THD of output AC voltage waveform of proposed MLI (n = 9)

4. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed MLI has been simulated using PSIM software. Figure 8 shows the equivalent schematic circuit diagram of a 9-level MLI operating in inverter mode. Each power MOSFET in the simulation is driven using a switch gating block. Two switching patterns, namely SPA and SPB, were tested. In the case with SPA, the switching angles are arranged to be equally spaced. Whilst for SPB, the switching angles are selected based on the scanning results obtained in previous section. The output voltage waveforms of the proposed MLI using SPA and SPB are shown in Figures 9(a) and 9(b), respectively. Note that the fundamental output voltages (and therefore the modulation indexes) in both SPA and SPB simulations are set to be identical. The Fast Fourier transform (FFT) of both output voltage waveforms resulted using SPA and SPB patterns are compared in Figure 9(c). As can be observed in the figure, the SPB switching pattern produces an output voltage waveform with lower THD. The reason for this is because the SPB switching pattern produces an output staircase AC voltage that resembles a sinusoidal waveform better than SPA.

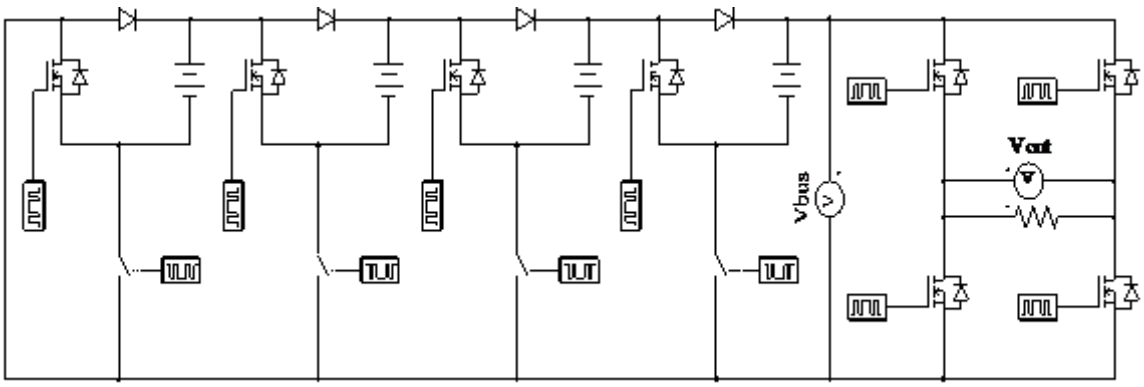
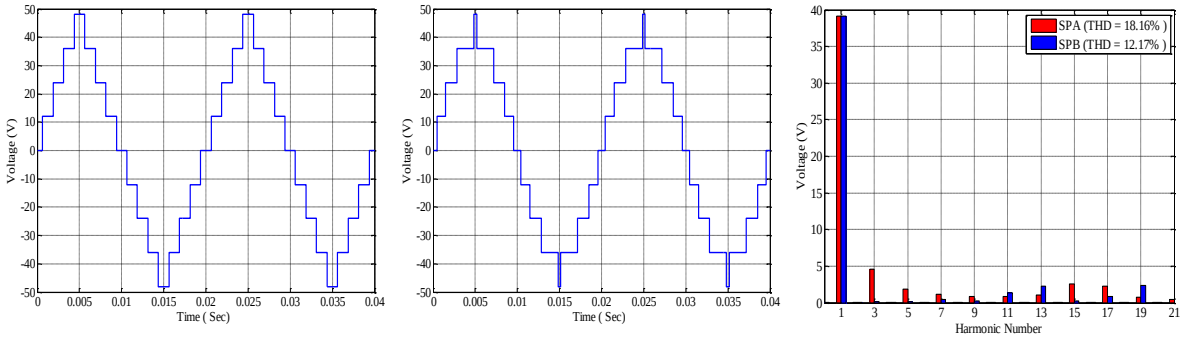


Figure 8. PSIM simulation model of proposed 9-level MLI

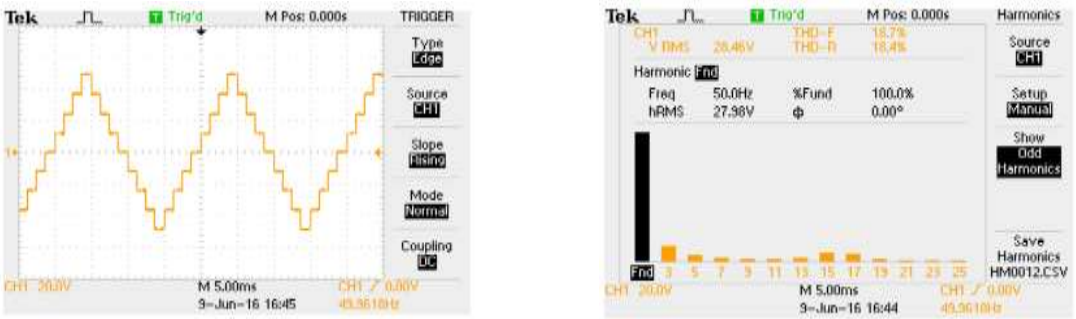


(a) (b) (c)

Figure 9. Output AC voltage waveforms using (a) SPA and (b) SPB, (c) FFT of output voltage waveforms

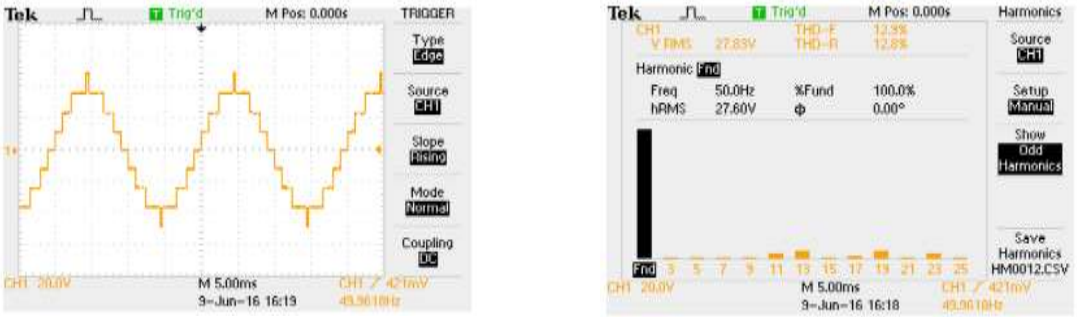
Figure 10 shows the proposed MLI prototype (n=9) controlled by using a Microchip PIC16F877A microcontroller. The DC sources of each basic cell are powered by a 12 V DC source. Figure 11 shows the experimental output voltage waveform and its FFT waveform when SPA is applied. The THD of the output voltage waveform is approximately 18.7%, which is close to that predicted by simulation. Figure 12 shows the output voltage waveform and its FFT waveform when SPB is applied. As compared to the experimental result in Figure 11, SPB switching pattern is again confirmed to be able to produce an output voltage waveform with lower THD. Figure 13 shows the experimental output voltage waveform and its FFT plot at M_i=0.82. The measured THD is 8.94%, which is very close to the lowest THD obtained using the DSM.

Figure 10. Proposed 9-level MLI prototype



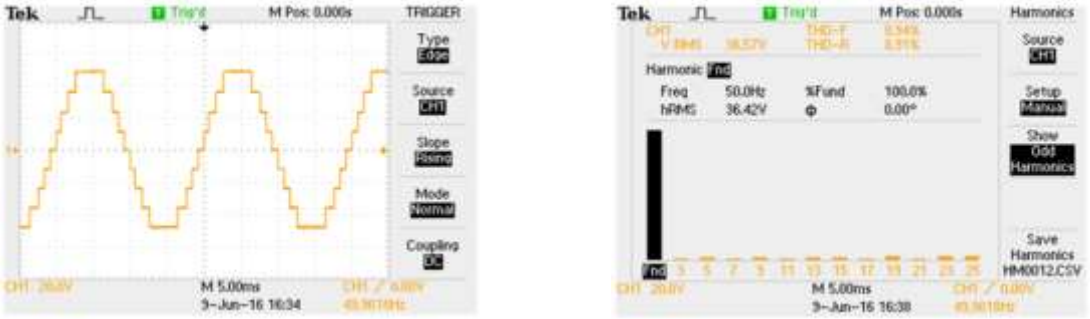
(a) (b)

Figure 11. (a) Output AC voltage waveform using SPA and (b) the respective FFT plot



(a) (b)

Figure 12. (a) Output AC voltage waveform using SPB and (b) the respective FFT plot



(a) (b)

Figure 13. (a) Output AC voltage waveforms and (b) the respective FFT plot at M_i = 0.82 (THD = 8.94%)

5. CONCLUSION

In this paper, a single-phase MLI with simpler basic unit cells for standalone PV power generation is proposed. The proposed topology can be configured to operate either in charge mode or inverter mode which makes it suitable for solar PV applications. As compared to conventional CHBMI, the proposed MLI requires lower number of power MOSFETs and gate driver units, and therefore making the inverter more compact, reliable and cheaper. The performance of the proposed MLI have been simulated and evaluated experimentally. The simulation and experimental results are in good agreement and this comfirms that the proposed MLI is able to produce an AC output voltage with low THD.

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