International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 7, No. 2, June 2016, pp. 340~348
ISSN: 2088-8694

FPGA Based Design and Validation of Asymmetrical Reduced Switch Multilevel Inverter

C. Bharatiraja, Harshavardhan Reddy, N. Sri Ramsai, Sunkavalli Satya Saisuma
Departement of Electrical and Electronics Engineering, SRM University, India

Article Info

Article history:

Received Jul 31, 2015
Revised Jan 29, 2015
Accepted Feb 16, 2016

Keyword:

Field programmable gate array
Multilevel inverter
Pulse width modulation
Reduced switch MLI
total harmonic distortion

ABSTRACT

This paper proposes a new Asymmetrical multilevel inverter topology with reduced number of switches. This topology is superior to the existing multilevel inverter (MLI) configurations in terms of lower total harmonic distortion (THD) value and lower cost. The idea incorporates a new module setup comprising of four different voltage sources having voltage output levels in a specific ratio. The proposed topology uses a novel pulse width modulation (PWM) technique (as presented) to control the gating pulses. The operation is simulated using MATLAB/SIMULINK and its results are validated through FPGA Spartan 3 based hardware prototype inverter (using three voltage sources to produce a 7 level output, which may be extended to 15 level). The circuit complexity is drastically reduced and it is suitable for medium and high power applications. THD for the output is quite low when compared with the conventional inverter.

Corresponding Author:

C. Bharatiraja,
Departement of Electrical and Electronics Engineering, SRM University, India
Email: bharatiraja@gmail.com

1. INTRODUCTION

Multilevel inverters are generally used for DC-AC conversion since they have nearly sinusoidal output voltage waveforms and an improved harmonic profile of the output current [1]. There is a reduction in the commutation frequency applied to the switching components, switching losses as well as in the voltages applied to the main power switches, enabling operation at higher load voltages without the use of transformers or filter circuits [2]. Transient voltages are automatically limited. Common topologies proposed for multilevel inverters are flying capacitor, diode clamped, cascaded H-bridge and modified H-bridge [3].

However, there are certain disadvantages associated with the multilevel inverter configurations. First, they also require a great number of auxiliary dc levels, provided by independent supplies. Second is their circuit complexity, requiring a high number of power switches that must be commutated in a precisely determined sequence by a dedicated (and complex) modulator circuit. The high number of switches also increases the probability of failure of one of the switches in the circuit. Therefore, decreasing the number of switches in a MLI configuration has been a prominent aim in recent times and many topologies have been invented with the aim of doing so. [4], [5], [6] and [7] provide some such topologies. [5] Presents a structure with reduced number of switches and reduction in THD. However, the number of DC sources must be equal to the number of output levels, N_{level}. [6] Reduces the number of active elements in the system, but requires a transistor for each voltage source, thereby additionally incurring losses at each of the transistors. [8] Presents a "series-connected sub multilevel converters blocks" to produce multilevel output but needs a control circuitry of increased complexity.

This paper deals with the development of a novel single phase fifteen level H-bridge multilevel inverter that has four front end control Switches S1, S2, S3 and S4 and a single H-bridge inverter. The proposed Multilevel Inverter Topology has more advantages than the existing topologies as the number of switching devices and Total Harmonic Distortion are reduced. Therefore the switching losses are also

reduced, increasing the efficiency of the output. [9], [10] and [11] describe the generation of multilevel output with a direct more number of switches that which is proposed. The proposed multilevel inverter overcomes all these disadvantages while being more compact. Carrier based Pulse Width Modulation (PWM) techniques are currently widely used due to their reduced computational requirement, simplicity and robustness [12]. A novel PWM technique has been implemented which makes use of 15 carrier signals compared with a reference signal which is fed to a 16-4 priority encoder to control the switching. The proposed topology is evaluated by simulation and hardware implementation. The simulation is carried out in MATLAB R2011a and the hardware implementation is carried out in a Xilinx based system generator facility in union with a FPGA based processor [13].

2. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed MLI generated fifteen level output without using bidirectional switches and capacitors. It consisted of four sources and diodes connected in between the switches S_1, S_2, S_3, andS_4 as shown in the Figure 1. The sources V_1, V_2, V_3 and V_4 generate voltages in the ratio 8:4:2:1 respectively. The H-Bridge inverter uses the four sources in series as its voltage source. The sources V_1-V_4 can be connected or disconnected using the switches S_1-S_4 respectively for producing different voltage levels. Switches S_5-$S_6$are used to control the direction of current flow and hence produces alternating output across the load. For the generation of 15 level output, an Diode clamped MLI requires 24 Switching devices, 60 diodes and 12 dc link capacitors whereas in the proposed topology, it requires only 8 switching devices and 4 diodes to generate same fifteen level output, the details of which are shown in Table 1.

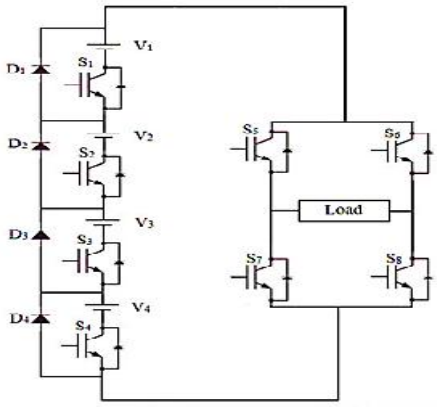

Figure 1. Proposed multilevel inverter topology

Table 1. Comparison of the per phase proposed topology with the conventional topologies

N_{level}	Components	Conventional Topologies				**Proposed Topology**
		Diode Clamped	Flying Capacitor	Cascaded Bridge	Referenced Topology	
15	Dc sources	1	1	7	1	**4**
	Dc link capacitor	12	12	-	-	**-**
	Diodes	60	-	-	12	**4**
	Clamping capacitors	-	30	-	-	**-**
	Switching devices (IGBT)	24	24	28	11	**8**

Considering the maximum dc link voltage level as $V_{dc,}$ the inverter produced fifteen output-voltage levels (V_{dc}/15, $2V_{dc}$/15, $3V_{dc}$/15, $4V_{dc}$/15, $5V_{dc}$/15, $6V_{dc}$/15, $7V_{dc}$/15, $8V_{dc}$/15, $9V_{dc}$/15, $10V_{dc}$/15, $11V_{dc}$/15, $12V_{dc}$/15, $13V_{dc}$/15, $14V_{dc}$/15, V_{dc}) from the dc supply voltage.

The operation is divided into 15 modes having different voltage levels. Considering the variable 'm', Mode m will have the voltage level of (m-1)V_{dc}/15. The switching states of the 15 modes are illustrated by Figure (2.1-2.15). The same voltage levels are obtained in negative as well.

The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switches, power diodes, and less capacitor for inverters of the same number of level [14].

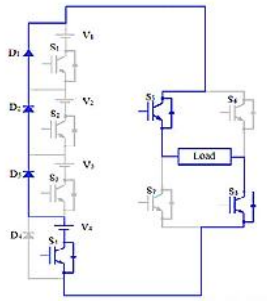

Figure 2.1. Mode I

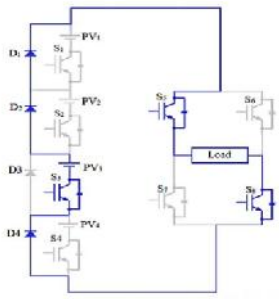

Figure 2.2. Mode II

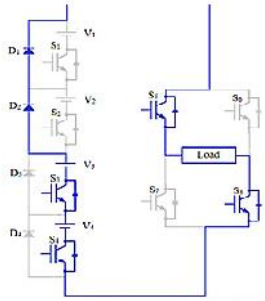

Figure 2.3. Mode III

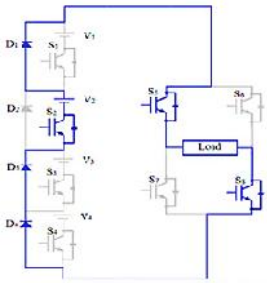

Figure 2.4. Mode IV

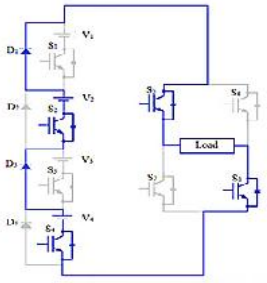

Figure 2.5. Mode V

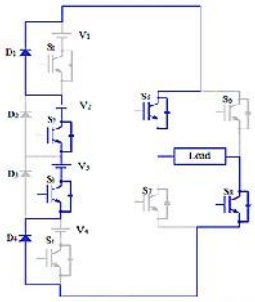

Figure 2.6. Mode VI

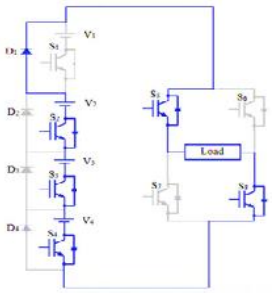

Figure 2.7. Mode VII

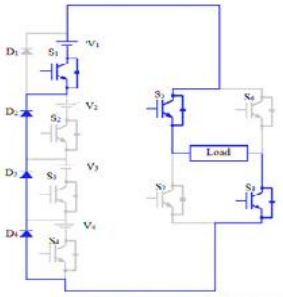

Figure 2.8. Mode VIII

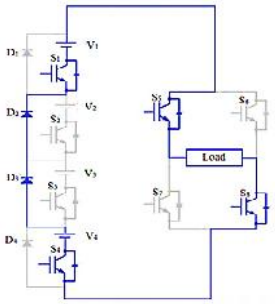

Figure 2.9. Mode IX

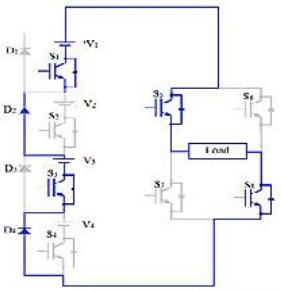

Figure 2.10. Mode X

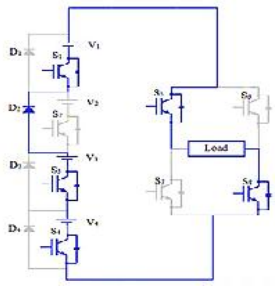

Figure 2.11. Mode XI

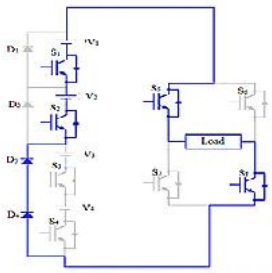

Figure 2.12. Mode XII

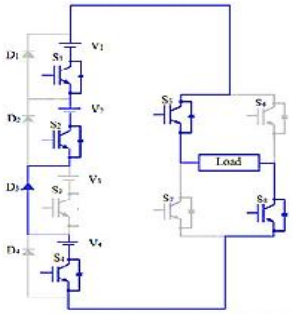

Figure 2.13. Mode XIII

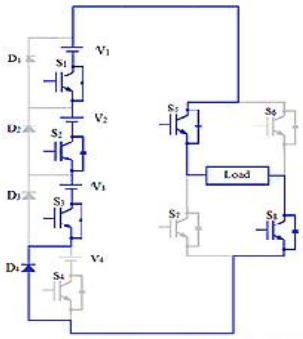

Figure 2.14. Mode XIV

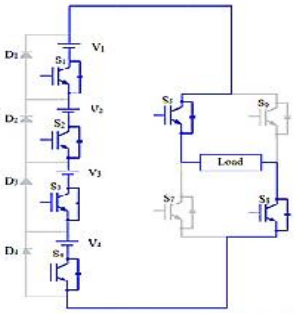

Figure 2.15. Mode XV

Figures 2.1 – 2.15. Show the various modes of operation of producing the DC link voltage

The switching sequence to the switches S_1, S_2, S_3, S_4 are given by a "Binary Logic", in which the digits in the binary system are formed such as 0000 to 1111. '0' indicates that the switch is in OFF condition and '1' indicates that Switch is in ON. This logic is explained in the next section. Based on this condition the

switching sequence to the front end IGBT's are fired, which generates the multilevel waveforms. The positive levels are attained when switches S_5 and S_8 are ON and switches S_6 and S_7 are OFF and similarly, negative levels are attained when switches S_6 and S_7 are ON and S_5 and S_8 are OFF respectively. The Switching pulses for the H-Bridge IGBTs are controlled by normal sinusoidal pulse width modulation technique, in which pair of IGBTs is fired simultaneously to obtain positive and negative cycle waveforms.

3. PROPOSED PWM TECHNIQUES

It is necessary to supply switching pulses to 8 switches in the circuit – 4(S_1, S_2, S_3 and S_4) that produce the DC Link voltage and 4 (S_5, S_6, S_7 and S_8) in the H bridge inverter circuit. Different PWM techniques are used here for each. For S5-S8, we use the normal SPWM technique. For generating the firing pulses for the switches S1-S4, a novel PWM technique is described. In this technique, there is one reference sine waveform, V_{ref} and 15 triangular carrier waves ($V_{Car1} - V_{Car15}$), each of much higher frequency than that of V_{ref}, as shown in Figure 3. In Figure 3, the topmost career wave is V_{car15} and the bottommost is V_{car1}. Each of the carrier waves is compared with the reference wave $V_{ref.}$ If the carrier signal's instantaneous value is less than that of the reference value, the comparator output is high. The outputs of the comparator values are tabulated in Table 3. These outputs are fed to a 16-to-4 bit Priority Encoder; the output bits act as the trigger pulses for switches S1-S4 as show (in Table 3). For example, consider the instant of time at which the output is $13V_{dc}/15$ – S4-ON, S3-ON, S2-OFF, S1-ON. This is the instant at which the value if V_{car13} becomes lesser than $V_{ref.}$ Therefore the encoder produces the value "1101", fed to the switches. Thus the switches S1-S4 switch at the rate of carrier signals. The firing pulses of the switches S1-S4 are shown in Figure 4.

Table 2 provides an insight about four arbitrary time frames of the waveform.The Switching Pulses given to the H-bridge IGBT's are controlled by normal SPWM. When a pair of switches is ON the other switches are OFF and vice-versa. When S_5 and S_8 are ON positive half of the waveform is generated and when S_6 and S_7 are ON, the negative half of waveform is formed. The firing pulses of the H-bridge are shown in Figure 5.

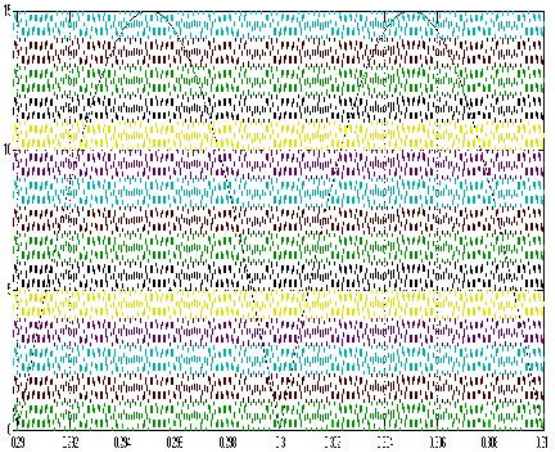

Figure 3. Carrier and Reference waveforms

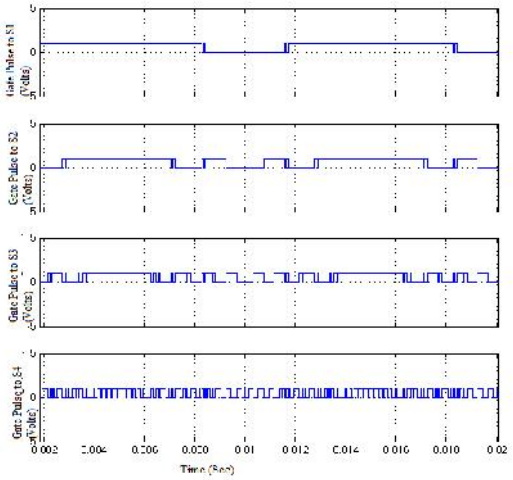

Figure 4. Firing Pulses to Switches S_1, S_2, S_3 and S_4

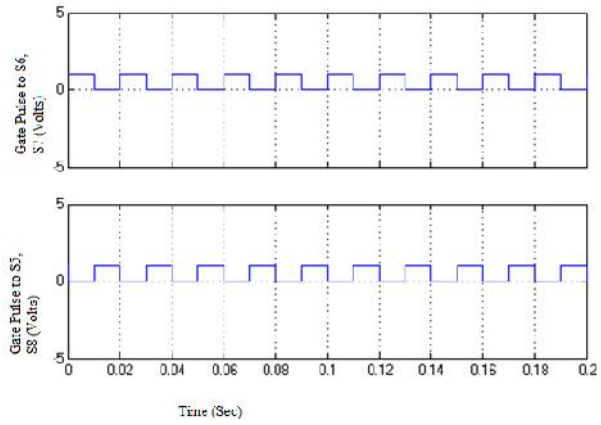

Figure 5. Firing Pulses to Switches S_5, S_6, S_7 and S_8

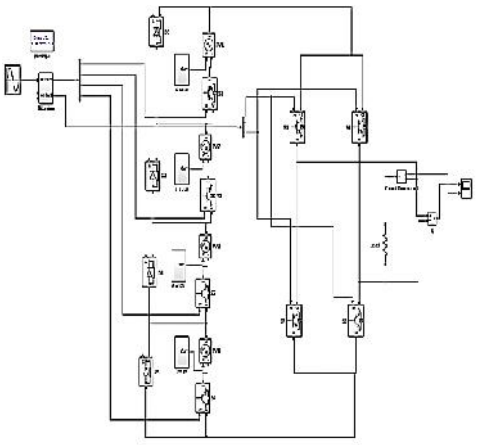

Figure 6. Simulink circuit of the proposed multilevel topology inverter

Table 2. Some timeframes of the switching pulses of S_1-S, shown in figure 5

Time	**S1**	**S2**	**S3**	**S4**	**DC Link Voltage**
0.002	1	0	0	0	$8V_{dc}/15$
0.004	1	1	1	1	V_{dc}
0.008	1	0	0	1	$9V_{dc}/15$
0.010	0	0	0	1	$V_{dc}/15$

4. SIMULATION

The proposed topology is simulated in MATLAB/SIMULINK R2011a. Figure 6 shows the simulated circuit. It consists of four front end IGBT's (S1-S4) which are connected with a four DC voltage sources rating V1=40V, V2=20V, V3=10V, V4=5V and diodes are connected to them as shown in the circuit. It also consists of four IGBT's which are connected in an H-bridge model as shown in the circuit.

Table 3. Truth Table for 15-to-4 Priority Encoder – 'X' represents a Don't Care Condition

	Inputs														**Outputs**			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	S1	S2	S3	S4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	X	X	X	X	0	1	0	1
0	0	0	0	0	0	0	0	0	1	X	X	X	X	X	0	1	1	0
0	0	0	0	0	0	0	0	1	X	X	X	X	X	X	0	1	1	1
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	1	0	0	0
0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	1	0	0	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	1	0	1	0
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	1	0	1	1
0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	1	1	0	0
0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0	1
0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1

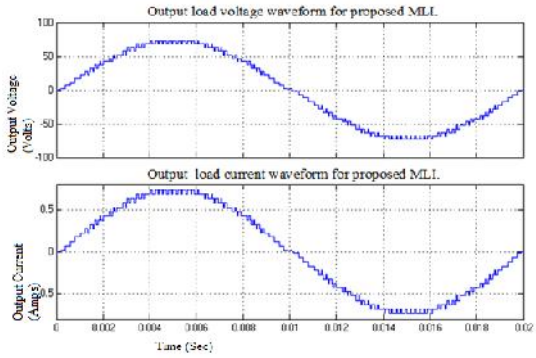

Figure 7. Output voltage and current waveform for proposed MLI

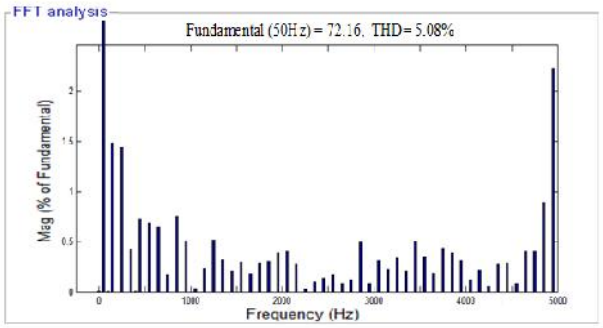

Figure 8. FFT Analysis for load voltage of proposed MLI

The Switching pulses are given to the H Bridge circuit by normal sinusoidal pulse width modulation technique (for the generation of positive and negative cycles). The switching pulses for the frontend IGBT's are given by the binary priority encoder logic as explained earlier (Circuit as shown in Figure 11). Table 3 shows the various switching pulse values of the frontend switches. These pulses are generated when the reference signal overlaps the carrier signals. The pulses are generated along with a delay which is given to each switch. Frequency of the Reference Sine wave is 50 Hz and those of the carrier waves are about 5 KHz each. The output voltage and current waveforms of the 15 level MLI are shows in Figure 7. Figure 8 shows the FFT analysis and the Total Harmonic Distortion (THD) obtained is about 5.08% for load voltage. Figure 9 shows the FFT analysis and the Total Harmonic Distortion (THD) obtained is about 5.28% for Load Current.

The number of levels in the output may be changed dynamically by changing the value of the Modulation Index (m_a). The values of m_a and the number of levels they correspond to are shown in Table 4 and in Figure 10.

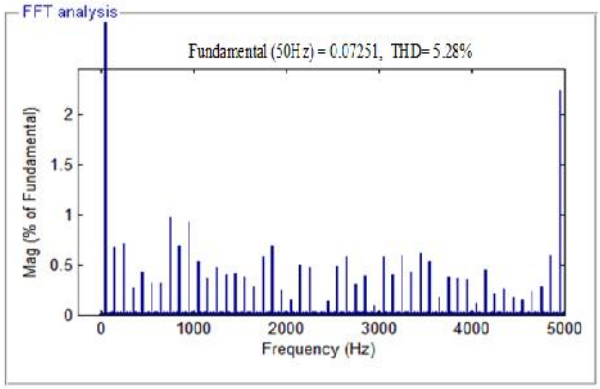

Figure 9. FFT Analysis for load current of proposed MLI

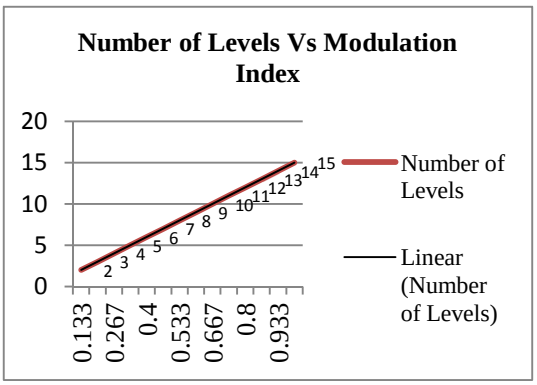

Figure 10. Number of Levels Vs Modulation Index

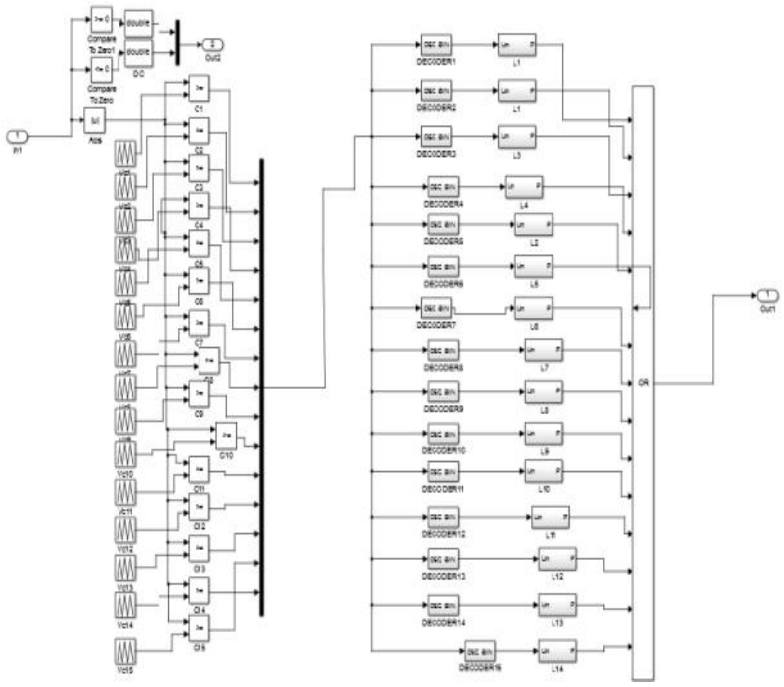

Figure 11. MATMAB/SIMULINK Simulation circuit of Proposed Control Technique using BINARY Code

Table. 4 Modulation Index Vs.No.Of Levels

Modulation Index (0-1)	Number of Levels (1-15)
0.133	2
0.200	3
0.267	4
0.333	5
0.400	6
0.467	7
0.533	8
0.600	9
0.667	10
0.733	11
0.800	12
0.867	13
0.933	14
1.0	15

Figure 12. Hardware implementation

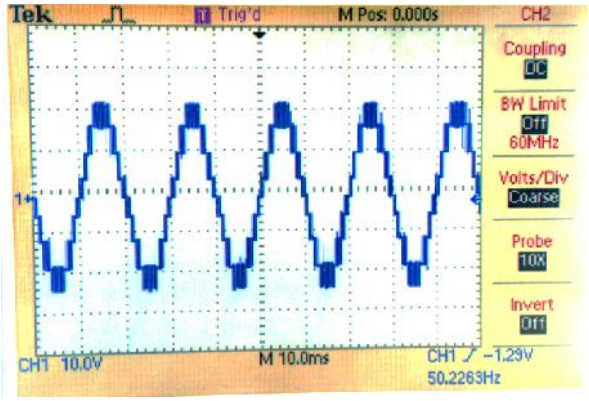

Figure 13. 5 level voltage output at m_a=0.71

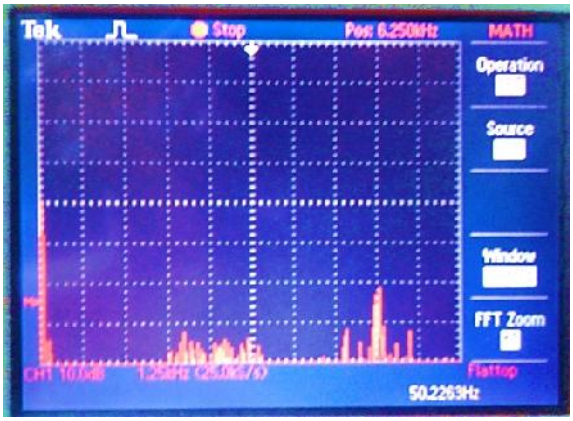

Figure 14. 5 level THD Spectrum at m_a=0.71

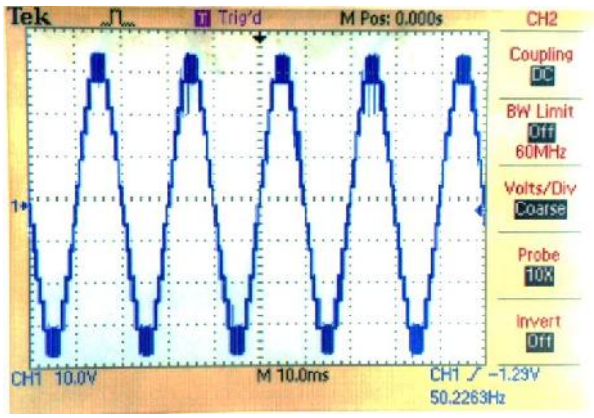

Figure 15. 7 level voltage output at m_a=1.0

5. HARDWARE IMPLEMENTATION

Hardware implementation of the simulation is done by constructing a 7 level MLI prototype (Figure 12). The power switches and conditions are similar to that of the simulation, but the number of levels is restricted to 7 due to economic constraints. However it is understood that once the operation of the seven level MLI experimental setup is verified, the 15-level (simulated) MLI is only an extension to it. The prototype comprises of seven IGBTs (FIO 5O-12BD), in which 3 IGBT are used as level producing which are connected with an three DC voltage sources rating V_1=20V, V_1=10V, V_2=5V and 3 diodes are connected to them and rest of 4 IGBT are used as to design H-Bridge to produce the sine wave with the Deadband time of 4.2 micro seconds is kept between each complimentary IGBT switching.The Xilinx based system generator facility, a toolbox in MATLAB R2011a, was used to generate MC-PWM pulses. Spartan based FPGA board (Spartan 3 XC3SFO-4PQ208C) is used for gernerating pulse to the MLI..

The output voltage waveform and THD spectrum for the Modulation Index value of 0.714 corresponding to 5 levels was captured in Figure 13 and 14; For the Modulation Index value of 1.0 corresponding to 7 levels was captured in Figure 15. The successful verification of the output of the hardware model against the simulation validates the PWM technique. Moreover, it proves the practical feasibility of the proposed MLI system.

6. COMPARISON WITH THE CONVENTIONAL METHODS

The number of source switches (S_N) is determined basedon below equaltionfor the required m output levels:

$$S_N = \frac{(15+1)}{4} + 4 \quad (1)$$

The proposed topology is superior to conventional CH bridge topology in terms of number of semiconductor switches used. However in terms of dc sources used for a given level when compared, the proposed topology is superior to [5] and conventional topologies as shown in the Table 1. For example, for a 13 level output the proposed topology utilizes 10 switches and single dc source for any number of levels whereas the [5] and H bridge topology requires 10 and 24 switches with six dc sources respectively.Further, the reduction of switching devices in the current path will result in the reduction of voltage drop and conduction losses on the devices.

7. CONCLUSION

A single phase 15 level reduced switch MLI topology is introduced and its various modes of operation are studied. A novel SPWM modulation approach is presented and utilized in the proposed topology, theacceptable simulation results are then verified with a FPGA IP Core Processor based Hardware prototype.

The results for the proposed system are summarized as follows:

1. The proposed MLI uses only 8 switches to give 15 level output
2. It is seen from the simulation results that the THD for the Output voltages and the current of the proposed system is quite low when compared with the conventional inverter [5], [8].
3. The proposed system may be extended to a 3 phase 3 line system
4. This configuration of reduced circuit complexity will be adequate for low and medium power applications whereas typical MLIs cannot compete with a standard UPS at (lower-) 2 level output configurations. The inverter can easily be expanded by increasing the levels with minimum number of switches, thus, the overall cost is reduced and the inverter generates higher quality output voltage.

REFERENCES

[1] Nabae; I. Takahashi; H. Akagi. “A new neutral-point-clamped PWM inverter”, IEEE Trans. on Industry Applications, vol. 17, no. 5, pp. 518-523, 1981.
[2] C. Bharatiraja, R. Latha, Dr. S. Jeevananthan, S. Raghu and Dr. S.S. Dash. “Design And Validation Of Simple Space Vector PWM Scheme For Three-Level NPC - MLI With Investigation Of Dc Link Imbalance Using FPGA IP Core”, Journal of Electrical Engineering, vol. 13, edition 1, pp 54-63, 2013.
[3] Rodriguez, J.; Jih-Sheng Lai; Fang Zheng Peng. “Multilevel inverters: a survey of topologies, controls, and applications”, IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp 724-738
[4] P. Jamuna; Dr. C. Christober Asir Rajan. “New Asymmetrical Multilevel Inverter Based Dynamic Voltage Restorer”, Journal of Electrical Engineering, vol. 13, edition 1, pp 244-252, 2013.

[5] Nikhil; V.K.; Joseph, K.D. "A Reduced Switch Multilevel Inverter for Harmonic Reduction", Power and Energy Engineering Conference (APPEEC), Asia-Pacific, pp 1-4, 2012.
[6] Al-Judi; A.; Bierk, H.; Nowicki, E. "A modified cascaded multilevel inverter with reduced switch count employing bypass diodes," IEEE Conference on Vehicle Power and Propulsion, pp. 742-747, 2009.
[7] Ebrahim B., Mohammad F., Farshid N. "Symmetric and asymmetric multilevel inverter topologies with reduced switching devices", Elsevier Journal of Energy Conversion and Management, Electric Power Systems Research Vol. 86, pp.122-130, 2012.
[8] E. Babaei, "A cascade multilevel inverter topology with reduced number of switches", IEEE Trans. Power Electron.Vol 23 no. 6, 2657–2664, 2008.
[9] M. Calais, V.G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems—an overview", in Proc. IEEE Int. Symp. Ind. Electron, vol. 1, pp. 224–229, 1998.
[10] S.B. Kjaer; J.K. Pedersen; F. Blaabjerg. "A review of single-phase grid connected inverters for photovoltaic modules", IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.
[11] P.K. Hinga; T.; Ohnishi; T. Suzuki, "A new PWM inverter for photovoltaic Power generation system", Rec. IEEE Power Electron. Spec. Conf., pp. 391–395, 1994.
[12] Boost, M.A.; Ziogas, P.D. "State-of-the-art carrier PWM techniques: a critical evaluation", IEEE Transactions on Industry Applications, vol. 24, no. 2, Mar 1998 pp 271-280.
[13] http://www.xilinx.com
[14] J. Rodríguez; J. S. Lai; F. Z. Peng. "Multilevel inverters: A survey of topologies, controls, and applications", IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.
[15] Bharatiraja, C., Raghu, S., Rao, P., Paliniamy, K.R.S. "Comparative analysis of different PWM techniques to reduce the common mode voltage in three-level neutral-point- clamped inverters for variable speed induction drives", International Journal of Power Electronics and Drive Systems, vol. 3, Issue 1, March 2013, Pages 105-116.
[16] Alishah, R.S., Hosseini, S.H. "A new multilevel inverter structure for high-power applications using multi-carrier PWM switching strategy", International Journal of Power Electronics and Drive Systems, vol 6, Issue 2, 1 June 2015, Pages 318-325.
[17] Gnana Prakash, M., Balamurugan, M, Umashankar, S. "A new multilevel inverter with reduced number of switches", International Journal of Power Electronics and Drive Systems, vol 5, Issue 1, September 2014, Pages 63-70.
[18] Hemanthakumar, R., Raghavendrarajan, V., AjinSekhar, C.S., Sasikumar, M. "A novel hybrid negative half cycle biased modulation scheme for cascaded multilevel inverter", International Journal of Power Electronics and Drive Systems, vol 4, Issue 2, June 2014, Pages 204-211.