International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 7, No. 2, June 2016, pp. 358~368
ISSN: 2088-8694

Analysis of 1MHz Class-E Power Amplifier for Load and Duty Cycle Variations

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Article Info

Article history:

Received Nov 30, 2015
Revised Mar 10, 2015
Accepted Mar 27, 2016

Keyword:

Class-E
Pulse width modulation
Resonant converter
Zero voltage switching

ABSTRACT

This paper presents the simulation and experimental of Class-E power amplifier which consists of a load network and a single transistor. The transistor is operated as a switch at the carrier frequency of the output signal. In general, Class-E power amplifier is often used in designing a high frequency ac power source because of its ability to satisfy the zero voltage switching (ZVS) conditions efficiently even when working at high frequencies with significant reduction in switching losses. In this paper, a 10W Class-E power amplifier is designed, constructed, and tested in the laboratory. SK40C microcontroller board with PIC16F877A is used to generate a pulse width modulation (PWM) switching signal to drive the IRF510 MOSFET. To be specific, in this paper, the effect on switching and performance at 1MHz frequency are studied in order to understand the Class-E power amplifier behavior. Performance parameters relationships were observed and analysed in respect to the load and duty cycle. The proposed Class-E power amplifier efficiency is 98.44% powered with 12V dc, operated at frequency 1MHz and 50% duty cycle to produce a stable sinusoidal signal. Theoretical calculations, simulation and experimental results for optimum operation using selected component values are then compared and presented.

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1. INTRODUCTION

Class-E power amplifier, also called class-E inverter, is a resonant power converter and often applied to design high frequency switching power converters. Class-E power amplifiers are the most efficient amplifiers known so far because of its ability to achieve a 100% fundamental efficiency due to soft switching or ZVS conditions [1] [2] [3] [4] [5] [6] [7] [8]. The Class-E power amplifier was first introduced by N.O and A.D Sokal in 1975 [1]. The conventional class-E amplifier was derived and analysed extensively by Raab in [2]. Early papers addressed the problem of the efficiency against switching frequency and duty cycle based on mathematical analysis. Since the introduction of the Class-E power amplifier that offers amazing advantages, the Class-E power amplifier has attracted a great deal of attention in recent years. After that, various topologies have appeared to expand the applications of class E circuit such as class E inverter [3] [14] [15] [13] [16] [17], class E DC/DC converter [14] [18] and class E rectifier [13]. Also, the class E circuits are applied to RF power amplifier [19] [20], induction heating system [20] [21], and RF powering [21] [22] [23] [24].

Figure 1 shows the conceptual desired current and voltage waveforms of the switch for maximum power efficiency. The low order Class-E power amplifier of Figure 2 generates voltage and current

waveforms that approximate to the conceptual desired waveforms in Figure 1. The current and voltage waveforms of the switch are displaced with respect to time, yielding a very low power dissipation in the transistor. In particular, the switch voltage is nearly zero when the switch in ON and the drain current is determined by the external circuit due to the switching action of the transistor. When the switch is OFF, the switch current is zero and the switch voltage is determined by the transient response of the load network. Since the switch current and voltage waveforms do not overlap during the switching time intervals, switching losses are virtually zero, yielding high efficiency, that is, theoretically 100% [1] [2] [9] [10] [11] [12] [25].

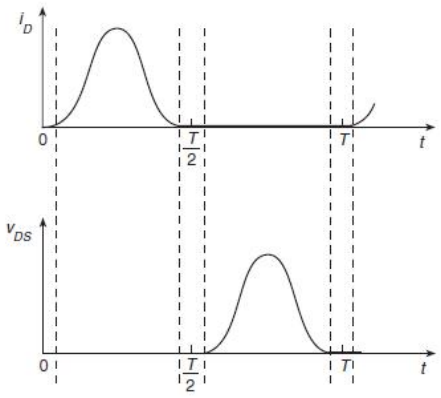


Figure 1. (a) Current Through Switch(b) Voltage Across Switch [13]

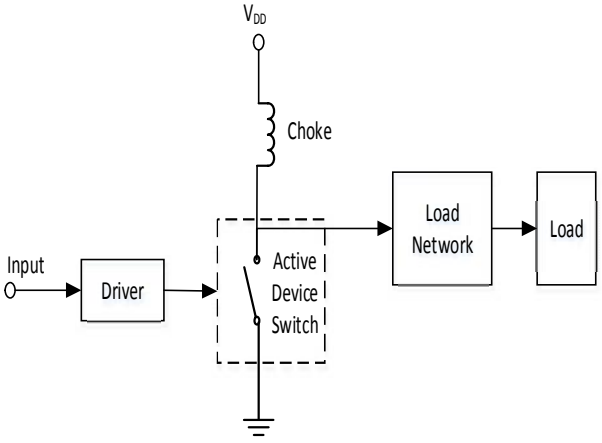


Figure 2. Single-ended Switch-mode Power Amplifier Block Diagram

From the literature we see that, every design of Class-E method has its own merits, although it is, up to today, there is still room to be explored and improved. Furthermore, to the best of our knowledge, this is the first time that simple yet flexible (can be reprogrammed) design of MOSFET driver circuit using microcontroller PIC16F877A are presented. This paper presents design and analysis for single ended Class-E power amplifier. The contribution of this paper can be summarized as follows:

1) The used of SK40C microcontroller board with PIC16F877A as a MOSFET driver circuit. More importantly, by implementing suggested circuit driver, the ZVS conditions can be achieved successfully.
2) Our theoretical analysis described in this paper is useful to understand the characteristics behaviour of Class-E power amplifier. The effects of circuit performance when the load and duty cycle varies under optimum operation were analysed systematically, being proof through theoretical, simulation and experimental results.

The structure of this paper is arranged as follows. Section 2 explains briefly the Class-E power amplifier circuit operation and reveal briefly some equations used in order to get theoretical value of components. Meanwhile, section 3 discusses on three sets of design examples, simulation and experimental results to verify the theoretical analysis and final conclusions are drawn in Section 4.

2. ANALYSIS OF CLASS-E POWER AMPLIFIER CIRCUIT

The typical circuit of the Class-E power amplifier and its theoretical waveforms is shown in Figure 3 and Figure 4, respectively. It consists of dc supply voltage source V_{dc}, a MOSFET as a switching device, a shunt capacitance Cp, a series-resonant R_L-L-C output circuit and dc choke inductor L_F. The choke inductor is usually high enough to force a dc current, I_{dc}. In the Class-E power amplifier, the switch Q is driven by a gate-to source voltage V_g. During the switch off interval, the sum of currents through the choke inductance and resonant filter flow through the shunt capacitance. The current through the shunt capacitance produces the switch voltage V_{ds}.

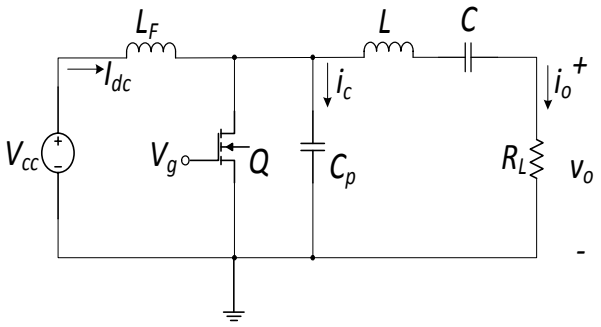


Figure 3. Typical Class-E Power Amplifier Circuit

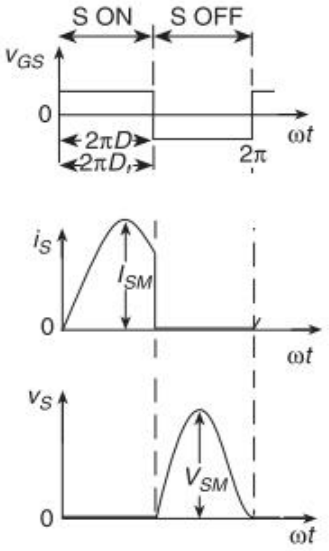


Figure 4. Theoretical Waveforms in Class E zero-voltage-switching amplifier [13]

Based on Figure 4, the switch turns ON and OFF at the operating frequency setting by a MOSFET gate drive. Circuit operation is determined by the switch when on and by the transient response of the load network when the switch is OFF. The switching pattern is defined as:

$$\text{Switch} = \begin{cases} ON\ satate\ for\ 0 \le \mu t < DT \\ OFF\ state\ for\ DT \le \mu t < T \end{cases}$$

where D is the switch duty cycle and *T* is the period for one complete cycle. The MOSFET turn ON and OFF alternately at $\mu t = 0$ and *DT*. Therefore, the switch voltage waveform that satisfies the Class-E nominal condition, i.e., condition (1) or (2), at the switch turn ON instant as a function of the duty ratio, is expressed as follows:

ZVS condition:

$$v_{ds}(\omega t)\big|_{\omega t=DT} = 0 \quad (1)$$

Zero derivative switching (ZDS) condition:

$$\frac{d\,v_{ds}(\omega t)}{d(\omega t)}\bigg|_{\omega t=DT} = 0 \quad (2)$$

where $v_{ds}(\omega t)$ is the switch voltage. In this case, the voltage v_{ds} across the switch and the shunt capacitance C_p is zero when the switch turns ON. In other word, the energy stored in the shunt capacitance C_p is zero when the switch turns on, yielding to zero turn ON switching loss.

2.1. Assumptions of Class-E Inverter for Optimum Operation

The assumptions of the circuit are quite similar to the one that is presented in [1] and [3]. The analysis of the Class-E power amplifier of Figure 3 is carried out under the following assumptions:

1) The MOSFET and diode form an ideal switch whose on-resistance is zero, off-resistance is infinity, and switching times are zero.
2) The choke inductance is high enough so that its ac component is much lower than the DC component of the input current.
3) The loaded quality factor Q of the L, C and R_L series-resonant circuit is high enough so that the current I through the resonant circuit is sinusoidal.
4) Duty cycle, D = 50%

5) All circuit elements are ideal.

2.2. Circuit Component Equations

In the typicalClass E power amplifier, inductor $L_F$is assumed to be large, the current through the load resistor is assumed to be a pure sine and no losses are included. Under these conditions, the parameters of the circuit shown in Figure 3 are defined and given as follows:
The full load resistance is

$$R_L = \frac{8V_{CC}^2}{(\pi^2 + 4)P} \tag{3}$$

where P is output power. The current drawn from the DC power supply is

$$I_o = \frac{P}{V_{CC}} \tag{4}$$

The load network component values are as follows:

$$C_p = \frac{I_o}{\omega V_{CC}} = \frac{1}{\omega R_L \left(\frac{\pi^2}{4} + 1\right)\frac{\pi}{2}} \tag{5}$$

$$C = \frac{1}{\omega R_L \left(Q - \frac{\pi(\pi^2 - 4)}{16}\right)} \tag{6}$$

$$L = \frac{QR_L}{\omega} \tag{7}$$

where Q is quality factor. In order to keep the current ripple in the choke inductor stays at below 10% of the full-load DC input current I_{dc}, the value of the choke inductance must be greater than

$$L_{f(\min)} = 2\left(\frac{\pi^2}{4} + 1\right)\frac{R}{f}. \tag{8}$$

In practical terms, the choke inductance value is not all that critical, as long as its impedance is at least an order of magnitude higher than the load resistance and it is not self-resonant at the first three or four harmonics. It needs to look like an open circuit to these harmonics, if possible.

3. DESIGN EXAMPLES AND RESULT DISCUSSIONS

There were three sets of simulation and experimental examples conducted in order to verify the previous equations and understand the Class-E behaviour. Based on the design equations and assumptions provided in Section 2, all the circuit parameters are calculated and tabulated as in Table I. Then simulations are carried out using Proteus before the real circuit is implemented. In order to validate the simulation results, the experimental work is carried out. IRF510 MOSFET is used as a switching device in the design. It is n-channel, enhancement mode and designed especially for high speed applications. Based on Table I, the peak switch voltage and current were 42.74V and 2.39A respectively. According to IRF 510 MOSFET datasheets, the breakdown switch voltage and current were 100V and 5.5A respectively. This confirms that the IRF510 MOSFET is suitable to be used in a Class-E power amplifier circuit in practical applications.

In Figure 5, the SK40C microcontroller board with PIC16F887A is used to generate a desired switching control signal frequency at 50% duty cycle for the MOSFET gate. However, the microcontroller output voltage, typically 5V is not sufficient to turn ON the IRF510 MOSFET that requires at least 10V to operate in safe operating area. Therefore, an IC gate drive TC4422 is used here to provide sufficient gate voltage or charge to drive the IRF510 MOSFET. The complete experimental setup is shown in Figure 6. All

the voltage and current of the designed amplifier are measured by a Sanwa CD771 Digital Multimeter and the Agilent Technologies DSO-X 2012A oscilloscope is used to obtain the waveforms data of the output voltage.

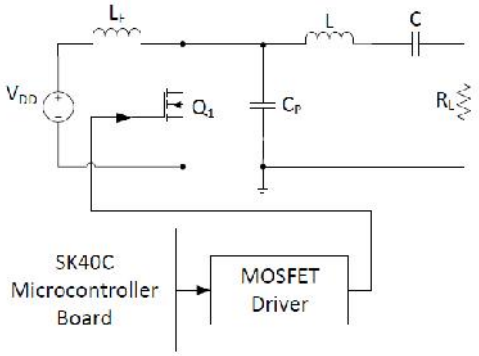


Figure 5. Class-E Power Amplifier with MOSFET Driver Circuit

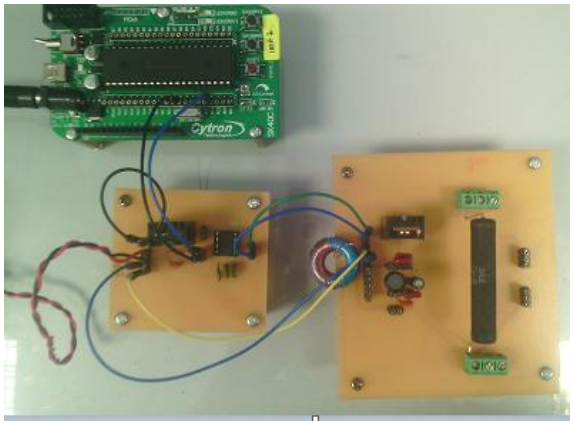


Figure 6. Class-E Power Amplifier Experimental Setup

3.1. Design of Class-E Power Amplifier for Optimum Operation

In the first circuit design, consider the circuit of Figure 3 with design specifications: V_{cc} = 12V, D = 0.5, Q = 10, Po = 10W, f = 1MHz, and components value R_L, C_P, C and L_f are calculated and tabulated in Table 1. In this part, the effects on switching and performance are studied.

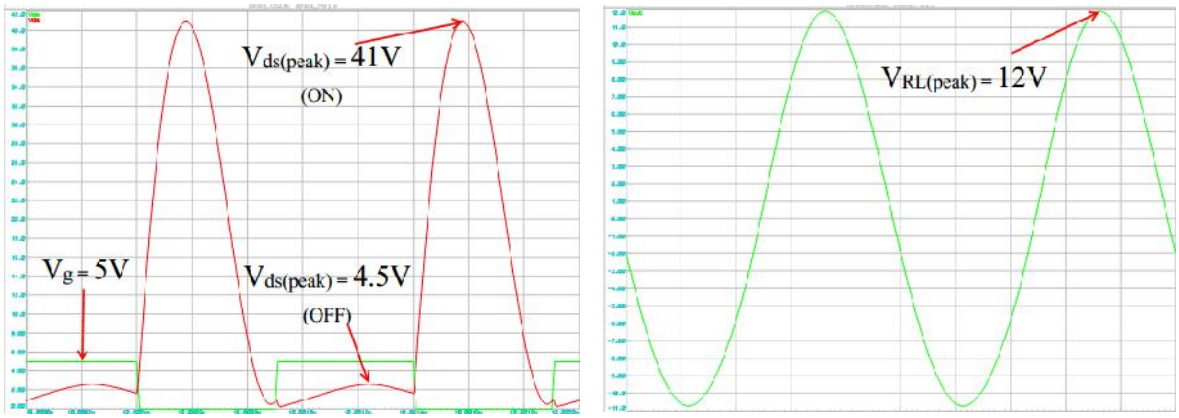
Table 1. Class-E Power Amplifier Results At Optimum Load

Parameter		Result		
		Calc.	Sim	Exp.
R_L	Ω	8.31	8.31	8.3
Cp	nF	3.52	3.52	3.60
C	nF	2.17	2.17	2.20
Lf	uH	57.60	57.60	100.00
L	uH	13.22	13.22	13.30
$V_{RL(peak)}$	V	12.89	12.00	12.90
$V_{ds(peak)}$	V	42.74	41.00	42.00
I_{dc}	A	0.83	0.82	0.83
$I_{RL(peak)}$	A	1.55	1.44	1.54
$V_{c(peak)}$	V	114.03	112.00	111.40
$V_{L(peak)}$	V	128.89	122.00	128.70
$I_{s(peak)}$	A	2.39	2.10	2.30
$I_{s(rms)}$	A	1.28	1.26	1.28
$P_{o(ac)}$	W	10.01	8.62	9.84
$P_{i(dc)}$	W	10.00	9.84	9.96
η	%	100.12	87.56	98.82

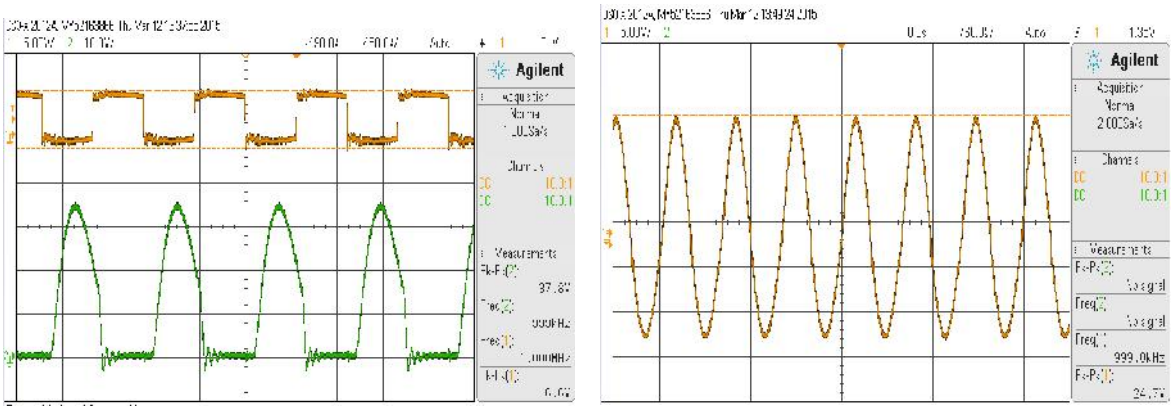
For 1MHz operation frequency, the simulation value of peak output voltage, $V_{RL(peak)}$ = 12V, 6.9% lower than the theoretical value. The simulation value of dc power input is $P_{i(dc)} = V_{CC} \times I_{dc}$= 9.84W which is 1.6% lower than the theoretical value. The simulation value of ac output power, $P_{o(ac)} = (I_{RL(rms)})^2 * RL$ = 8.62W, 13.8% lower than theoretical value. The simulation value of efficiency,η = 87.56% which is 12.4% lower than the theoretical value.

Figure 7 shows the waveforms obtained from Proteus simulation and circuit experiment. It can be seen in Figure 7(a), simulation value for the maximum voltage across MOSFET during turn OFF is $V_{ds(peak)}$ = 41V, almost three times larger than Vcc. Meanwhile, during turn ON, $V_{ds(peak)}$ = 4.5V, nearly 11% of the peak switch voltage. In an optimum design yielding the maximum drain efficiency, the switch voltage V_{ds} at the switch turn time is usually 10% to 50% of the peak switch voltage, which is a nonzero voltage switching condition. Refer to Figure 7(b), the experiment value of maximum voltage across the MOSFET during turn OFF is $V_{ds(peak)}$ =37.8, 8.75% lower than the simulation value. Meanwhile, during turn ON, $V_{ds(peak)}$ = 4V, nearly 10% of the switch peak voltage. The experiment value of the peak output voltage, $V_{RL(peak)}$ is 12.50V, 2.9 % higher than the simulation value.

All the simulation and experiment results are consistent with the theoretical predictions for the first circuit design. Therefore, it can be concluded that the optimum operation can be achieved only at an optimum load resistance, $R_L = R_{opt}$. When $R_L = R_{opt}$, the sinusoidal output voltage will reach nearly to maximum for the tested operating frequency. Furthermore, the experiment switching voltage waveform proved that the Class-E power amplifier circuit using PIC16F877A satisfy the ZVS conditions since there is no overlap between voltage over the MOSFET channel and current through the channel. In terms of the efficiency, it can be seen that the experiment circuit produces 98.4% efficiency, 11.05% higher than the simulated value. This is due to switching losses, non-pure resistive load, equivalent series resistance (ESR), parasitic resistance of each components and dissimilarities in component selections.



(a) Proteus Simulation



(b) Circuit Experiment

Figure 7. Input, Switching Voltage and Output Voltage Waveforms for the First Design at 1MHz Frequency

3.2. Class-E Power Amplifier with Load Variations

In the second circuit design, consider the circuit of Figure 3 with design specifications: V_{cc} = 12V, D = 0.5, f = 1MHz, Q = 10 and Po = 10W. Part 3.1 investigated Class-E power amplifier circuit for optimum load at 1MHz operating frequency. However, in many applications, the load resistance varies over a certain range.

As shown in Figure 8(a) and 8(b), if R_L is greater than R_{opt}, the amplitude of I_{RL} of the current i_o, through L-C-R_L series-resonant circuit is lower than that for optimum operation. Voltage drop across the shunt capacitor C_p decreases, and the switch voltage V_{ds} is greater than zero at turn on. On the other hand, in Figure 8(c) and 8(d), if R_L is less than R_{opt}, the amplitude I_{RL} is higher than that for optimum operation, the voltage drop across the shunt capacitor C_p increases, and the switch voltage V_{ds} is less than zero at turn on. Therefore, the load power and efficiency for both cases are lower than the load power and efficiency at optimum load.

Based on simulation and experiment results tabulated in Table 2, it can be concluded that the efficiency of the circuit is maximum when R_L=R_{opt}. In addition, V_{cc}, P and R_L are interdependent quantities as referred to (11). In many applications, the load resistance is given and is different from that given in (11). There is a need for matching circuits that can provide impedance transformation to overcome this problem. This work will be done in the near future.

Table 2. Class-E Power Amplifier Results At Different Load

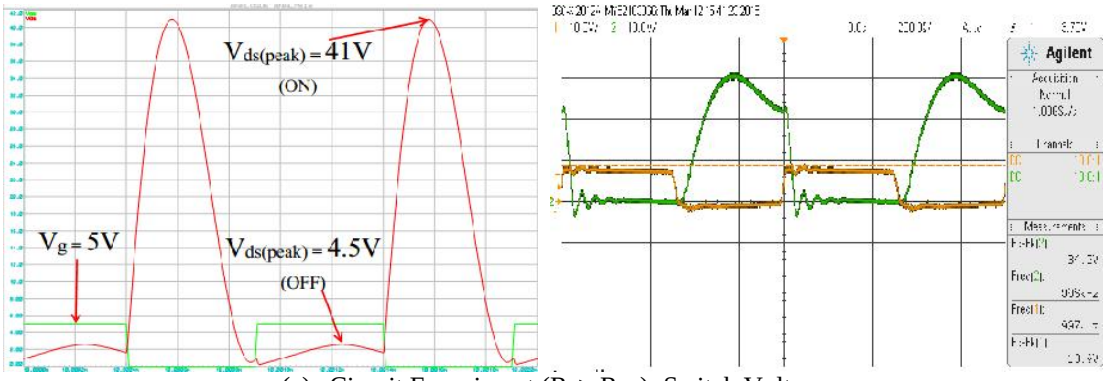
Frequency		f = 1MHz						
Result			RL = opt		RL<Ropt		RL>Ropt	
		Calc.	Sim	Exp.	Sim	Exp.	Sim	Exp.
R_L	W	8.31	8.31	8.4	5	5	20	20
Cp	nF	3.52	3.52	3.60	3.52	3.60	3.52	3.60
C	nF	2.17	2.17	2.20	2.17	2.20	2.17	2.20
Lf	uH	57.60	57.60	100.00	57.60	100.00	57.60	100.00
L	uH	13.22	13.22	13.30	13.22	13.30	13.22	13.30
$V_{RL(peak)}$	V	12.89	12.00	12.50	8.00	9.00	14.50	13.70
$V_{ds(peak)}$	V	42.74	41.00	39.00	44.00	40.20	30.50	31.00
I_{dc}	A	0.83	0.82	0.80	0.84	0.80	0.55	0.50
$I_{RL(peak)}$	A	1.55	1.44	1.50	1.70	1.80	0.72	0.70
$V_{c(peak)}$	V	114.03	112.00	108.50	130.00	120.00	64.00	64.00
$V_{L(peak)}$	V	128.89	122.00	125.50	146.00	140.00	61.00	59.00
$I_{s(peak)}$	A	2.39	2.10	2.30	2.25	2.30	1.20	1.10
$I_{s(rms)}$	A	1.28	1.26	1.20	1.29	1.20	0.85	0.80
$P_{o(ac)}$	W	10.01	8.62	9.45	7.23	8.10	5.18	4.90
$P_{i(dc)}$	W	10.00	9.84	9.60	10.08	9.60	6.60	6.00
h	%	100.12	87.56	98.44	71.68	84.38	78.55	81.67

3.3. Class-E Power Amplifier with Duty Cycle Variations for 1MHz

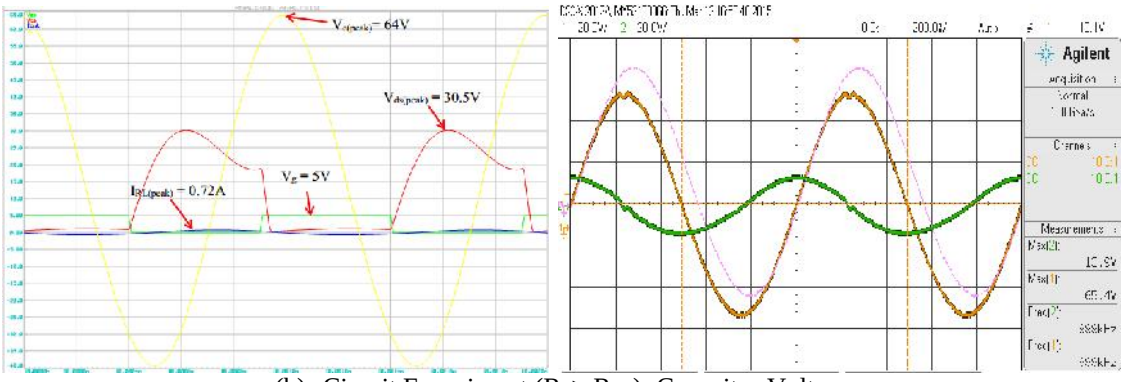
In the third circuit design, the effect of changing the duty cycle to the output power performance will be discussed. Consider Figure 3 with the design specifications: Vcc = 12V, Q = 10, Po = 10W, R_L = R_{opt}, and f = 1MHz. In this part, the duty cycle D is controlled in the range of 10% to 90%. Figure 9 shows a plot of output power performance versus D. It shows that all the parameters that have been simulated will subsequently reach maximum value. Also the maximum output power performance is only occur at D = 0.5. At this point, the efficiency for the experiment equals to 98.44%, 1.56% lower than the calculated value. Based on (9) and (10) below, the initial phase of current is dependent on the duty cycle. ZVS will miss out while the duty ratio is changed to regulate the power output if the operating frequency cannot adaptive tune. This will lead to switching losses due to phase shifting. The miss out of ZVS can be solved by implementing self-tuning feedback controller and this will have to be investigated.

$$¤ = ® + \tan^{-1}\left(\frac{\cos 2®D - 1}{2®(1-D)}\right) \quad (9)$$

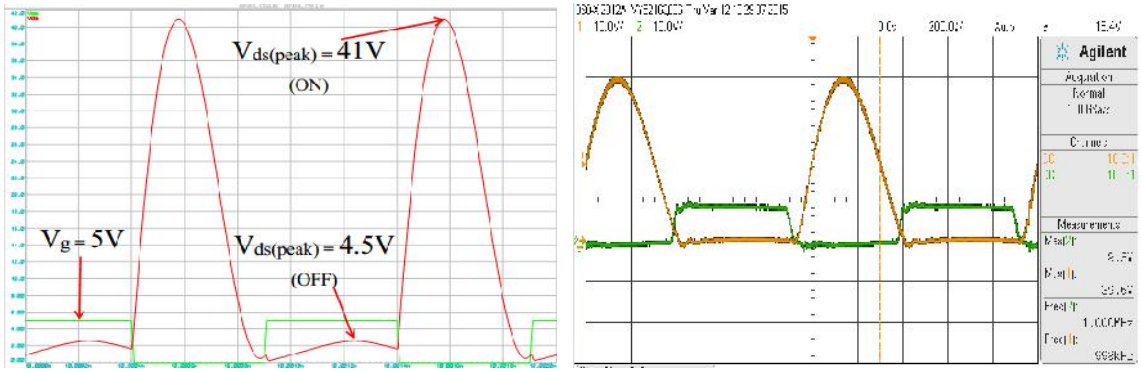
$$V_{RL(peak)} = \frac{2\sin ®D \sin(®D + ¤)}{®(1-D)}(V_{CC}) \quad (10)$$



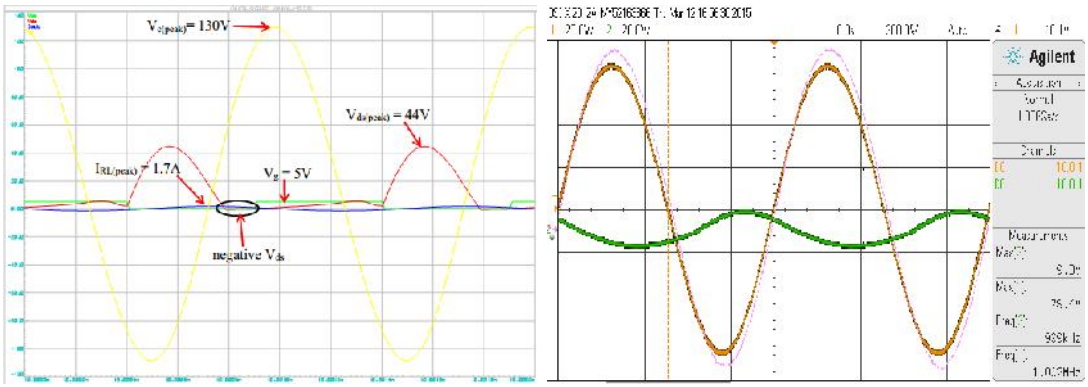
(a) Circuit Experiment ($R_L > R_{opt}$): Switch Voltage



(b) Circuit Experiment ($R_L > R_{opt}$): Capacitor Voltage



(c) Circuit Experiment ($R_L < R_{opt}$): Switch Voltage



(d) Circuit Experiment ($R_L < R_{opt}$): Capacitor Voltage

Figure 8. Simulation and Experimental Waveforms of Capacitor Voltage and Switching Voltage

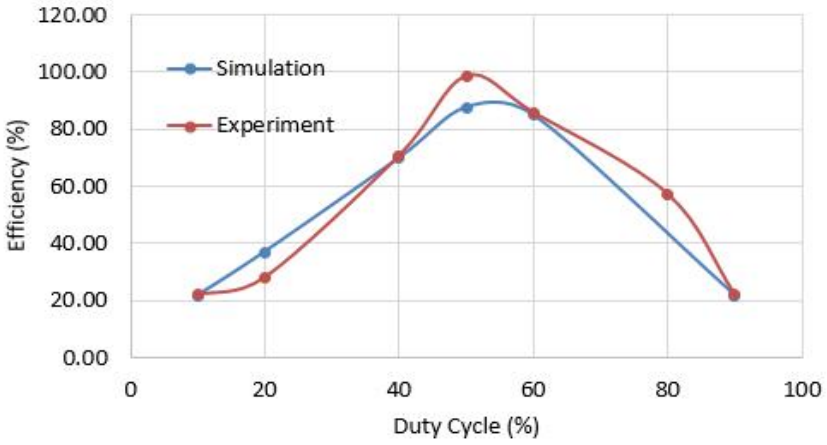


Figure 9. Plot of Output Power Capability When Varies the Duty Cycle

4. CONCLUSION

An analysis of the Class-E power amplifier operation has been presented in this paper. Three circuit design examples along with the Proteus simulation and experiment waveforms are given to show the validity of the analytical expression. The switch control signal for IRF510 MOSFET using microcontroller PIC16877A has been proposed and the results indicate that ZVS condition can be achieved successfully. In the laboratory experiment, the Class-E with optimum load and D = 0.5 has achieved 98.44% efficiency at 10W output power for 1MHz operating frequency. From the three design examples, it can be concluded that the optimum operation can be achieved only at an optimum load resistance, $R_L = R_{opt}$ .In order to transfer a specified amount of output power at specified dc voltage, the load resistance R must be of the value determined by (3) and the maximum output power capability only occur at D = 0.5. Moreover, the agreement between experiment performance and theoretical performance can still be considered excellent. This analysis will assists the researchers to understand more on the Class E behavior thus able to produce a better performance in the upcoming investigation. For future development, this circuit will be applied at the transmitter side of a capacitive power transfer system.

ACKNOWLEDGEMENTS

This research was supported by the Universiti Teknikal Malaysia Melaka (UTeM) [PJP/2014/FKEKK(2A)/S01299] and Malaysian Ministry of Education [RAGS/2013/FKEKK/TK02/B00035] grants.

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