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Modelling and Simulation of a Sensorless Control of a True Asymmetric Cascade H-Bridge Multilevel Inverter PMSM Drives

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Article Info	ABSTRACT
	This paper introduces a new method to track the saliency of an AC motor fed by a multilevel converter through measuring the dynamic current response of the motor line currents due the IGBT switching actions. The method uses only the fundamental PWM waveform (i.e there is no modification to the operation of the multilevel converter) similar to the fundamental PWM method proposed for a 2-level converter. Simulation results are provided to demonstrate the performance of the complete sensorless speed control of a PM motor driven by such a converter over a wide speed range. Finally the paper introduces a comparison between the 2-level converter and the multilevel converter in terms of the reduction of the total harmonic distortion (THD) using the fundamental PWM method in both cases.

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1.   INTRODUCTION

Sensorless control of motor drives using two level converters has been widely researched for systems employing standard two level converters. At low and zero speed, some form of additional excitation has been proposed, such as the injection of a high frequency (HF) voltage or current [1-3] or the injection of test pulses [4-6]. However, these techniques introduce significant additional current distortion either due to the injected signals themselves (as in the HF injection methods and the INFORM method [4]) or due to the insertion of the minimum pulse width in the operation of the drive system when applying the Fundamental PWM Excitation method (FPE) [6]. This distortion causes audible noise, torque pulsations and increases the system losses.

The multilevel converter can achieve a higher voltage and power capability with conventional switching devices compared to two level converters, and is now used for high power drives [7, 8, 9]. Multilevel converters employ switching devices connected in a chain, which sequentially switch different DC voltages across the motor using a special PWM technique, to create a stepped output voltage. The particular structure of some of these converters offers significant potential for improving sensorless control of motors, as they employ H bridge circuits with a relatively low DC link voltage. [10] uses H-Bridges connected in series with 2-Level inverter which are used to generate a small voltage pluses used only to track the saliency position, this technique achieve a good sensorless results at the same time reduce significantly the current distortion due to the use of small voltage pulses. Previous researches into sensorless multilevel drives used a special multilevel topology where the H-Bridges were used only for generating the voltage pulses to track the saliency [10] and were added to a conventional 2-level converter. In this paper a new technique is proposed to track the saliency in any motor driven by any multilevel converter topology without disturbing the operation of the multilevel converter. At the same time it reduces the current distortion associated with the 2-

Level sensorless techniques significantly through making use of the small voltage steps of the multilevel inverter output as excitation voltages.

2. THE MULTILEVEL TOPOLOGY AND OPERATION

Lipo [7] proposes a multilevel topology which uses two cascaded H bridge circuits per phase. The first has a high DC link voltage, and employs GTOs or IGCTs as the switching devices which are controlled at relatively low frequency. The second uses a lower DC link voltage (for example 1/2 of the GTO DC link voltage) and employs IGBTs with a higher switching frequency. This operation of IGBT and IGCT meets with the features of each particular one. For example the IGCT can block high voltages but it has a slow switching action while the IGBT can switch very quickly but has small voltage blocking capabilities. The combination of these circuits can provide a good quality voltage waveform for high voltage applications.

In This paper, a similar topology is used but with using a combinations of 2V (400V) and V(200V) as DC source voltage levels as shown in Figure 1.
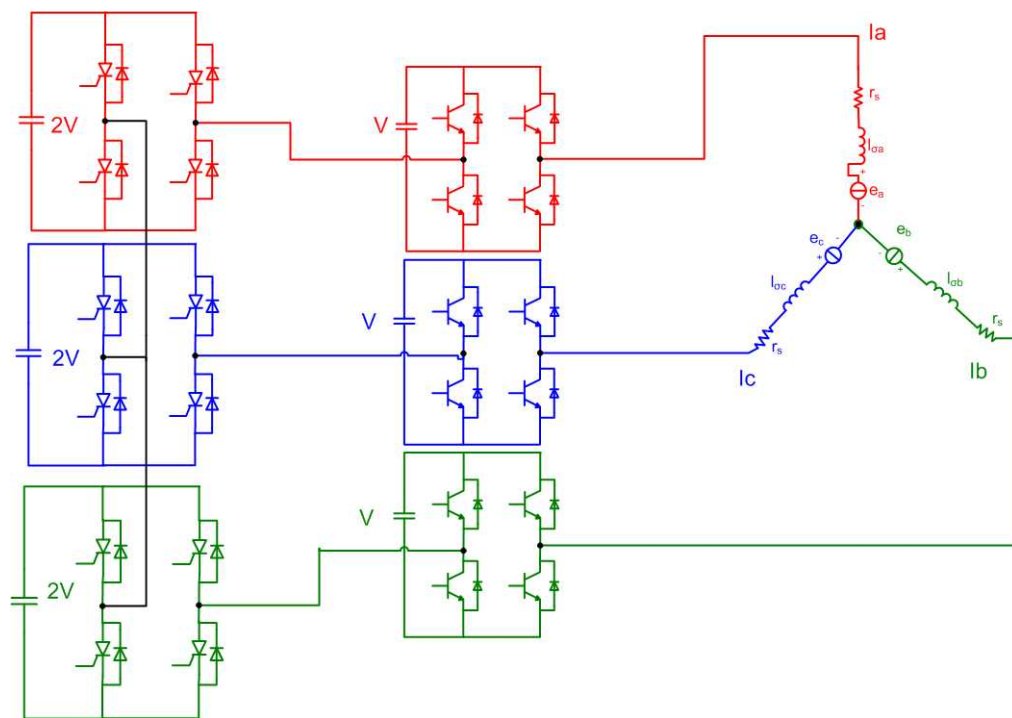

Figure 1. Hybrid asymmetric cascaded H-Bridge seven level converter

The number of levels that can be generated using this topology will be 7 (3V, 2V, V, 0, -V, -2V, -3V) although only 2 H-Bridges are used in each leg. This is due to the asymmetric DC source levels used. Each level can be generated by a specific switching of each H-Bridge according to table 1:

Table 1. Relation between output voltage and output of each cell in seven level asymmetric Hybrid cascaded H-Bridge converter

Output voltage	H-Bridge 1	H-Bridge 2
3V	2V	1V
2V	2V	0V
V	0V	1V
0	0V	0V
-V	0V	-1V
-2V	-2V	0V
-3V	-2V	-1V

The waveform obtained from each H-Bridge in one fundamental period is shown in Figure 2.
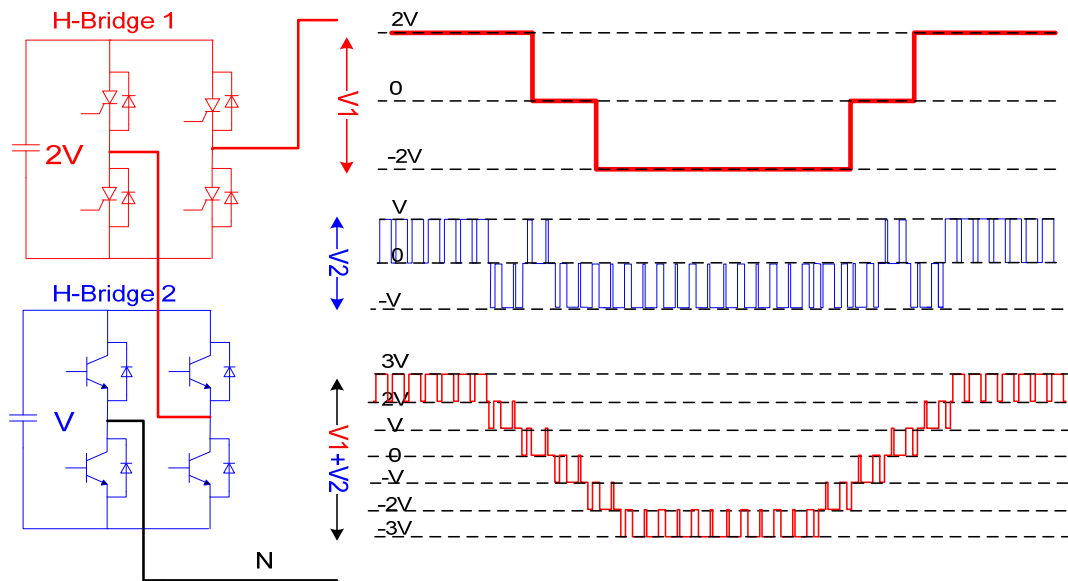

Figure 2. Operation of the seven level asymmetric hybrid cascaded H-bridge converter.

2.1. Space Vector Modulation for 7-Level Inverter

Consider the 7 level cascade H-Bridge converter shown in Figure 2. The possible output voltages that can be generated from each leg are 3V, 2V, V, 0, -V, -2V and -3V. According to the switching state of each cell in the multilevel converter, it is possible to generate 2^7 switching states in a space plane as shown in Figure 3. The nodes represent the tips of these vectors (basic vectors) in the plane. For example; the node that has the switching pattern (3,0,-1) means that the H-Bridges in phase a generates +3V, in phase b generates 0V and in phase c generates –V. The same output voltage of the inverter can be generated by other switching patterns for example (2,-1,-2) and (1,-2,-3). Many methods proposed in using space vector modulation of multilevel inverter [11, 12, 13].The method that is adopted in this work is proposed in [11], as it has the following feature:

- It is very simple and effective.
- The output voltage contains minimum distortion.
- The input current has minimum current distortion.
- It is general and applicable to any level.

Returning to Figure 3, each vector in space is generated according to the voltage generated from the cells in phases A, B and C. These vectors can be transformed into αβ coordinates (60^0 coordinate system) according to the following equations:

$$V_\alpha = V\cos\theta - \frac{V\sin\theta}{\sqrt{3}} \tag{1}$$

$$V_\beta = \frac{2V\sin\theta}{\sqrt{3}} \tag{2}$$

Where V_α and V_β are the coordinates of the vector V in the 60^0 coordinate system, V and θ are the amplitude and phase angle of the reference vector respectively. To illustrate this transformation, Figure 3 is considered again. All the switching patterns that generate V_1 in the coordinates shown in Figure 3 which are (2,0,-2), (3,1,-1) and (1,-1,-3) will be represented by the point (2,2) in αβ coordinate system using (1) and (2). Repeating for all the vectors in space, the new coordinate system will be as shown in Figure 4.
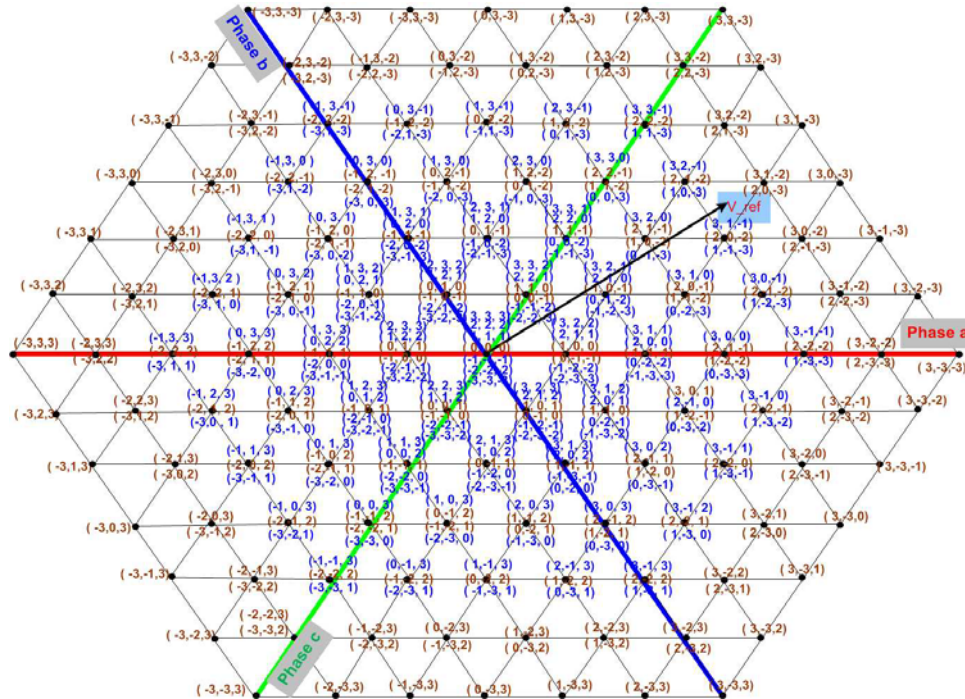
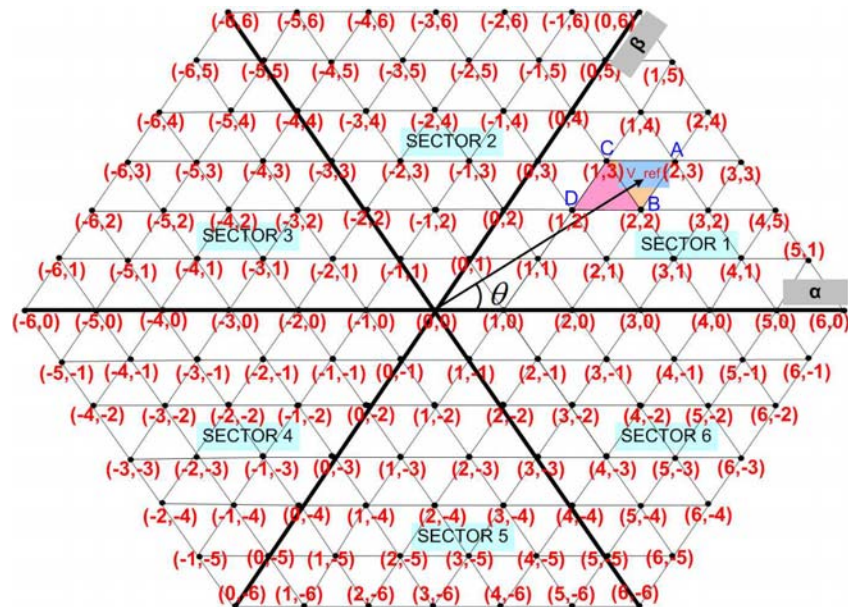Figure 3. The available switching states and corresponding vector of the seven level SVPWM state diagram

Figure 4. Seven level SVPWM state diagram in αβ coordinates

To determine the location of the reference voltage $V_{\_ref}$, two quantities will be used which are :

$$V_{D\alpha} = \mathrm{int}\left(V_{\alpha_{ref}}\right) \tag{3}$$

$$V_{D\beta} = \mathrm{int}\left(V_{\beta_{ref}}\right) \tag{4}$$

Where int() is a lower integer function. After these two values are calculated, it is possible to identify in which pair of triangles the reference voltage exist. For example ΔCBA or ΔCBD according to Figure 4. The coordinates of the three other vectors can be calculated according to the following equations:

$$\begin{cases} (V_{B\alpha}, V_{B\beta}) = (V_{D\alpha} + 1, V_{D\beta}) \\ (V_{C\alpha}, V_{C\beta}) = (V_{D\alpha}, V_{D\beta} + 1) \\ (V_{A\alpha}, V_{A\beta}) = (V_{D\alpha} + 1, V_{D\beta} + 1) \end{cases} \tag{5}$$

The extra determination of the triangle where the reference vector exists can be achieved using the following criterion:

$$\begin{cases} V_{ref} \text{exist in } \Delta CBD \text{ if } (V_{\alpha_{ref}} + V_{\beta_{ref}}) \leq (V_{D\alpha}, V_{D\beta}) \\ V_{ref} \text{exist in } \Delta CBA \text{ if } (V_{\alpha_{ref}} + V_{\beta_{ref}}) > (V_{D\alpha}, V_{D\beta}) \end{cases} \tag{6}$$

2.2. Choosing the Switching Sequence

The switching pattern for each basic vector will be chosen according to what is called 'All mean Method' [11]. In this method an equivalent mean switching state is used for every basic space vector. If the number of the switching patterns that generate a specific basic vector is odd then the mean switching will be the middle one while if the number of the switching patterns is even then the mean switching will be the two switching patterns in the middle. For instance, the vector whose tip has the coordinates (0,1) has 6 different switching patterns (3,3,2), (2,2,1), (1,1,0), (0,0,-1), (-1,-1,-2) and (-2,-2,-3). The mean switching patterns will be (1,1,0) and (0,0,-1). Another example is the vector whose tip has the coordinate (1,1) has five different switching patterns (3,2,1), (2,1,0), (1,0,-1), (0,-1,-2) and (-1,-2,-3). The mean switching pattern will be (1,0,-1). The mean switching patterns for all the vectors in space for 7-level converter is shown Figure 2 in brown. Considering the switching sequence, there are two general requirements:

- The transition from one switching state to another is achieved by switching only one H-Bridge in one leg.
- The transition of V_{ref} from one sector to another or from one triangle to another requires none or the minimum number of switching.

The switching sequence used in this paper consists of 7 segments in each PWM period; in each segment one vector is applied. To meet the general requirements for the switching sequence mentioned above, the following consideration should be taken into account when choosing the vectors. The vector that is applied in the first segment must be always the one who has an even number of switching (two mean switching patterns). The next vector must be chosen in a way such that only one cell in one leg is switched to obtain the new vector. The same thing must be done in choosing the third vector. The fourth vector should be same as the first one but obtained by the other mean switching pattern. The fifth, sixth and seventh vectors must be same as the third, the second, the first respectively. To illustrate the switching sequence that is used in this paper, Figure 5.a, Figure 5.b, Figure 6.a, Figure 6.b, Figure 7.a, Figure 7b, Figure 8.a, Figure 8.b are used. If the reference voltage V_{ref} exists in ΔCBD and $V_{D\alpha} + V_{D\beta}$ is even, the switching sequence will be (2,0,-3),(2,0,-2),(3,0,-2).(3,1,-2),(3,0,-2),(2,0,-2),(2,0,-3). This case is named by type 0 in the simulation.
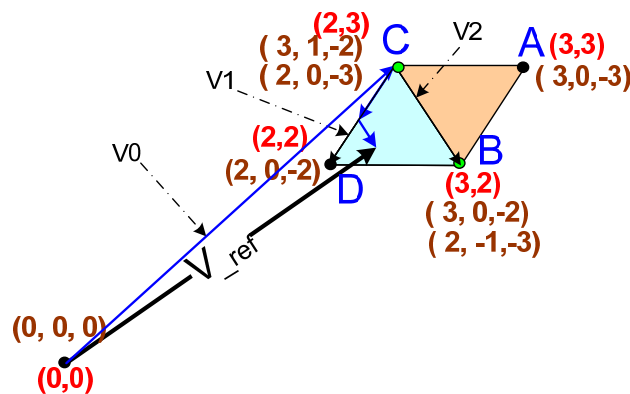

Figure 5.a. Switching sequence used in SVPWM for the multilevel converter

Figure 5.b. Timing diagram for SVPWM for the multilevel converter

If the reference voltage V$_{ref}$ exists in ΔCBA and V$_{D\alpha}$ + V$_{D\beta}$ is even, the switching sequence will be (2,0,-3), (3,0,-3), (3,0,-2), (3,1,-2), (3,0,-2), (3,0,-3), (2,0,-3). This case is named by type 1 in the simulation.

Figure 6.a. Switching sequence used in SVPWM for the multilevel

Figure 6.b. Timing diagram for SVPWM for the multilevel

If the reference voltage V$_{ref}$ exists in ΔCBD and V$_{D\alpha}$ + V$_{D\beta}$ is odd, the switching sequence will be (1,0,-2), (2,0,-2), (2,1,-2). (2,1,-1), (2,1,-1), (2,0,-2), (1,0,-2). This case is named by type 1 in the simulation.

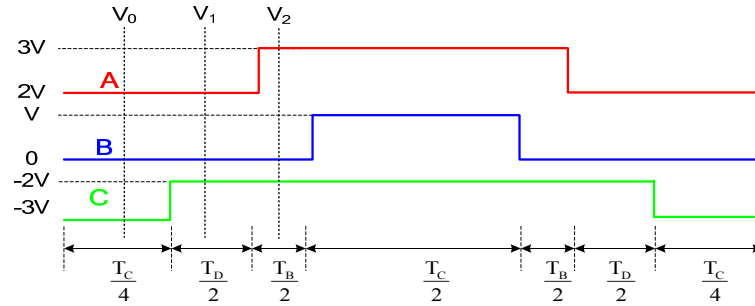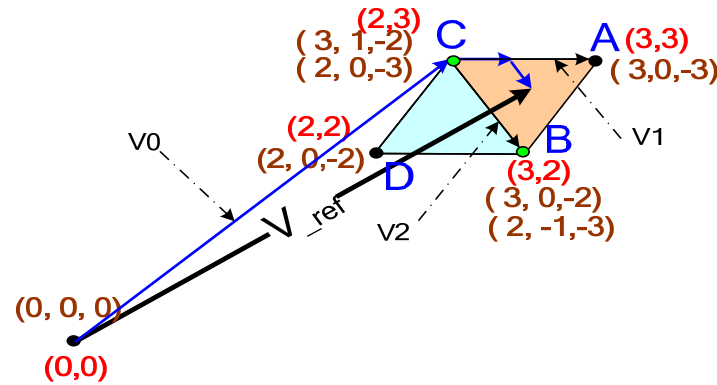Figure 7.a. Switching sequence used in SVPWM for the multilevel converter
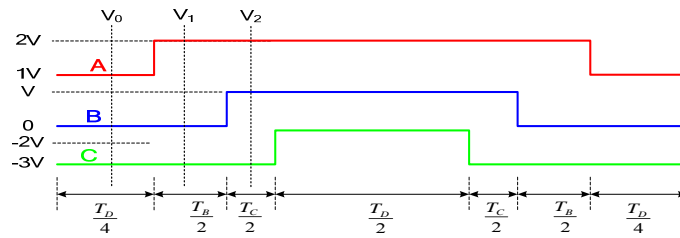
Figure 7.b. Timing diagram for SVPWM for the multilevel converter

If the reference voltage V_{ref} exists in ΔCBA and $V_{D\alpha} + V_{D\beta}$ is odd, the switching sequence will be (2,0,-3), (2,0,-2), (2,1,-2), (3,1,-2), (2,1,-2), (2,0,-2), (2,0,-3). This case is named by type 3 in the simulation.

Figure 8.a. Switching sequence used in SVPWM for the multilevel

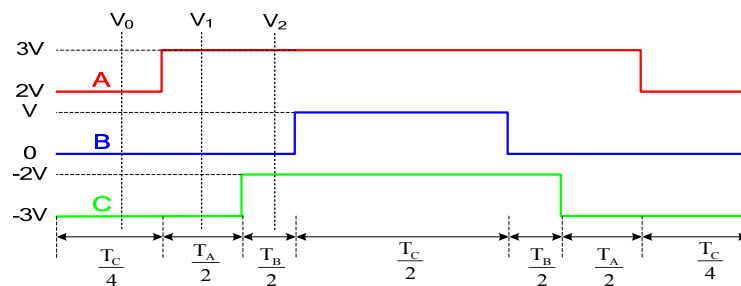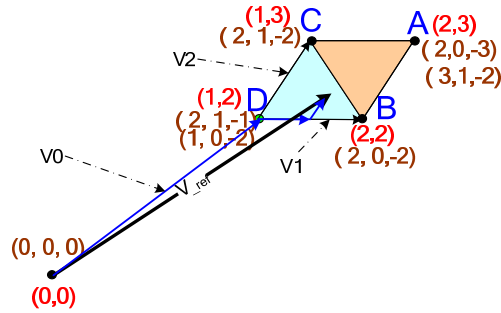Figure 8.b. Timing diagram for SVPWM for the multilevel

Applying the same rules that are used in the examples shown in Figure 5.a, Figure 6.a, Figure 7.a and Figure 8.a in choosing the switching sequence, the switching sequence for the reference voltage existing in sector 1 is given in table 2 where $(V_{D\alpha}, V_{D\beta})$ are calculated using (3, 4):

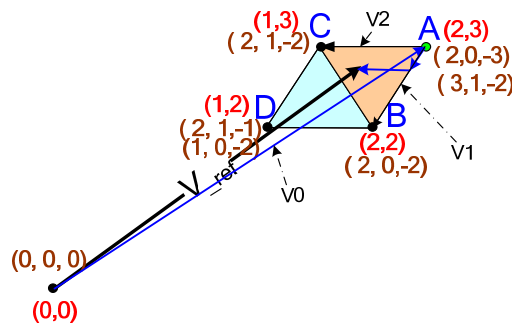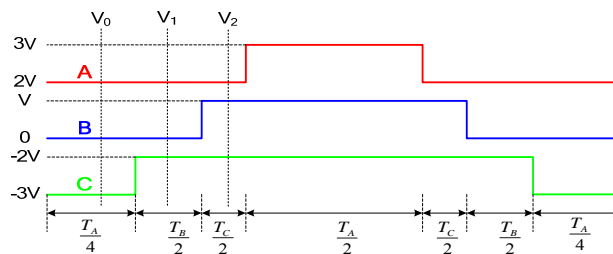Table 2 Switching sequence in sector 1 for SVPWM used in the multilevel converter

$(V_{D\alpha},V_{D\beta})$		V0/4	V1/2	V2/2	V0/2	V2/2	V1/2	V0/4
				SECTOR 1				
(0,0)	ΔBCD	(0,0,-1)	(0,0,0)	(1,0,0)	(1,1,0)	(1,0,0)	(0,0,0)	(0,0,-1)
	ΔBCA	(0,0,-1)	(1,0,-1)	(1,0,0)	(1,1,0)	(1,0,0)	(1,0,-1)	(0,0,-1)
(1,0)	ΔBCD	(0,-1,-1)	(1,-1,-1)	(1,0,-1)	(1,0,0)	(1,0,-1)	(1,-1,-1)	(0,-1,-1)
	ΔBCA	(1,-1,-2)	(1,-1,-1)	(1,0,-1)	(1,0,0)	(1,0,-1)	(1,-1,-1)	(1,-1,-2)
(2,0)	ΔBCD	(1,-1,-2)	(1,-1,-1)	(2,-1,-1)	(2,0,-1)	(2,-1,-1)	(1,-1,-1)	(1,-1,-2)
	ΔBCA	(1,-1,-2)	(2,-1,-2)	(2,-1,-1)	(2,0,-1)	(2,-1,-1)	(2,-1,-2)	(1,-1,-2)
(3,0)	ΔBCD	(1,-2,-2)	(2,-2,-2)	(2,-1,-2)	(2,-1,-1)	(2,-1,-2)	(2,-2,-2)	(1,-2,-2)
	ΔBCA	(2,-2,-3)	(2,-2,-2)	(2,-1,-2)	(3,-1,-2)	(2,-1,-2)	(2,-2,-2)	(2,-2,-3)
(4,0)	ΔBCD	(2,-2,-3)	(2,-2,-2)	(3,-2,-2)	(3,-1,-2)	(3,-2,-2)	(2,-2,-2)	(2,-2,-3)
	ΔBCA	(2,-2,-3)	(3,-2,-3)	(3,-2,-2)	(3,-1,-2)	(3,-2,-2)	(3,-2,-3)	(2,-2,-3)
(5,0)	ΔBCD	(2,-3,-3)	(3,-3,-3)	(3,-2,-3)	(3,-2,-2)	(3,-2,-3)	(3,-3,-3)	(2,-3,-3)
(0,1)	ΔBCD	(0,0,-1)	(1,0,-1)	(1,1,-1)	(1,1,0)	(1,1,-1)	(1,0,-1)	(0,0,-1)
	ΔBCA	(1,0,-2)	(1,0,-1)	(1,1,-1)	(2,1,-1)	(1,1,-1)	(1,0,-1)	(1,0,-2)
(1,1)	ΔBCD	(1,0,-2)	(1,0,-1)	(2,0,-1)	(2,1,-1)	(2,0,-1)	(1,0,-1)	(1,0,-2)
	ΔBCA	(1,0,-2)	(2,0,-2)	(2,0,-1)	(2,2,-1)	(2,0,-1)	(2,0,-2)	(1,0,-2)
(2,1)	ΔBCD	(1,-1,-2)	(2,-1,-2)	(2,0,-2)	(2,0,-1)	(2,0,-2)	(2,-1,-2)	(1,-1,-2)
	ΔBCA	(2,-1,-3)	(2,-1,-2)	(2,0,-2)	(2,0,-1)	(2,0,-2)	(2,-1,-2)	(2,-1,-3)
(3,1)	ΔBCD	(2,-1,-3)	(2,-1,-2)	(3,-1,-2)	(3,0,-2)	(3,-1,-2)	(2,-1,-2)	(2,-1,-3)
	ΔBCA	(2,-1,-3)	(3,-1,-3)	(3,-1,-2)	(3,0,-2)	(3,-1,-2)	(3,-1,-3)	(2,-1,-3)
(4,1)	ΔBCD	(2,-2,-3)	(3,-2,-3)	(3,-1,-3)	(3,-1,-2)	(3,-1,-3)	(3,-2,-3)	(2,-2,-3)
(0,2)	ΔBCD	(1,1,-2)	(1,1,-1)	(2,1,-1)	(2,2,-1)	(2,1,-1)	(1,1,-1)	(1,1,-2)
	ΔBCA	(1,1,-2)	(2,1,-2)	(2,1,-1)	(2,2,-1)	(2,1,-1)	(2,1,-2)	(1,1,-2)
(1,2)	ΔBCD	(1,0,-2)	(2,0,-2)	(2,1,-2)	(2,1,-1)	(2,1,-2)	(2,0,-2)	(1,0,-2)
	ΔBCA	(2,0,-3)	(2,0,-2)	(2,1,-2)	(3,1,-2)	(2,1,-2)	(2,0,-2)	(2,0,-3)
(2,2)	ΔBCD	(2,0,-3)	(2,0,-2)	(3,0,-2)	(3,1,-2)	(3,0,-2)	(2,0,-2)	(2,0,-3)
	ΔBCA	(2,0,-3)	(3,0,-3)	(3,0,-2)	(3,1,-2)	(3,0,-2)	(3,0,-3)	(2,0,-3)
(3,2)	ΔBCD	(2,-1,-3)	(3,-1,-3)	(3,0,-3)	(3,0,-2)	(3,0,-3)	(3,-1,-3)	(2,-1,-3)
(0,3)	ΔBCD	(1,1,-2)	(2,1,-2)	(2,2,-2)	(2,2,-1)	(2,2,-2)	(2,1,-2)	(1,1,-2)
	ΔBCA	(2,1,-3)	(2,1,-2)	(3,1,-2)	(3,2,-2)	(3,1,-2)	(2,1,-2)	(2,1,-3)
(1,3)	ΔBCD	(2,1,-3)	(2,1,-2)	(3,1,-2)	(3,2,-2)	(3,1,-2)	(2,1,-2)	(2,1,-3)
	ΔBCA	(2,1,-3)	(3,1,-3)	(3,1,-2)	(3,2,-2)	(3,1,-2)	(3,1,-3)	(2,1,-3)
(2,3)	ΔBCD	(2,0,-3)	(3,0,-3)	(3,1,-3)	(3,1,-2)	(3,1,-3)	(3,0,-3)	(2,0,-3)
(0,4)	ΔBCD	(2,2,-3)	(2,2,-2)	(3,2,-2)	(3,3,-2)	(3,2,-2)	(2,2,-2)	(2,2,-3)
	ΔBCA	(2,2,-3)	(2,2,-2)	(3,2,-2)	(3,3,-2)	(3,2,-2)	(2,2,-2)	(2,2,-3)
(1,4)	ΔBCD	(2,1,-3)	(3,1,-3)	(3,2,-3)	(3,2,-2)	(3,2,-3)	(3,1,-3)	(2,1,-3)
(0,5)	ΔBCD	(2,2,-3)	(3,2,-3)	(3,3,-3)	(3,3,-2)	(3,3,-3)	(3,2,-3)	(2,2,-3)

2.3. Calculating the Dwell Time

The dwell time calculations depend on whether $V_{D\alpha} + V_{D\beta}$ is odd or even and also whether the reference vector exists in ΔCBD or ΔCBA as following:

1. $V_{D\alpha} + V_{D\beta}$ is even and the reference voltage exists in ΔCBD (type 0):

$$\begin{cases} T_D = \left(1 - (V_{\alpha ref} - V_{D\alpha}) - (V_{\beta ref} - V_{D\beta})\right)T \\ \quad T_B = (V_{\alpha ref} - V_{D\alpha})T \\ \quad\quad T_C = T - T_B - T_D \end{cases} \tag{7}$$

2. $V_{D\alpha} + V_D$ is even and the reference voltage exists in ΔCBA (type 1) :

$$\begin{cases} T_A = \left((V_{\alpha ref} - V_{D\alpha}) - (V_{\beta ref} - V_{D\beta}) - 1\right)T \\ \quad T_B = \left(V_{D\beta} + 1 - V_{\beta ref}\right)T \\ \quad\quad T_C = T - T_A - T_B \end{cases} \tag{8}$$

3. $V_{D\alpha} + V_{D\beta}$ is odd and the reference voltage exists in ΔCBD (type 2):

$$\begin{cases} T_B = (V_{\alpha ref} - V_{D\beta})T \\ T_C = (V_{\beta ref} - V_{D\beta})T \\ T_D = T - T_B - T_C \end{cases} \tag{9}$$

4. $V_{D\alpha} + V_{D\beta}$ is odd and the reference voltage exists in ΔCBA (type3):

$$\begin{cases} T_B = (V_{D\beta} + 1 - V_{\beta ref})T \\ T_C = (V_{D\alpha} + 1 - V_{\alpha ref})T \\ T_A = T - T_B - T_C \end{cases} \tag{10}$$

5. The algorithm that illustrates the procedure for applying the space vector modulation in a multilevel inverter will be:
    -   Transform the reference voltage to sector 1 by subtracting the value (n-1)*60° from the angle of the reference voltage where n is the number of sector.
    -   Calculate $V_{\alpha ref}, V_{\beta\_ref}$ according to (1), (2)
    -   Specify the triangle where the reference voltage exists according to (5),(6)
    -   Choose the switching sequence from Table 2
    -   Calculate the dwell time according to (7), (8), (9), (10)
    -   Transform the switching sequence to the sector where the reference voltage exists according to Table 3

Table 3. Relation of switching states in different sectors

Sector	Switching state		
1	Va	Vb	Vc
2	-Vb	-Vc	-Va
3	Vc	Va	Vb
4	-Va	-Vb	-Vc
5	Vb	Vc	Va
6	-Vc	-Va	-Vb

2.4. Sensored Operation of a Cascade H-Bridge Multilevel Inverter PMSM Drive

Figure 9 shows the vector control structure proposed for the cascade H-Bridge multilevel inveter PMSM drive system when using an encoder for feedback i.e in sensored mode. The simulation of the cascade H-Bridge multilevel inveter PMSM drive has been carried out using the SABER simulation package. The simulation results in Figure 10 show the feasibility of the system. It can be seen from the figure that at low speeds the demand voltage is small and hence only the H-Bridges synthesized V(200V) are used to generate such a voltage. When the speed is increased, the demand voltage is increased and all the H-Bridges are switched in order to generate this demand voltage in a way that the H-Bridge synthized the voltage 2V(400V) has switching frequency equals the fundamental
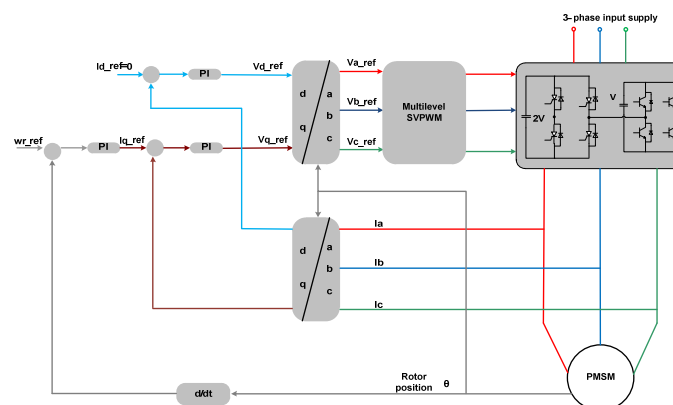

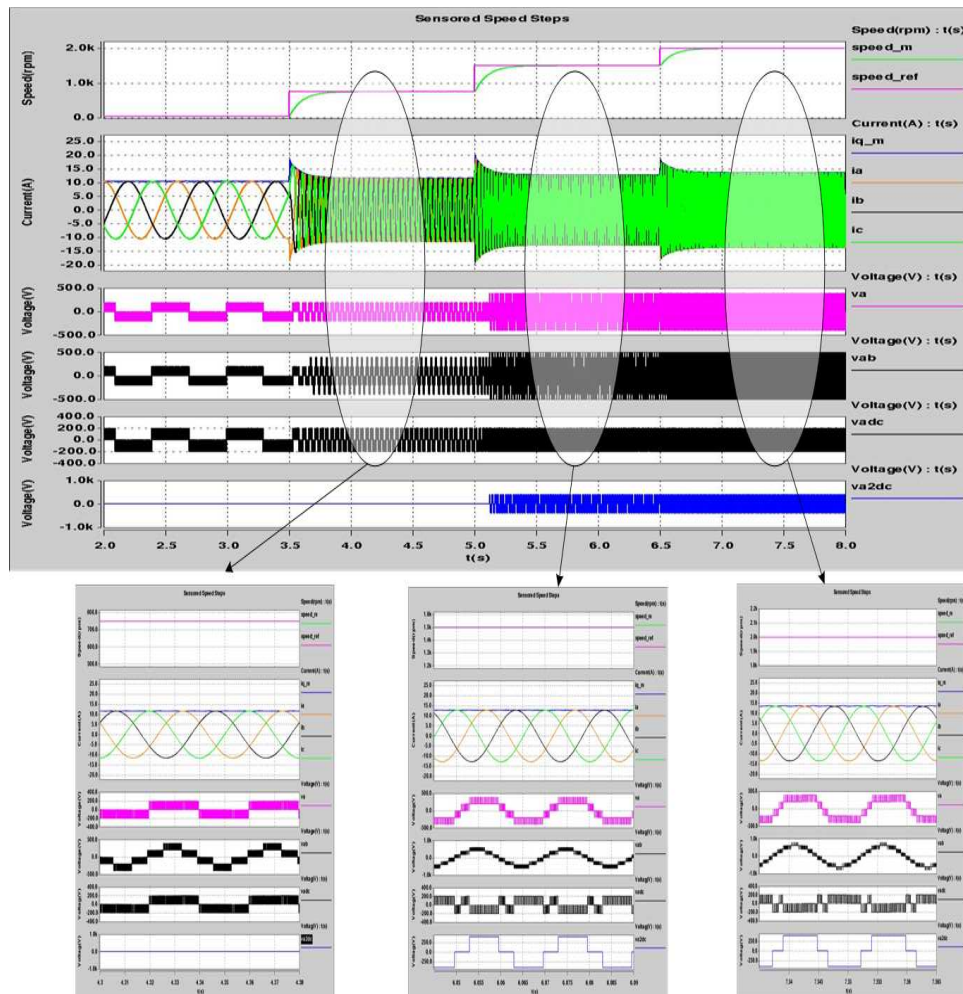Figure 9. Vector control topology using multi level space vector PWM for multilevel inverter

Figure 10. Speed steps in sensored mode using Space vector modulation for 7-level inverter

3.   TRACKING THE SALIENCY IN MULTILEVEL INVERTER

It is possible to track the saliency using the PWM signals in a multilevel inverter in similar way to that introduced in [6] for a 2-level inverter without interrupting the multilevel inverter normal operation because of the test vectors. Figure 11 shows the Type0 switching sequence. The stator circuit when the vectors V1, V2 and V0 are applied are shown in Figure 12.a, 12.b and 12.c respectively.
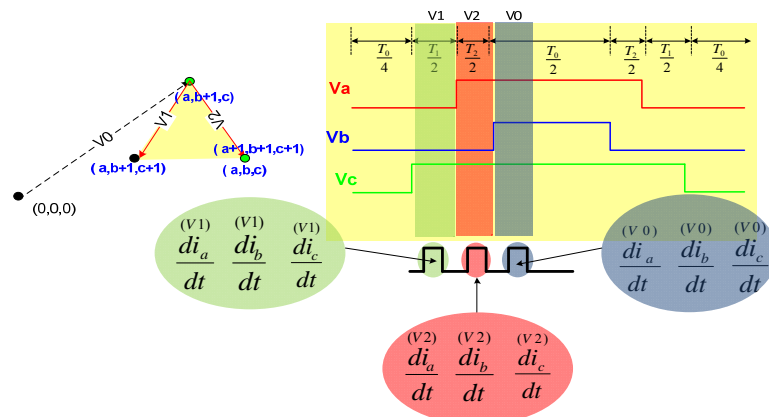

Figure 11. Switching sequence for Type 0 in sector 1 in the multilevel space diagram
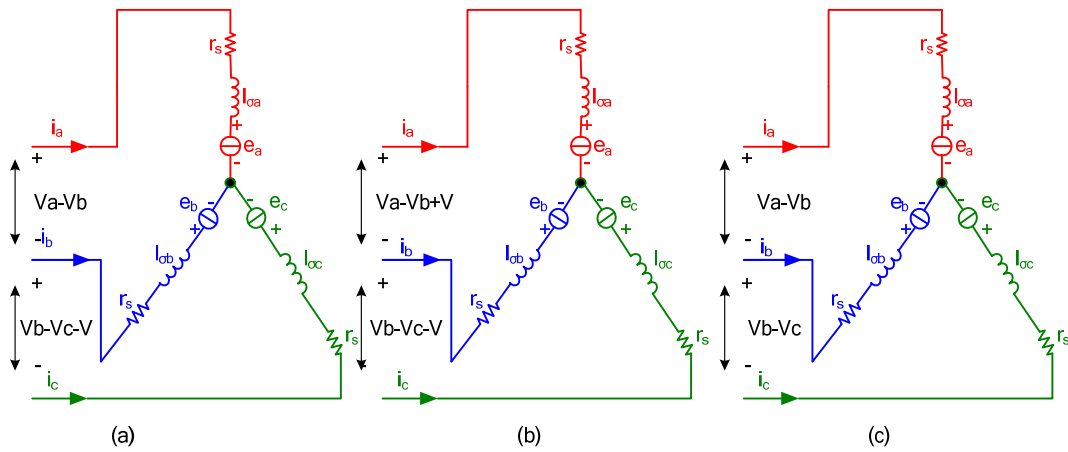
Figure 12. Stator circuits when: (a) V1 is applied; (b) V2 is applied; (c) V0 is applied

Using the circuit in Figure 12.a, the following equations hold true:

$$Va - Vb = l_{\sigma a} * \frac{di_a^{(V1)}}{dt} - l_{\sigma b} * \frac{di_b^{(V1)}}{dt} \qquad (11)$$

$$Vb - Vc - V = l_{\sigma b} * \frac{di_b^{(V1)}}{dt} - l_{\sigma c} * \frac{di_c^{(V1)}}{dt} \qquad (12)$$

$$Vc - Va + V = l_{\sigma c} * \frac{di_c^{(V1)}}{dt} - l_{\sigma a} * \frac{di_a^{(V1)}}{dt} \qquad (13)$$

The following equations are obtained using Figure 12.b:

$$Va - Vb + V = l_{\sigma a} * \frac{di_a^{(V2)}}{dt} - l_{\sigma b} * \frac{di_b^{(V2)}}{dt} \qquad (14)$$

$$Vb - Vc - V = l_{\sigma b} * \frac{di_b^{(V2)}}{dt} - l_{\sigma c} * \frac{di_c^{(V2)}}{dt} \qquad (15)$$

$$Vc - Va = l_{\sigma c} * \frac{di_c^{(V2)}}{dt} - l_{\sigma a} * \frac{di_a^{(V2)}}{dt} \qquad (16)$$

Finally when V0 is applied as shown in Figure 12.c, the following equations hold true:

$$Va - Vb = l_{\sigma a} * \frac{di_a^{(V0)}}{dt} - l_{\sigma b} * \frac{di_b^{(V0)}}{dt} \qquad (17)$$

$$Vb - Vc = l_{\sigma b} * \frac{di_b^{(V0)}}{dt} - l_{\sigma c} * \frac{di_c^{(V0)}}{dt} \qquad (18)$$

$$Vc - Va = l_{\sigma c} * \frac{di_c^{(V0)}}{dt} - l_{\sigma a} * \frac{di_a^{(V0)}}{dt} \qquad (19)$$

All the above equations are obtained based on two assumptions. The first one is that the voltage drop across the stator resistances are small and can be neglected. The second one is that back emf can be cancelled if the time separation between the vectors is small.
Subtracting (17, 18 and 19) from (14, 15 and 16) respectively yields:

$$0 = l_{\sigma a} * \left(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) - l_{\sigma b} * \left(\frac{di_b^{(V1)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) \tag{20}$$

$$-V = l_{\sigma b} * \left(\frac{di_b^{(V1)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) - l_{\sigma c} * \left(\frac{di_c^{(V1)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) \tag{21}$$

$$V = l_{\sigma c} * \left(\frac{di_c^{(V1)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) - l_{\sigma a} * \left(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) \tag{22}$$

Repeating the previous procedure with equations (11, 12 and13) gives:

$$V = l_{\sigma a} * \left(\frac{di_a^{(V2)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) - l_{\sigma b} * \left(\frac{di_b^{(V2)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) \tag{23}$$

$$-V = l_{\sigma b} * \left(\frac{di_b^{(V2)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) - l_{\sigma c} * \left(\frac{di_c^{(V2)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) \tag{24}$$

$$0 = l_{\sigma c} * \left(\frac{di_c^{(V2)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) - l_{\sigma a} * \left(\frac{di_a^{(V2)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) \tag{25}$$

Multiplying (20) by $(l_{\sigma c})$, (21) by $(l_{\sigma a})$ and (22) by $(l_{\sigma b})$ and then subtracting the new equations from each other yields:

$$-l_{\sigma b} * V = \left(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt}\right)(l_{\sigma a} \, l_{\sigma b} + \, l_{\sigma b} l_{\sigma c} + l_{\sigma c} l_{\sigma a}) \tag{26}$$

$$-l_{\sigma a} * V = \left(\frac{di_b^{(V1)}}{dt} - \frac{di_b^{(V0)}}{dt}\right)(l_{\sigma a} \, l_{\sigma b} + \, l_{\sigma b} l_{\sigma c} + l_{\sigma c} l_{\sigma a}) \tag{27}$$

$$(l_{\sigma a} + l_{\sigma b}) * V = \left(\frac{di_c^{(V1)}}{dt} - \frac{di_c^{(V0)}}{dt}\right)(l_{\sigma a} \, l_{\sigma b} + \, l_{\sigma b} l_{\sigma c} + l_{\sigma c} l_{\sigma a}) \tag{28}$$

Substituting $l_{\sigma a} \, l_{\sigma b} + \, l_{\sigma b} l_{\sigma c} + l_{\sigma c} l_{\sigma a}$ by $3L_0(1 - \left(\frac{\Delta L}{2L_0}\right)^2)$ yields:

$$\left(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) = \frac{-V * l_{\sigma b}}{3L_0(1 - \left(\frac{\Delta L}{2L_0}\right)^2)} \tag{29}$$

$$\left(\frac{di_b^{(V1)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) = \frac{-V * l_{\sigma a}}{3L_0(1 - \left(\frac{\Delta L}{2L_0}\right)^2)} \tag{30}$$

$$\left(\frac{di_c^{(V1)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) = \frac{V * (l_{\sigma a} + l_{\sigma b})}{3L_0(1 - \left(\frac{\Delta L}{2L_0}\right)^2)} \tag{31}$$

By assuming a constant $C = \frac{3(1 - \left(\frac{\Delta L}{2L_0}\right)^2)}{V}$, (29, 30 and 31) can be rearranged for the position signals:

$$Pa = -1 - C\left(\frac{di_b^{(V1)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) \tag{32}$$

$$Pb = -1 - C\left(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) \tag{33}$$

$$Pc = 2 - C\left(\frac{di_c^{(V1)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) \tag{34}$$

In the same way (23, 34 and 25) yields:

$$Pa = -1 + C\left(\frac{di_c^{(V2)}}{dt} - \frac{di_c^{(V0)}}{dt}\right) \tag{35}$$

$$Pb = 2 + C\left(\frac{di_b^{(V2)}}{dt} - \frac{di_b^{(V0)}}{dt}\right) \tag{36}$$

$$Pc = -1 + C\left(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt}\right) \tag{37}$$

Comparing these equations to the positional equations obtained in table 4 (position equation obtained using SVPWM in a 2 level inverter) [6], it is quite clear that (32, 33 and 34) are exactly the same as those obtained by applying vectors V_5 and V_0 in table 4. Also (35, 36 and 37) are exactly the same as those obtained by applying V_6 and V_0 in table 4.

This result can be understood by imagining that the Type 0 triangle in Figure 5.a is similar to sector 5 in a 2 level SVPWM switching state diagram. Also the active vectors V1 and V2 in the multilevel SVPWM switching sequence in this example are similar to V5 and V6 respectively of the 2-level SVPWM switching sequence. Based on that the scalar position equations for Type1, Type2 and Type 3 triangles in sector 1 for multilevel SVPWM switching state diagram will be the same as those obtained for sector 6, sector 1, and sector 4 in 2-level SVPWM switching state diagram as shown in Table5.

Table 4. Selection of pa, pb and pc for a star-connected machine with a 2 level SVPWM

	p_a	p_b	p_c
V_1+V_0	$2 - c(\frac{di_a^{(V1)}}{dt} - \frac{di_a^{(V0)}}{dt})$	$-1 - c(\frac{di_c^{(V1)}}{dt} - \frac{di_c^{(V0)}}{dt})$	$-1 - c(\frac{di_b^{(V1)}}{dt} - \frac{di_b^{(V0)}}{dt})$
V_2+V_0	$-1 + c(\frac{di_b^{(V2)}}{dt} - \frac{di_b^{(V0)}}{dt})$	$-1 + c(\frac{di_a^{(V2)}}{dt} - \frac{di_a^{(V0)}}{dt})$	$2 + c(\frac{di_c^{(V2)}}{dt} - \frac{di_c^{(V0)}}{dt})$
V_3+V_0	$-1 - c(\frac{di_c^{(V3)}}{dt} - \frac{di_c^{(V0)}}{dt})$	$2 - c(\frac{di_b^{(V3)}}{dt} - \frac{di_b^{(V0)}}{dt})$	$-1 - c(\frac{di_a^{(V3)}}{dt} - \frac{di_a^{(V0)}}{dt})$
V_4+V_0	$2 + c(\frac{di_a^{(V4)}}{dt} - \frac{di_a^{(V0)}}{dt})$	$-1 + c(\frac{di_c^{(V4)}}{dt} - \frac{di_c^{(V0)}}{dt})$	$-1 + c(\frac{di_b^{(V4)}}{dt} - \frac{di_b^{(V0)}}{dt})$
V_5+V_0	$-1 - c(\frac{di_b^{(V5)}}{dt} - \frac{di_b^{(V0)}}{dt})$	$-1 - c(\frac{di_a^{(V5)}}{dt} - \frac{di_a^{(V0)}}{dt})$	$2 - c(\frac{di_c^{(V5)}}{dt} - \frac{di_c^{(V0)}}{dt})$
V_6+V_0	$-1 + c(\frac{di_c^{(V6)}}{dt} - \frac{di_c^{(V0)}}{dt})$	$2 + c(\frac{di_b^{(V6)}}{dt} - \frac{di_b^{(V0)}}{dt})$	$-1 + c(\frac{di_a^{(V6)}}{dt} - \frac{di_a^{(V0)}}{dt})$

Table 5. Selection of pa, pb and pc for a star-connected machine for triangles located in sector 1 in multilevel SVPWM

Triangle	Vectors	Pa	Pb	Pc
Type0 ΔBCD	V1+Vo	$-1-c(\frac{di_b^{(V1)}}{dt}-\frac{di_b^{(V0)}}{dt})$	$-1-c(\frac{di_a^{(V1)}}{dt}-\frac{di_a^{(V0)}}{dt})$	$2-c(\frac{di_c^{(V1)}}{dt}-\frac{di_c^{(V0)}}{dt})$
	V2+Vo	$-1+c(\frac{di_c^{(V2)}}{dt}-\frac{di_c^{(V0)}}{dt})$	$2+c(\frac{di_b^{(V2)}}{dt}-\frac{di_b^{(V0)}}{dt})$	$-1+c(\frac{di_a^{(V2)}}{dt}-\frac{di_a^{(V0)}}{dt})$
Type1 ΔBCA	V1+Vo	$2-c(\frac{di_a^{(V1)}}{dt}-\frac{di_a^{(V0)}}{dt})$	$-1-c(\frac{di_c^{(V1)}}{dt}-\frac{di_c^{(V0)}}{dt})$	$-1-c(\frac{di_b^{(V1)}}{dt}-\frac{di_b^{(V0)}}{dt})$
	V2+Vo	$-1+c(\frac{di_c^{(V2)}}{dt}-\frac{di_c^{(V0)}}{dt})$	$2+c(\frac{di_b^{(V2)}}{dt}-\frac{di_b^{(V0)}}{dt})$	$-1+c(\frac{di_a^{(V2)}}{dt}-\frac{di_a^{(V0)}}{dt})$
Type 2 ΔBCD	V1+Vo	$2-c(\frac{di_a^{(V1)}}{dt}-\frac{di_a^{(V0)}}{dt})$	$-1-c(\frac{di_c^{(V1)}}{dt}-\frac{di_c^{(V0)}}{dt})$	$-1-c(\frac{di_b^{(V1)}}{dt}-\frac{di_b^{(V0)}}{dt})$
	V2+Vo	$-1+c(\frac{di_b^{(V2)}}{dt}-\frac{di_b^{(V0)}}{dt})$	$-1+c(\frac{di_a^{(V2)}}{dt}-\frac{di_a^{(V0)}}{dt})$	$2+c(\frac{di_c^{(V2)}}{dt}-\frac{di_c^{(V0)}}{dt})$
Type 3 ΔBCA	V1+Vo	$-1-c(\frac{di_b^{(V1)}}{dt}-\frac{di_b^{(V0)}}{dt})$	$-1-c(\frac{di_a^{(V1)}}{dt}-\frac{di_a^{(V0)}}{dt})$	$2-c(\frac{di_c^{(V1)}}{dt}-\frac{di_c^{(V0)}}{dt})$
	V2+Vo	$2+c(\frac{di_a^{(V2)}}{dt}-\frac{di_a^{(V0)}}{dt})$	$-1+c(\frac{di_c^{(V2)}}{dt}-\frac{di_c^{(V0)}}{dt})$	$-1+c(\frac{di_b^{(V2)}}{dt}-\frac{di_b^{(V0)}}{dt})$

One point should be taken in consideration is that this table is correct in sector 1 only. In other sectors the triangles Type0, Type1, Type2 and Type 3 will no longer be similar to sector 5, sector 6, sector1 and sector 4 of the 2-level switching state diagram and so the position scalar equations will be slightly different but still can be deduced directly from Table 4 as the only change will be the sector that the triangle will be similar to. For example, Type 0 is similar to sector 5 if V_ref exists in sector 1 of the multilevel inverter SVPWM switching state diagram. And it will be similar to sector 1 if V_ref exists in sector 3 of the multilevel SVPWM switching state diagram as shown in Figure 13. Hence the scalar position equations will be chosen from table 5 accordingly.
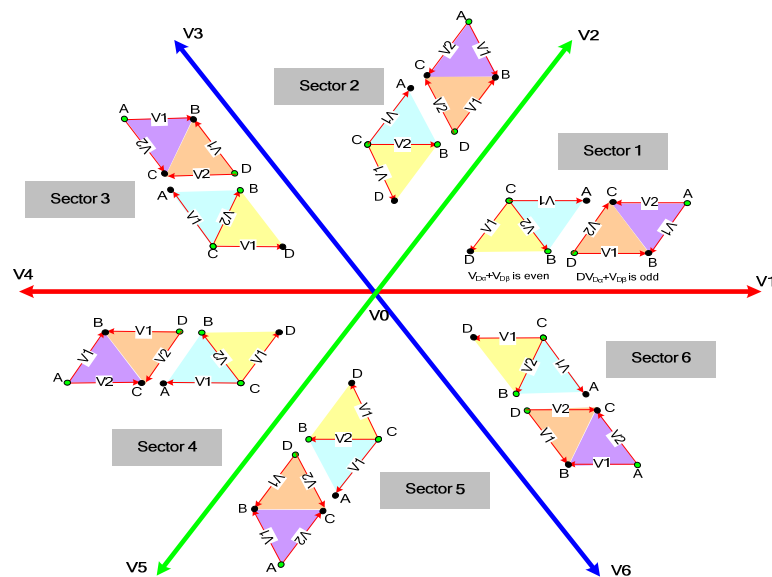

Figure 13. Change of the way the switching sequence is defined in different sectors when using multilevel SVPWM

The above equations has been implemented using saber simulator program to track the saturation saliency (2fe) in PM motor at differerent speeds as shown in Figure 14 where the equation to estimate the position is chosen according to the value of Type. From The figure it is quite clear that this scheme has tracked the saturation saliency whatever is the speed. Also, the minimum pulse width time is chosen to be 10μs which is a realistic choice.

4. FULLY SENSORLESS SPEED CONTROL

The speed control for a PM machine has been implemented in simulation in the Saber modelling environment. The estimated position signals Pa, Pb and Pc from obtained from table 5 are used as the input to a mechanical observer [14] to obtain the speed $\omega^{\wedge}$ and a "cleaned" position $\theta_r^{\wedge}$. Note the simulation includes a minimum pulse width of 10us when di/dt measurements are made – a realistic values seen from experimental results of [6, 9]. This estimated speed $\omega^{\wedge}$ and position $\theta_r^{\wedge}$ are used to obtain a fully sensorless speed control as shown in Figure 15.
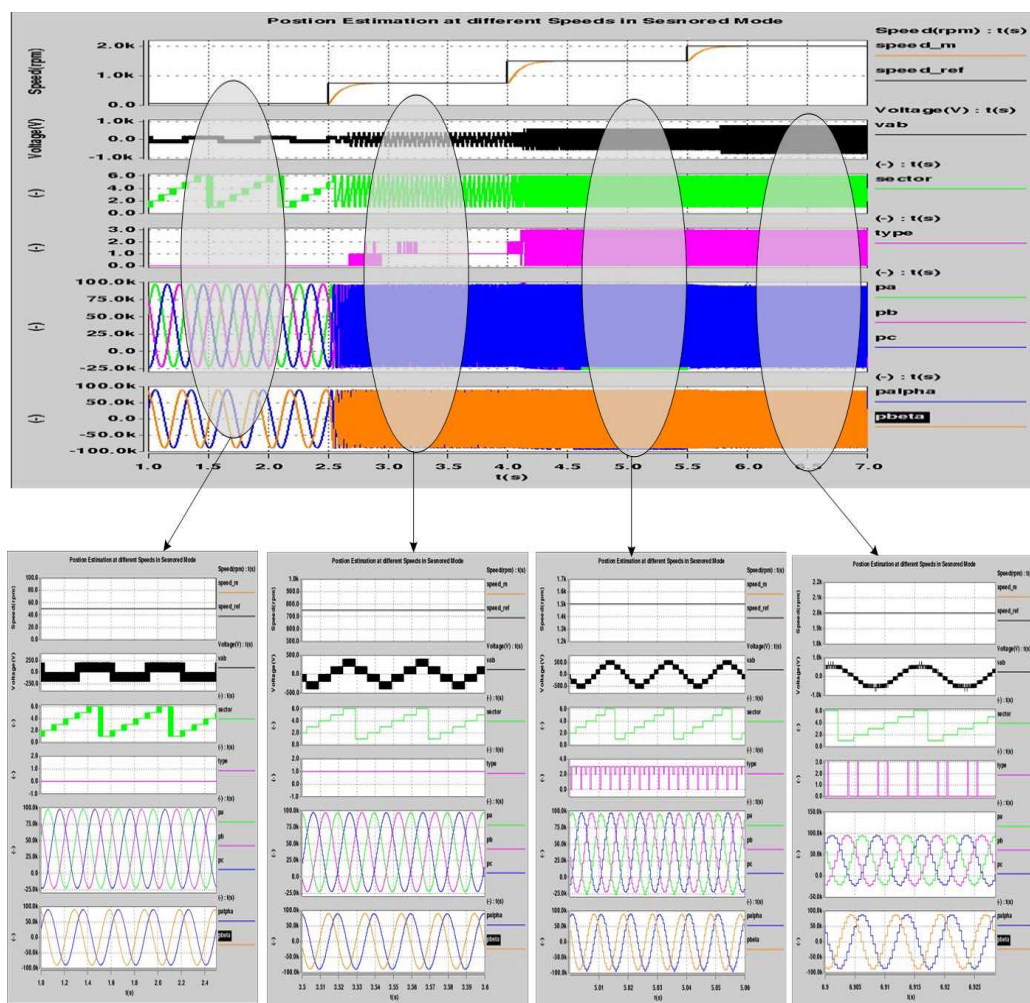

Figure 14. Position estimation in multilevel inverter

4.1. Low Speed

Figures 16 shows the results of full sensorless speed control under full loaded conditions using the proposed method. A speed step change from 0 to 15 to -15 back to 0 rpm at full load was demanded. The measured speed and position seen in the figure proved that the system responded to the speed steps with good dynamic response and good steady state behavior.
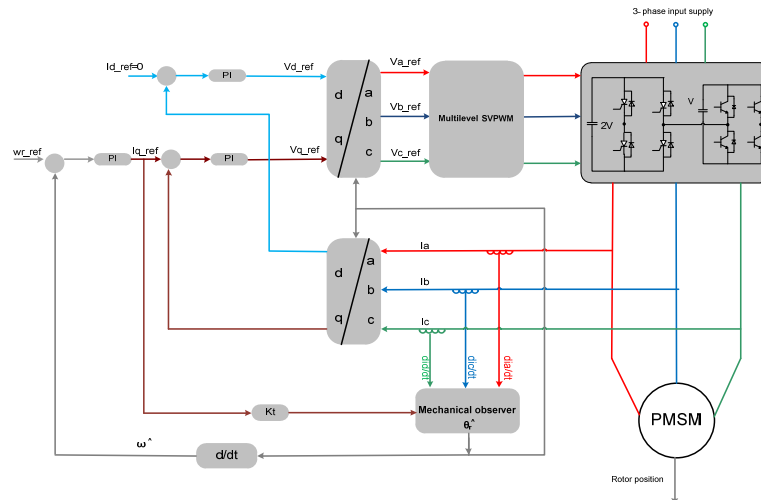
Figure 15. The sensorless vector control structure for the cascade multilevel inverter PMSM
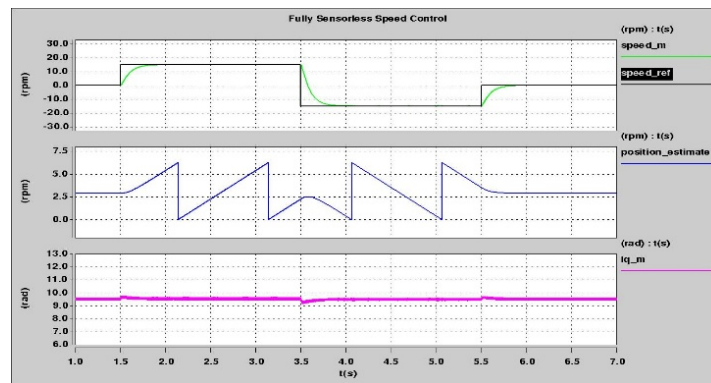

Figure 16. Fully Sensorless Speed Steps between 0,15,-15 and 0 rpm at full load

4.2. High Speed

One of the advantages of this method is that its ability to work in sensorless mode over a wide speed range as all the di/dt signals are sample in one PWM period and hence the effect of the back EMF will be very small even at high speed. This is shown Figure 17 where the motor responded to a speed steps between 0 to 2000 rpm at no load. The performance of the system in this case is good.
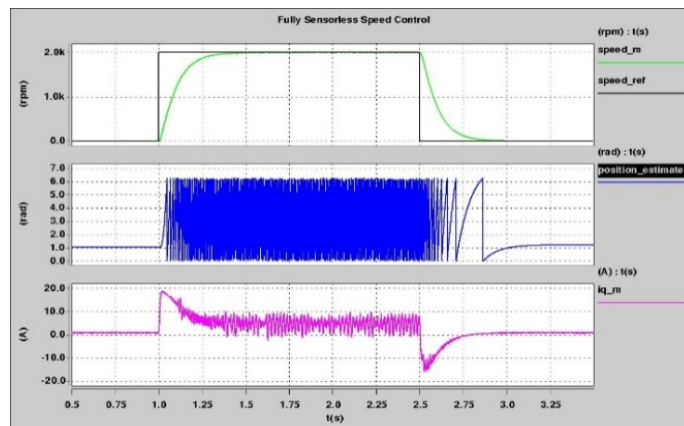

Figure 17. Fully Sensorless Speed Steps between 0 and 2000 rpm at no load

4.3. Load Disturbance

Figure 18 demonstrates the visibility of the fully sensorless system under the condition of applying a full load disturbance at very load speed. The system recovered at very short time.
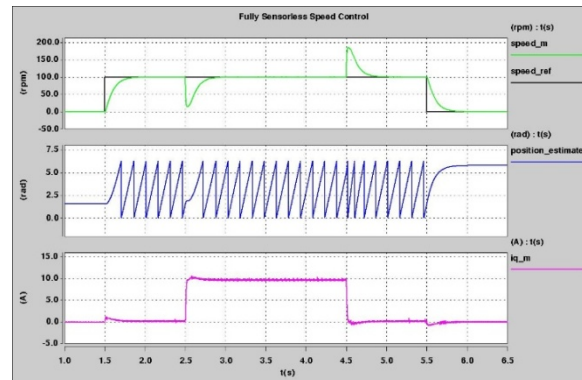

Figure 18. Fully Sensorless Full load steps Steps at 100 rpm

5. 5 IMPROVEMENT IN CURRENT DISTORTION

In this part, A comparison between the total harmonic distortion due to the minimum pulse width introduced to the operation of both a multilevel inverter and a 2-level inverter with the normal operation of both inverters at different speeds and load conditions is done. The minimum pulse width in both converters were chosen to be 10μs. Tables 5 and 6 show in details how many times the vectors V1,V2 and V0 needed to be extended in both the 2-level converter and the multilevel converter. This calculation is done in 4 second period of time. As the switching frequency is 5kHz, this means that the number of PWM cycles in this period of time is 20000 and so, the number of times the position is sampled during this period will be 2500 as the position is sampled every 4 PWM periods. From the Tables, it is clear that in the case of multilevel converter, the situation where no extensions are needed happened at lower speed (250 rpm) compared to the 2-level converter (500 rpm) which helps in reducing the current distortion.

Figure 19 shows the current waveforms for both the 2-level converter and multilevel converter operating at 30 rpm and no load with and without pulse extension. Form the current waveform it is quite clear the improvement in the distortion due to the used of small voltage steps for excitations in the case of multilevel inverter.

Table 6. Illustration of number of minimum pules introduced due to different cases at different condition when the motor driven by 2-level converter

		2-Level converter- Full Load						
		Case1	*Case2*	*Case3*	*Case4*	*Case5*	*Case6*	*Case7*
Speed (rpm)	*all*	T0<Tmin T1<Tmin T2>Tmin	T0<Tmin T1>Tmin T2>Tmin	T0<Tmin T1>Tmin T2>Tmin	T0>Tmin T1<Tmin T2<Tmin	T0>Tmin T1<Tmin T2>Tmin	T0>Tmin T1>Tmin T2<Tmin	T0>Tmin T1>Tmin T2>Tmin
15	2500	0	0	0	2500	0	0	0
30	2500	0	0	0	2500	0	0	0
100	2500	0	0	0	2500	0	0	0
250	2500	0	0	0	1600	450	450	0
500	2500	0	0	0	0	900	1000	600
1000	2500	0	0	0	0	500	400	1600
1500	2500	0	0	0	0	300	314	1886
2000	2500	200	300	2000	0	0	0	0

Table 7. Illustration of number of minimum pules introduced due to different cases at different condition when the motor driven by multi-level converter

| peed (rpm)	all	Multi-Level converter- Full Load						
		Case1	Case2	Case3	Case4	Case5	Case6	Case7
		T0<Tmin T1<Tmin T2>Tmin	T0<Tmin T1>Tmin T2<Tmin	T0<Tmin T1>Tmin T2>Tmin	T0>Tmin T1<Tmin T2<Tmin	T0>Tmin T1<Tmin T2>Tmin	T0>Tmin T1>Tmin T2<Tmin	T0>Tmin T1>Tmin T2>Tmin
15	2500	0	2500	0	0	0	0	0
30	2500	0	2500	0	0	0	0	0
100	2500	0	1502	996	0	0	0	0
250	2500	0	0	1300	0	0	602	598
500	2500	0	0	686	0	0	304	1510
1000	2500	0	0	396	0	402	602	1100
1500	2500	100	350	1900	0	100	100	100
2000	2500	200	0	392	298	602	200	808
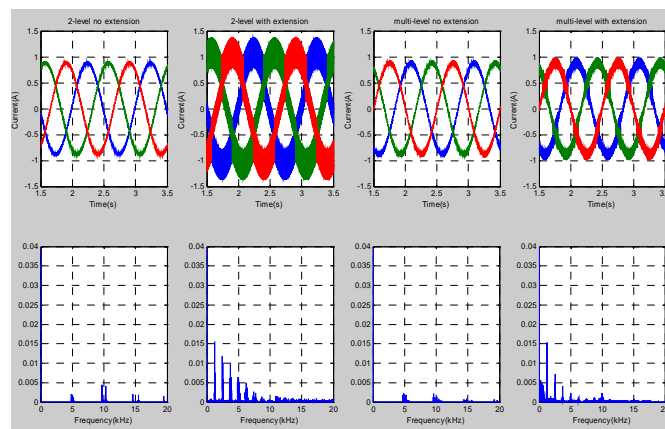
Figure 19. Current waveforms and FFT in 2-level inverter and multilevel inverter at 30 rpm and no load

6. CONCLUSION

This paper has outlined a new scheme for tracking the saliency in ac machines driven by a multilevel inverter using the current transient response due multilevel-inverter switching actions without any need to include additional excitation voltages and without any modification to the normal operation of the multilevel inverter. The equations to track the saliency will be similar to those in 2-level inverter [3]. The new method helps to reduce the current distortion significantly compared to the standard 2-level inverter due to the reduction in excitation voltage. The method can be also implemented to different multilevel topologies such as the diode clamped multilevel inverter and can track both the saturation saliency and the rotor slotting saliency.

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