International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 7, No. 2, June 2016, pp. 450~459
ISSN: 2088-8694

A Novel High Gain SEPIC Converter with the Tapped Inductor Model Operating in Discontinuous Conduction Mode for Power Factor Correction

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Article Info

Article history:

Received Dec 22, 2015
Revised Apr 6, 2015
Accepted Apr 20, 2016

Keyword:

Discontinuous conduction
Power factor correction
SEPIC converter
Tapped inductor model
Zero-current switching
Zero-voltage switching

ABSTRACT

Power factor correction (PFC) has become one of the most active research areas in the field of power electronics due to the surplus power required for various industrial applications around the world. In this work, a novel SEPIC converter with the tapped inductor model operating in discontinuous conduction mode (TI-SEPIC- DCM) is proposed for PFC. The proposed TI-SEPIC-DCM improves the voltage gain through voltage multiplier cell and charge pump circuit. The voltage multiplier cell also helps in attaining the zero-voltage switching (ZVS) and zero-current switching (ZCS), which results in higher switching frequency and size reduction. Moreover, a third order harmonic reduction control loop has been proposed for better harmonic mitigation. The proposed work has been simulated in MATLAB and the results are obtained to validate the significance of the proposed TI-SEPIC-DCM with near unity power factor and reduced harmonics.

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1. INTRODUCTION

Power supplies through active power factor correction (PFC) schemes are have turned out to be essential for several categories of electronic equipment to satisfy harmonic laws and standards, like the IEC 61000-3-2 [1]. PFC is a kind of rectifier which have extensive array of industrial applications like telecommunication and biomedical industries.

The majority of PFC schemes until now implement a boost-type circuit configuration at its front end [2]–[9] owing to its low cost and its high performance in terms of efficiency, simplicity and power factor. Then again, for universal input voltage applications, the boost converter undergoes the complication of lower efficiency and higher total harmonic distortion during low input voltage. Additionally, the boost converter has reasonably high switch voltage stress which is almost same as the output voltage. Also, the boost rectifier has certain shortcomings, like, input–output isolation cannot be implemented with any trouble, the startup inrush current is extremely high, and there is a need of current limiting at some stage in overload conditions.

Moreover, it is well known that the boost converter functioning in Discontinuous Current Mode (DCM) can offer several benefits, like inherent PFC function, extremely simple control, flexible turn-on of the main switch, and decreased diode reversed-recovery losses. On the other hand, the DCM operation necessitates a high-quality boost inductor because it must switch very high peak ripple currents (third harmonic current) and voltages. Thus, a more robust input filter must be utilized for the purpose of suppressing the high-frequency constituents of the pulsating input current, which raises the overall weight and cost of the rectifier. The conventional boost preregulator functioning in DCM is shown in Figure 1.

Besides, numerous PFC topologies in accordance with flyback, buck-boost, and Cuk converters have been available in on-line [10]–[16]. On the other hand, these topologies have an inverting output.

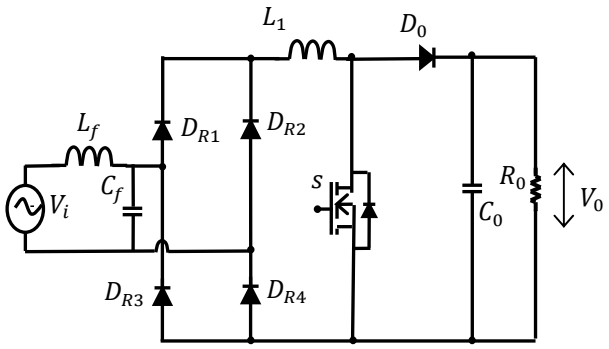


Figure 1. The conventional boost preregulator functioning in DCM

In contrast, SEPIC rectifier has quite a lot of benefits like: Step up and step down capabilities besides magnetic coupling that will bring about reduction in input current ripple [16]–[20]. In case of [20], an extensive static gain SEPIC converter operating in Continuous Conduction Mode (CCM) have been formulated for the purpose of increasing the static gain at low input voltage without excessive switch duty-cycle and with decreased switch voltage stress. This has been accomplished through inserting a voltage multiplier cell (DM and CM) in the traditional SEPIC converter as shown in Figure 2.

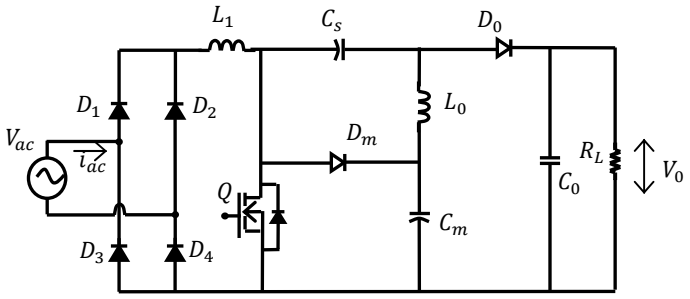


Figure 2. The DCM SEPIC converter

Traditionally, inverters for grid interconnection are realized by a two-stage power processing approach, comprised of a high step-up ac–dc front-end converter with high PFC followed by a grid tied dc–ac inverter. Fact that grid-tied inverter stage needs high dc-bus voltage, the ac–dc stage possibly will require to stepup the low voltage about near unity power factor. Conversely, basic ac–dc converters like boost, buck–boost, Cuk [21-22], Sepic, and Zeta cannot offer high efficiency during the required conversion ratio.

In a quest for higher voltage gain and efficiency, several innovative schemes have been formulated in recent literature. These comprise application of multipliers [23], switched capacitor/ inductor hybrid structures [24], voltage-lift [25], and cascaded boost converters [26]. In general, these schemes bring about increased component count and cost in addition to control complexity. Tapped Inductor (TI) is kinds of converters are an option, which provides simple circuit and low part count. The TI boost (TI-boost) converter [27] can accomplish much more gain than its fundamental counterpart simply by adjusting the turns ratio. TI can be introduced to other conventional dc–dc converters also. TI-flyback [28], [29], TI-cascaded boost [30], TI-SEPIC [31], [32], [35] and TI-ZETA [33] topologies have been reported. The leakage inductance can cause high-voltage spike across the switch, while dissipation of the leakage energy impairs the efficiency. Furthermore, it impedes secondary current, limits the power transfer to the load, and makes the voltage conversion ratio load dependent.

In this work, a novel SEPIC converter with the Tapped Inductor model operating in discontinuous conduction mode (TI-SEPIC-DCM) is proposed for PFC. The proposed TI-SEPIC-DCM improves the voltage gain through voltage multiplier cell and charge pump circuit. The voltage multiplier cell also helps in attaining the zero-voltage switching (ZVS) and zero-current switching (ZCS), which results in higher switching frequency and size reduction.

2. PROPOSED METHODOLOGY

Schematic diagram of the proposed SEPIC converter with TI model operating in DCM (TI-SEPIC-DCM) and adopted convention of circuit variables is shown in Figure 3. This converter circuit includes a Diode Bridge Rectifier (DBR); an input inductor L1; a main switch Q; an intermediate capacitor C1; A voltage multiplier cell is added into the circuit, which includes CM, DM; a Tapped Inductor (TI) of Lp, Ls; and a charge pump is added into the circuit, which includes C2, D1 and Do, feeding an output filter capacitor, Co, and a load, RL. The TI's turn's ratio, n is given as,

$$n = N2/N1 \quad (1)$$

At this point, N1 and N2 are the primary and the secondary number of turns, correspondingly.

This converter is developed from the basic SEPIC topology [20] as in Figure 2. From the Figure 3, the inductor L1 is swapped with TI in order to accomplish higher voltage gain. Additional increase in voltage gain is achieved through the process of applying a voltage multiplier cell. As well, the incorporated "voltage multiplier cell" assists the proposed converter attaining Zero-Voltage (ZV) and Zero-Current (ZC) switching, which enhance the efficiency, and permit higher switching frequency and size reduction.

This converter topology possesses an extra advantage. In case if the switch,Q is turned on, the charge pump capacitor,C1 fastens the anode voltage of the output diode, Do, to ground. Therefore, the voltage stress of Do is free of the TI turns ratio and same as the output voltage. This lessens the switching losses of Do and is an additional benefit of this converter. In addition, this converter is designed to function in DCM in order to achieve almost a unity power factor and low Total Harmonic Distortion (THD) of the input current. The DCM operation provides additional benefits like simple control circuitry i.e. only one voltage sensor is needed to control this converter.

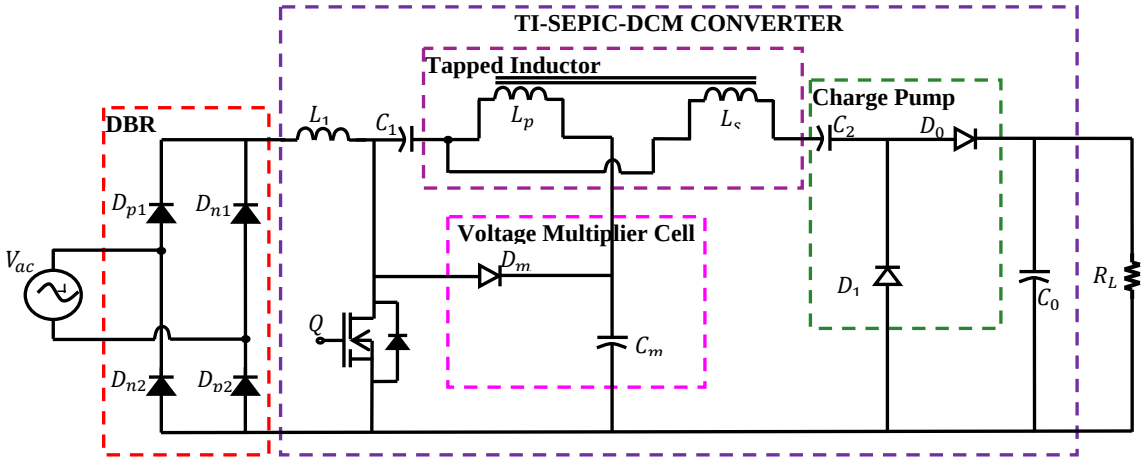


Figure 3. Schematic diagram of the proposed SEPIC converter with the TI model operating in Discontinuous Conduction Mode (TI-SEPIC- DCM)

3. PRINCIPLE OF OPERATION

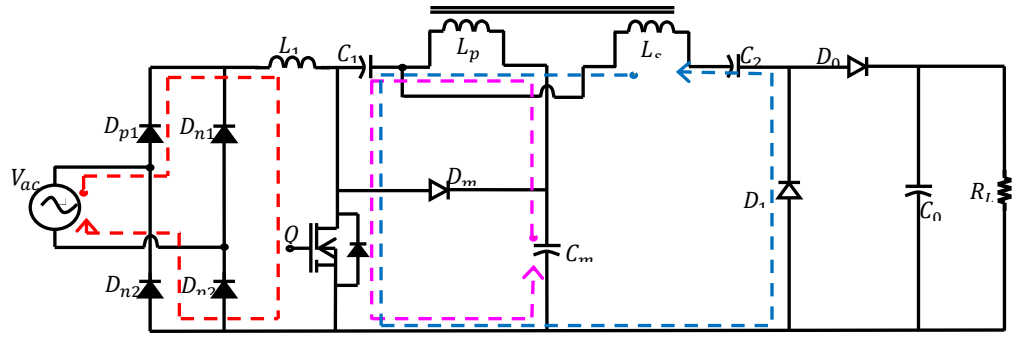
The proposed TI-SEPIC- DCM converter operating in DCM presents three operation stages. The theoretical analysis is initially developed considering the operation as a dc–dc converter at steady state and all circuit components are considered ideal. The voltages across all capacitors are considered constant during a switching period, as an ideal voltage source. The DCM operation occurs when there is the third operation stage, where the power switch is turned off and the currents in all diodes of the circuit are null. Therefore, the DCM operation occurs when D_o and D_M diodes are blocked before the switch turn-on.

This circuit presents two inductors; accordingly, different inductor values combination can be adopted for the DCM operation. In order to reduce the input current ripple of the preregulator, a relative high value for the inductor L_1 is considered. A relative low value of the Tapped Inductor (TI) is used for the converter operation in DCM as a voltage follower, where the input current follows the input voltage waveform. Accordingly, the preregulator input current follows the input voltage waveform with low current ripple, without input filter and without current-control loop.

In view of the fact that the proposed circuit is analysed for the complete switching period is shown in Figures. 4. Assuming that the three inductors are operating in DCM, then the circuit operation during one switching period Ts can be divided into three distinct operating modes, as shown in Figure. 4(a)–(c), and it can be described as follows.

Mode 0

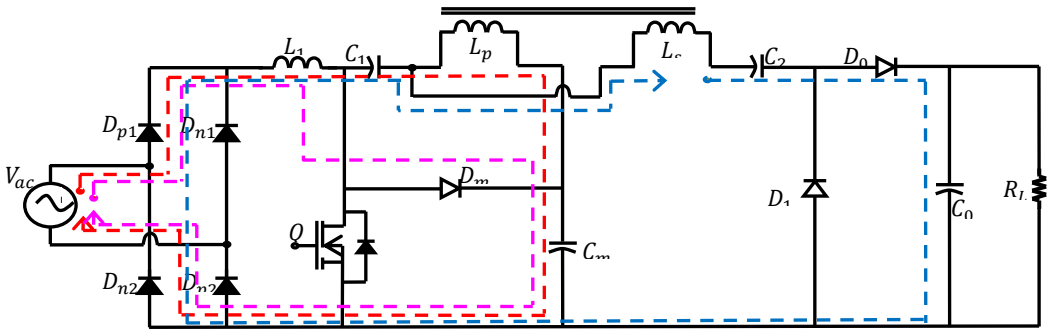
At some point in the conduction of power switch Q (i.e.)when switch Q is turned on by the control signal, and both diodes Dp1 and Dp2 are forward biased, Consequently, the input voltage, Vac, is applied across the inductor, L1 , and the input current, iL1, starts ramping up, whereas multiplier cell capacitor Cm starts discharging via switch Q, therefore the voltage applied across TI(Lp) is equal to the voltage of capacitor Cm minus the voltage of capacitor C1, and the diode DM is blocked during this operation stage. Furthermore, capacitor C2 starts charging from TI(Ls) via switch Q, during this operation stage diode D1is forward biased as shown in Figure 4(a).



Figures 4(a). The proposed TI-SEPIC- DCM converter operating in DCM presents at Mode 0 operation

Mode 1

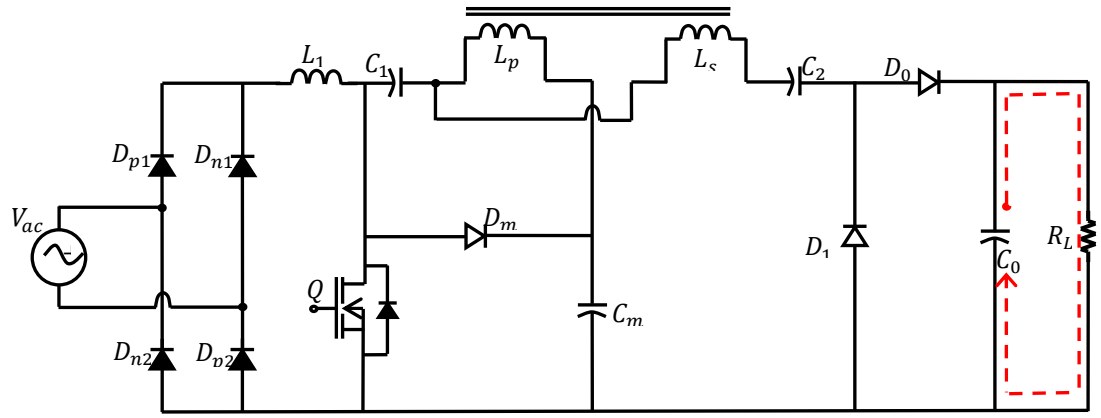
In case if the power switch Q is turned off, the supply current and the energy stored in the input inductor L1 is transferred to the multiplier cell capacitor CM via capacitor C1 and TI(Lp), and both diodes Dp1 and Dp2 are forward biased during this operation stage. There is also energy transference to CM capacitor through diode DM and the maximum switch voltage is equal to the CM capacitor voltage. Subsequently, the secondary side of tapped inductor TI (Ls) keeps discharging the secondary current, through diode D0 to the output capacitor C0. In this stage the capacitor C0 voltage increased steeply, because the energy stored in the TI(Ls), capacitor C2, energy in main supply(Vac), input inductor L1 and capacitor C1is transferred to the capacitor C0 (i.e. high gain is attained during this operating stage) as shown in Figure 4(b).



Figures 4(b). The proposed TI-SEPIC- DCM converter operating in DCM presents at Mode 1 operation

Mode 2

In case if the diodes D0 and DM are blocked, the voltage applied across the input inductor L1 and TI are null, maintaining the inductors currents constant as presented in (2) and (3). The currents through the input inductor L1 and TI present the same value, operating as a freewheeling stage as shown in Figure 4(c).



Figures 4(c). The proposed TI-SEPIC- DCM converter operating in DCM presents at Mode 2 operation

This operation stage is finished when the power switch is turned on, returning to the first operation stage

$$VL1 = VL2 = 0 \quad (2)$$

$$\Delta iL1 = \Delta iL2 = 0 \quad (3)$$

Control of proposed TI-SEPIC-DCM converter

In case if the proposed converter operating in DCM present a third-harmonic distortion in the input current. This current distortion is a function of the voltage difference between the input and output voltage. In general, the output voltage is increased to reduce the third-harmonic distortion to maintain high power factor, however the semiconductors losses are increased. With the aim of reducing the third-harmonic distortion without increasing the output voltage, an open-loop control action for the classical boost converter in [34].

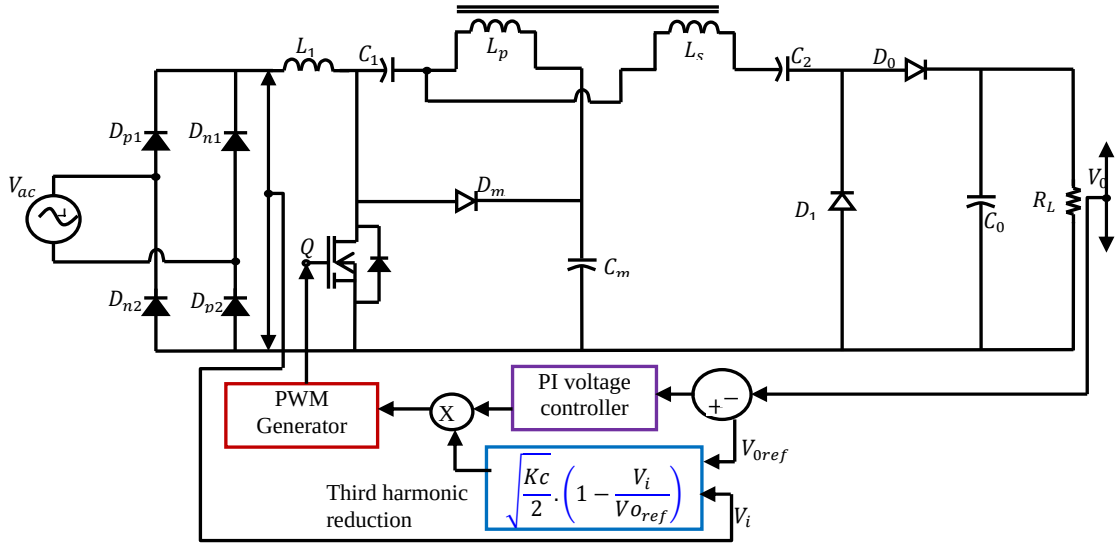


Figure 5. The block diagram of the proposed converter control loop

The same open-loop technique is developed in this TI-SEPIC-DCM converter for obtaining high power factor. The proposed preregulator operation in DCM allows obtaining near unity PF and low THD without a current-control loop and only a voltage control loop is necessary [34]. The output voltage control algorithm used in the proposed converter is based on the classical PI controller. The block diagram of the converter control loop is presented in Figure 5, including the third-harmonic reduction technique.

$$D(\omega t) = \sqrt{\frac{K_c}{2}} \cdot \sqrt{1 - \frac{V_{pk}.\sin(\omega t)}{V_0}} \quad (4)$$

Where, $K_c = \frac{8.P_0.L_{eq}.f}{V_{pk}^2}$

Only the output and input voltages are necessary to control the preregulator. The sensed output voltage signal (V0) is compared to an output voltage reference (V0 ref) and the error (Ev) is applied to a PI voltage controller. Simultaneously, the sensed rectified input voltage (Vi) and the output voltage reference are applied to (4) in order to calculate the duty-cycle variation for the third-harmonic reduction. The result of the PI output voltage controller and the result of the third-harmonic reduction are multiplied obtaining the preregulator duty cycle and generating the PWM signal that controls the main switch Q. The experimental setup of MATLAB/Simulink diagram of the proposed TI-SEPIC- DCM converter is shown in the figure 6.

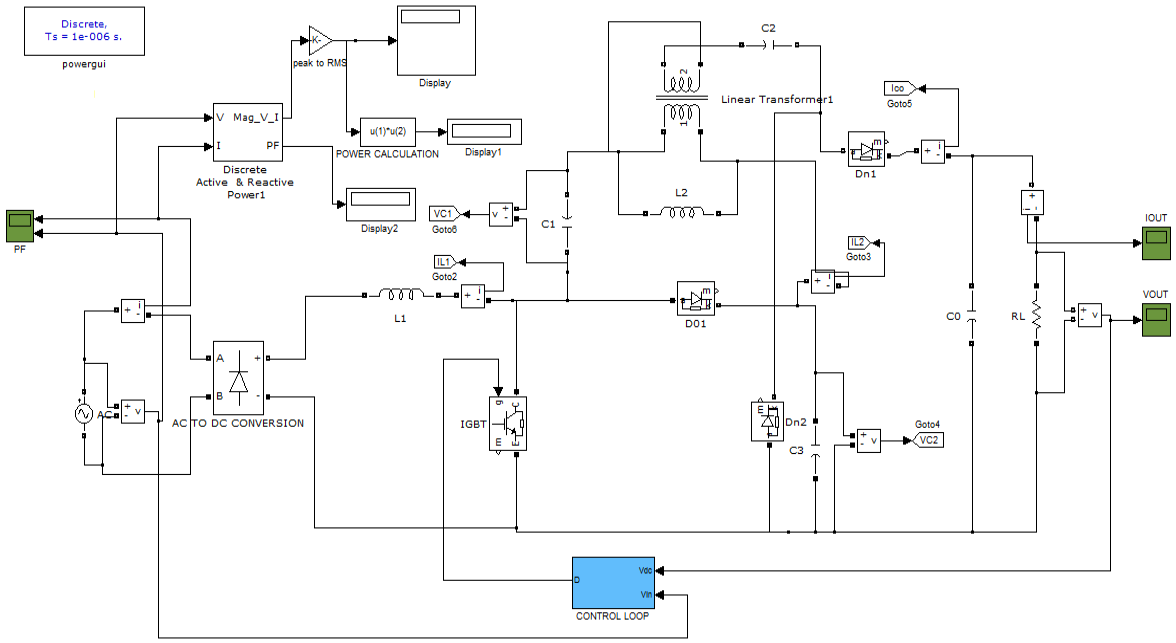


Figure 6. MATLAB/Simulink experimental setup of the proposed TI-SEPIC- DCM converter

4. RESULTS AND DISCUSSION

The performance of the proposed TI-SEPIC- DCM converter is simulated in a MATLAB / Simulink environment using the SimPower-System Toolbox. The proposed converter performance is evaluated for both rated and dynamic conditions and the achieved power quality indices obtained at ac mains. Parameters such as supply voltage (V_s), supply current (i_s), main switch current (i_Q), main switch voltage (V_Q), converter output voltage, output current and output power (V_{OUT}), (I_{OUT}) and (P_{OUT}) respectively, of the proposed converter are evaluated to demonstrate its proper functioning. Moreover, power quality indices such as power factor (PF) [36], Total Harmonic Distortion (THD) of supply current are analysed for finding power quality at ac mains. The converter specifications for simulations are given in Table 1.

Table 1. Specification

Parameters	Values
V_{S_peak}	8.484 V
V_{S_RMS}	6 V
I_{S_peak}	22.27 A
I_{S_RMS}	15.75 A
Input Power	94.54 Watts
Output Voltage	90 V
Output Current	1 A
Output Power	90 Watts
Efficiency	95.2%
Power Factor (PF)	0.9991

A. Steady-State Performance

Figure 7(a)-(e) shows the proposed converter operates at rated supply voltage of (8.48 V) and rated power on load (90W) respectively. As shown in these figures, the load voltage, load current and load power is maintained at the desired reference value as shown in Figures 7(c-e). Here parameters like $V*_L$, $I*_L$ and $P*_L$ desired reference voltage, current and power of load respectively.

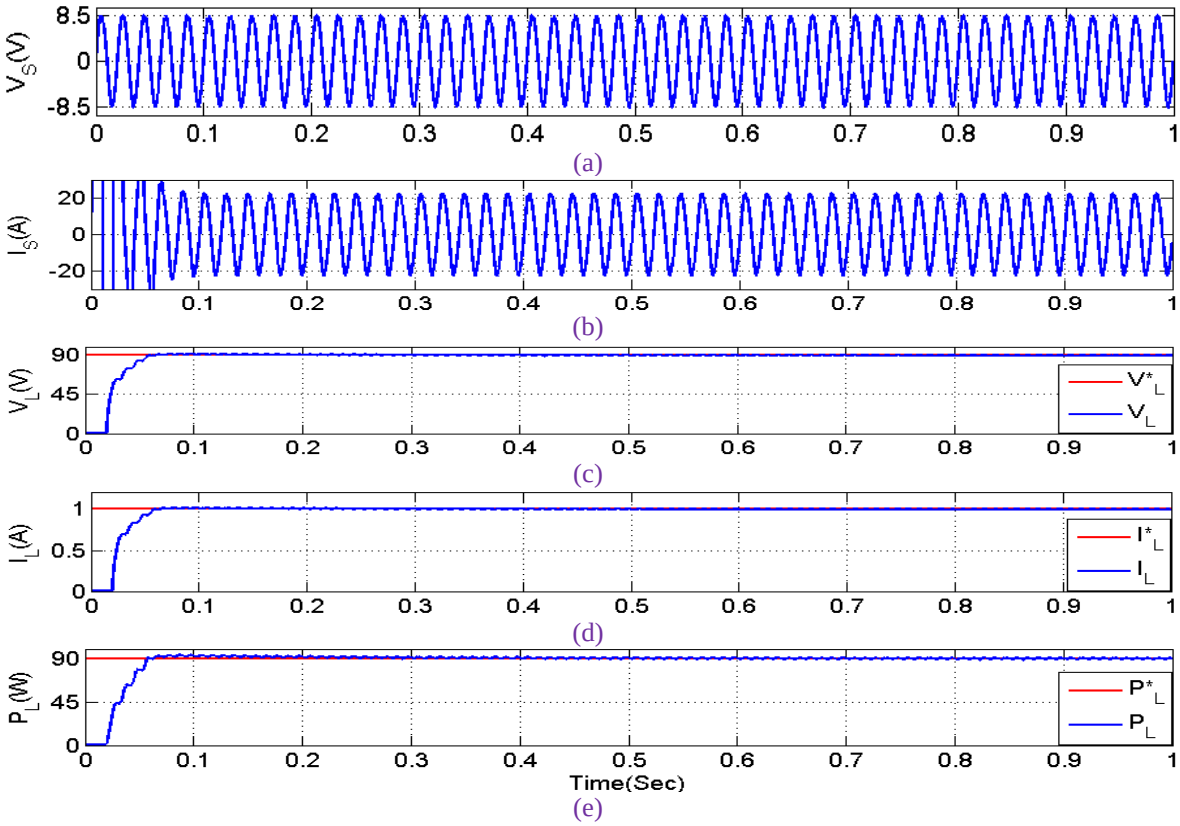


Figure 7(a)-(e). The proposed converter operates at rated supply voltage of (8.48 V)

B. Dynamic Performance

As given in this Figures 8 the proposed converter during closed loop control corresponding to the supply voltage is reduced from 6 V to 5 V at instant of 0.7 sec as shown in Figure 8(a). The rated load voltage of 90 V is maintained constant and the corresponding supply current variation is depicted in Figure 8(c) and (b). As shown in this Figure 8(c), the load voltage is maintained at the desired reference value with limited overshoot and undershoots. A smooth closed loop control is obtained, moreover Figure 8(d) and 8(e) shows the harmonic spectra of supply current at ac mains at rated load voltage (90V) with supply voltage as 6

V and 5 V, respectively. An acceptable THD of supply current is obtained for both the cases which show an improved power quality operation of the proposed TI-SEPIC- DCM converter at universal ac mains.

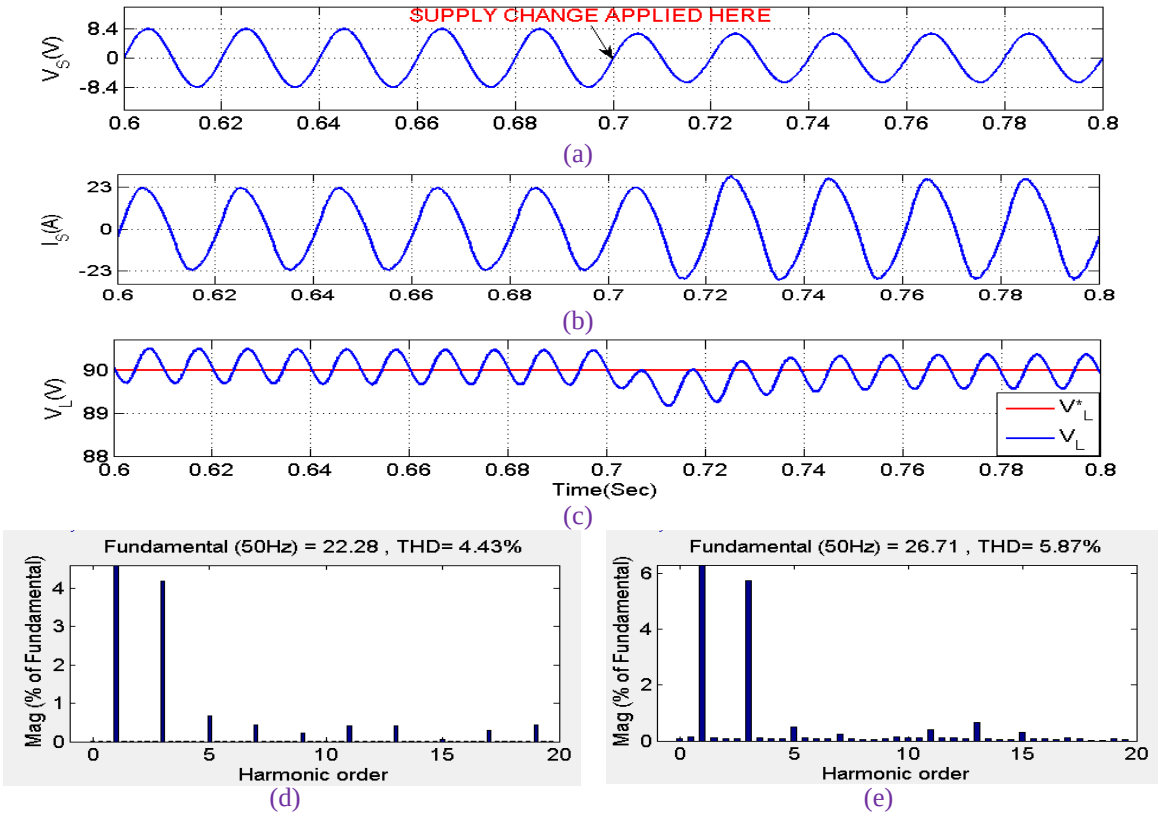


Figure 8(a -e). The dynamic performance of the proposed converter during a step change

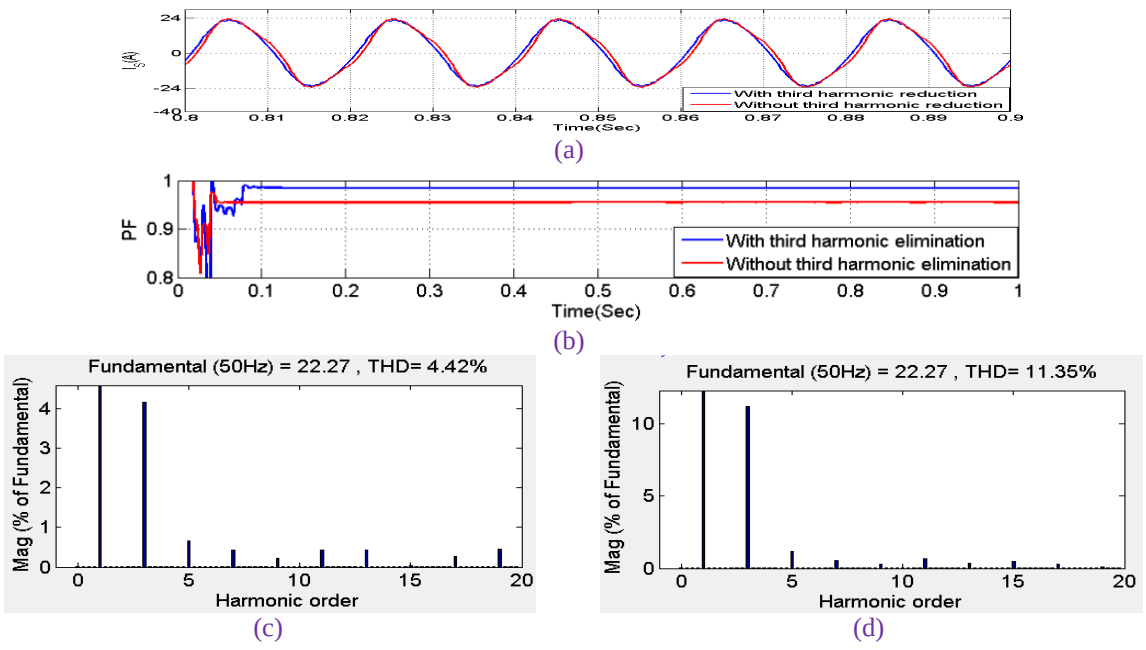


Figure 9. The proposed TI-SEPIC-DCM converter performance is compared with and without the implementation of the third-harmonic reduction technique

C. Performance Comparison of Third Order Reduction Control Loop

The proposed TI-SEPIC-DCM converter performance is compared with and without the implementation of the third-harmonic reduction technique is shown in Figures 9. When the proposed converter operating with rated supply voltage of $V_{S_{RMS}} = 6V$ and rated load power on 90W then the corresponding supply current of the proposed converter with and without implementation of third order reduction technique is shown in Figure 9(a). The total input current harmonic distortion is equal to 11.35% without the application of the third-harmonic reduction technique and the converter power factor is equal to 0.9552 is shown in Figure 9(d) and 9(b) respectively. The total input current harmonic distortion is reduced to 4.42% with the application of the third-harmonic reduction technique and the converter power factor is increased to 0.9841 is shown in Figure 9(c) and 9(b) respectively.

D. Soft Switching Operation of Proposed Converter

The Figure 10 shows the obtained voltage and current at the ac mains for the operation of the proposed converter at various values of output voltages. Moreover soft switching operation i.e. ZVS and ZCS is achieved for proper control of the converter is shown in Figure 10(a) and 10(b) respectively.

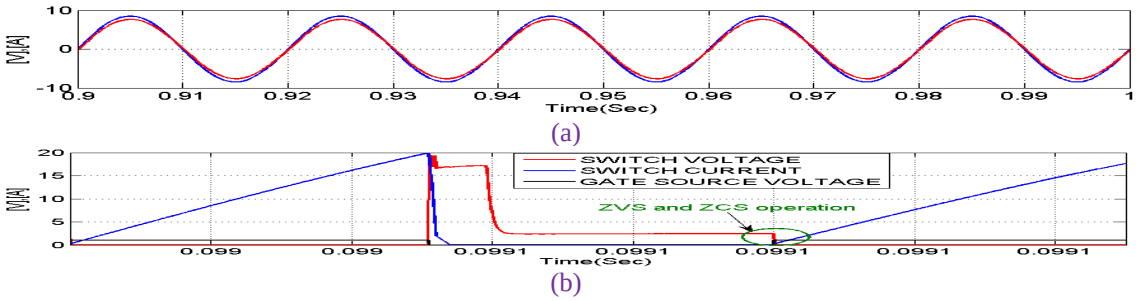


Figure 10. The soft-switching operation of proposed TI-SEPIC-DCM converter

5. CONCLUSION

This paper presented a novel PFC Converter with minimal THD. The proposed TI-SEPIC- DCM introduced the tapped inductor model to alleviate the switching voltage stress and to improve converter performance. ZVS and ZCS are attained in this work through voltage multiplier cell. The converter performance is improved by voltage gain and charge pump circuit with higher switching frequency. The THD results are obtained for third order harmonic reduction wherein the only 4.4% THD. Similarly, the significance of the converter performance is validated through ZVS and ZCS simulation results. Thus, the proposed converter results in near unity PF improvement through third order harmonic reduction.

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