International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 8, No. 1, March 2017, pp. 59~68
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v8i1.pp59-68

Design of Full-bridge DC-DC Converter 311/100 V 1kW with PSPWM Method to Get ZVS Condition

Toni Prasetya, F. Danang Wijaya, Eka Firmansyah
Department of Electrical Engineering and Information Technology, Faculty of Engineering, Universitas Gadjah Mada, Indonesia

Article Info

Article history:

Received Sep 23, 2016
Revised Nov 28, 2016
Accepted Dec 09, 2016

Keyword:

DC-DC converter
High frequency transformer
Leakage inductance
Paracitic capacitance
Zero voltage switching

ABSTRACT

Enhancing the switching frequency can increase the power density of a full-bridge dc-dc converter. However, power loss in switches will increase due to the intersection of voltage and current during turn-on and turn-off transition process. The switching power loss can be reduced by making the condition of zero voltage switching (ZVS) which in this study is obtained by using the phase-shifted PWM method. Achieving this condition requires appropriate parameters such as deadtime, leakage inductance, and the primary current of transformer in sufficient value. In this study, ZVS is achieved when the transformer leakage inductance of 14.12 μH is added with external inductance of 24.29 μH which is installed in series with transformer and when the primary current of transformer is more than 1.289 A.

Corresponding Author:

Eka Firmansyah,
Department of Electrical Engineering and Information Technology,
Faculty of Engineering, Universitas Gadjah Mada, Indonesia.
Email: eka.firmansyah@gmail.com

1. INTRODUCTION

DC power supply is increasingly being used for various applications such as battery charger (for rechargeable battery in electric vehicles, electronic equipments, energy storage systems in photo-voltaic and wind power plant), induction heating, welding machine, and other applications. DC power supply used and developed today is a switch mode power supply (SMPS). SMPS has been chosen to replace linear power supply because of its higher efficiency, smaller and lighter size [1]–[9].

The main part of dc power supply is a dc-dc converter which has various kinds of topology. One of them is full-bridge topology which can be applied to a higher power than the other topologies (≥ 500 W). This topology is development of a buck converter topology with four electronic switches and insulated transformer [10]–[14]. On the development, the converter technology is always strived to improve efficiency as high as possible and with size as small as possible. Some ways to achieve these conditions are developing from hard switching to soft switching method, applying high frequency and selecting component values accordingly [4],[8],[9],[15].

One of the frequently used soft switching method is phase-shifted PWM. The aim of that method is to get zero voltage switching (ZVS) condition, at the time of the switch turn-on, the switch will be active when the voltage value is zero. So that the power loss in the switching process can be minimized [2],[16],[17]. The parameters that must be satisfied in order to achieve the ZVS condition are leakage inductance in a sufficient value, deadtime as small as possible and current which is greater than the value required. Leakage inductance value is very dependent on the high-frequency transformer design. Deadtime value is determined by considering the value of rise time, fall time, and delay time of the gate-driver circuit and the MOSFET which are used. While the current depends on the load. Therefore, by making the design,

method and selection of components for correct and appropriate converter loading area, it is expected to significantly reduce the switching losses and losses in the converter as a whole [12],[13],[16],[17].

Many studies that discussed the method of making a transformer and also the equation to calculate the leakage inductances of each method used [1],[18],[19]. In practice, there are several chalanges to design a transformer with parameters as needed, in order to obtain the leakage inductance value as small as possible to achieve ZVS condition. Therefore, on this paper, it is discussed the design of dc-dc converter with the phase-shifted PWM method to obtain ZVS condition which mainly focuses on the transformer leakage inductance. Then, if the value of the leakage inductance is not sufficient, an external inductance will be added in series with the transformer to increase the size of the transformer leakage inductance. DC-DC converter that is made will be used to convert an input voltage of 311 Vdc to ± 100 Vdc output voltage with a maximum power of 1 kW.

2. RESEARCH METHOD

Figure 1 is a block diagram of the dc-dc converter that has been made. In general, the diagram is divided into four parts: power supply, power converter, control circuit and sensors. However, the focus of this research is on the power converter, phase-shifted PWM method, and the factors in that method to obtain zero voltage switching conditions. Parts of the power converter which will be discussed are inverter and high-frequency transformer because of their important role in ZVS condition.

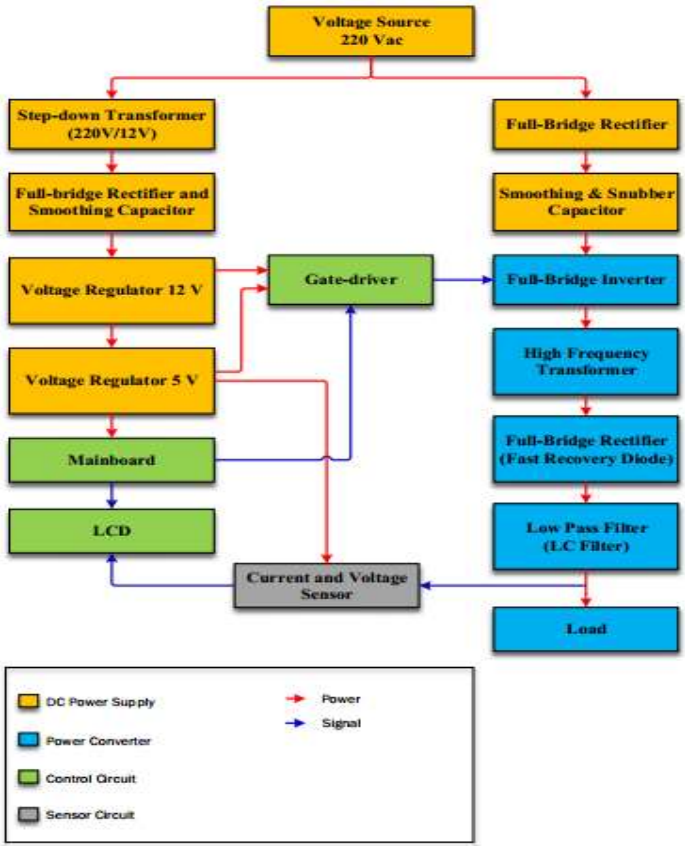


Figure 1. Block diagram of the dc-dc converter system as a whole

2.1. Power Converter

2.1.1. Full-bridge Inverter

Inverter is an electronic circuit that is used to convert dc voltage into ac voltage. An inverter with full-bridge topology is used because it can be applied for higher power compared to other topologies (≥ 500 W) [12],[13]. This topology requires four electronic switches, two pairs of top and bottom switch (S1-S2 and S3-S4) as in Figure 2.

Each switch used in the converter must has a higher voltage rating than the system voltage plus 10% of the system voltage. This 10% is a voltage spike that still can be tolerated in a system. Because system voltage is 311 V, the switch used must have a higher voltage rating than 341.1 V. The switch current rating should be higher than twice of the nominal current passing through the switch at full load conditions in order to avoid damage to the switch at the time of a spike current. The applied full-load current is 3.21 A, so the switch used must have a higher current rating than 6.42 A. From these parameters, MOSFET with IRF740 series are chosen. This MOSFET has a maximum voltage rating of 400 V and a maximum current of 8 A that is sufficient for the application of this converter.

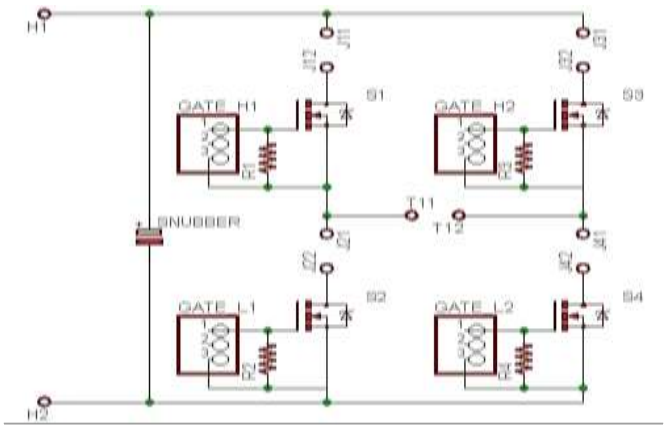


Figure 2. Schematic of full bridge inverter

In the dc-link side as shown in Figure 2, snubber capacitors are installed in parallel to reduce the voltage spike that occurs in the MOSFET to the permissible values. These capacitors should be an ac capacitor with a low ESR (equivalent series resistance) value and able to withstand higher voltage than in the system. Therefore, ceramic capacitor 820 pF with a voltage rating of 450 V in parallel is used. On each gate-source, resistors 4k7 Ω are installed in parallel (R1, R2, R3, R4) as a pull-down resistor. The function of each resistor is to ensure that the switch will be completely off when no signal coming into the gate.

2.1.2. High Frequency Transformer

High frequency transformer plays an important role in a dc-dc converter. It is used to step-down voltage and as an insulation between the input and output side of the converter. Moreover, it can determine in achieving ZVS condition in a phase-shifted PWM method [1],[19]. The selection of switching frequency will determine power density of transformer. However, a problem in increasing the switching frequency is the switching losses in the MOSFET on the inverter side will also increase. Those losses are due to the intersection between the voltage and current during turn-on and turn-off process. Therefore, appropriate switching frequency, switching method, and component design should be meticulously chosen in order to obtain more compact and lighter converter with higher power efficiency. In the design, the operating frequency used is 25 kHz. Ferrite core used is MnZn because of its large resistivity. Thus, at high frequency, the eddy current loss can be ignored due to its very small ratio to hysteresis loss [4],[12],[13],[16],[18]–[20].

Figure 3. High frequency transformer

2.2. Phase-shifted PWM method

In conventional method, the duty cycle output of inverter is represented by the duty cycle of the microcontroller output PWM, while in the phase-shifted PWM method, the PWM duty cycle is maintained at a value of 50%. Then the duty cycle output of the inverter is set by shifting the phase between the diagonal switches pair as seen in Figure 4 [16],[19]. The magnitude of the phase-shifted PWM is shown at the time t_1 to t_2 and t_3 to t_4.

An important part in the phase-shifted PWM method is determining the value of deadtime which in Figure 4 is shown in the period t_0 to t_1 and t_2 to t_3. The deadtime value should be set as small as possible so that the leakage inductance value is smaller and ZVS can be reached at wider area. But the deadtime value also should be large enough to avoid short circuits that may occur due to the turn-on and turn-off process in MOSFET. With consideration of rise time, fall time, and delay time value of the gate-driver circuit and the MOSFET that is used, then the deadtime value selected is 250 ns.

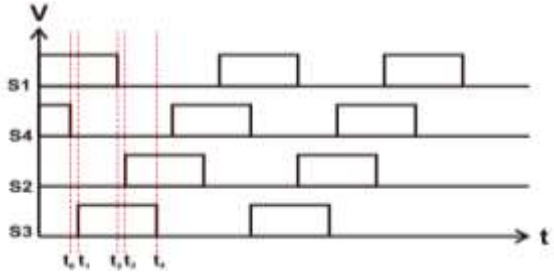


Figure 4. Phase-shifted PWM method scheme

2.3. Parameters limitation in phase-shifted PWM method to get the ZVS condition

2.3.1. Determining of the maximum deadtime

The process of charging and discharging energy of parasitic capacitance of the MOSFET occurred in the dead time. The energy transfers from the parasitic capacitance to the leakage inductance and also from the leakage inductance to parasitic capacitance of the MOSFET in other side is happened when the top and the bottom switch pair are off together [12],[13],[16]. The value of the maximum deadtime can be determined by using equation (1). Deadtime value was affected by the resonant frequency (W_r) expressed in equation (2) [13],[16],[21].

The maximum value of deadtime:

$$t_{deadtime\ (max)} = \frac{\pi}{2\ x\ W_r} \quad (1)$$

The resonan frequency:

$$W_r = \frac{1}{\sqrt{(L_r\ x\ C_r)}} \quad (2)$$

2.3.2. Determining the minimum value of leakage inductance

Leakage inductance that is used must be able to store energy from discharging of two MOSFET parasitic capacitance (C_{oss}) coupled in parallel with the capacitance transformer (C_{xfmr}). In practice, the value of each C_{oss} need to be exceeded by a factor of 4/3 to accommodate the increase in capacitance due to high voltage operation [13],[16],[21]. The total value of C_r is shown in equation (3). While the amount of energy required in a capacitor when the transition process is determined by the equation (4).

The total of resonance capacitance:

$$C_r = [(\tfrac{8}{3} x Coss) + C_{xfmr}] \quad (3)$$

The capacitive energy required when the transition process:

$$W(C_r) = \tfrac{1}{2}\ x\ C_r\ x\ (V_{primer})^2 \quad (4)$$

By using the equation of capacitans and inductans energy equivalence, the leakage inductance value (resonant inductance) can be determined by the equation (5) and (6).

Leakage inductance required:

$$L_r = \frac{1}{w_r{}^2 x\, C_r} \quad (5)$$

$$Lr = \frac{1}{\left[\frac{\pi}{2\,x\,(t_{\text{deadtime (max)}}}\right]^2 x\,[C_r]} \quad (6)$$

2.3.3. The minimum value of the transformer primary current

The amount of energy stored in the inductor is very dependent on the amount of current flows. In order to achieve ZVS condition, the energy stored in the inductor must be greater than or equal to the amount of energy stored in two MOSFET parasitic capacitances related [13],[16],[21]. The equation for calculating the minimum current value can be determined by the following equation.

The minimum value of current required:

$$I_p(\text{min}) = \sqrt{\left[\frac{C_r\, x\, V_{in}{}^2}{L_r}\right]} \quad (7)$$

2.4. Hardware setup

Hardware setup and description of each part of the full-bridge dc-dc converter that has been made is shown in Figure 5.

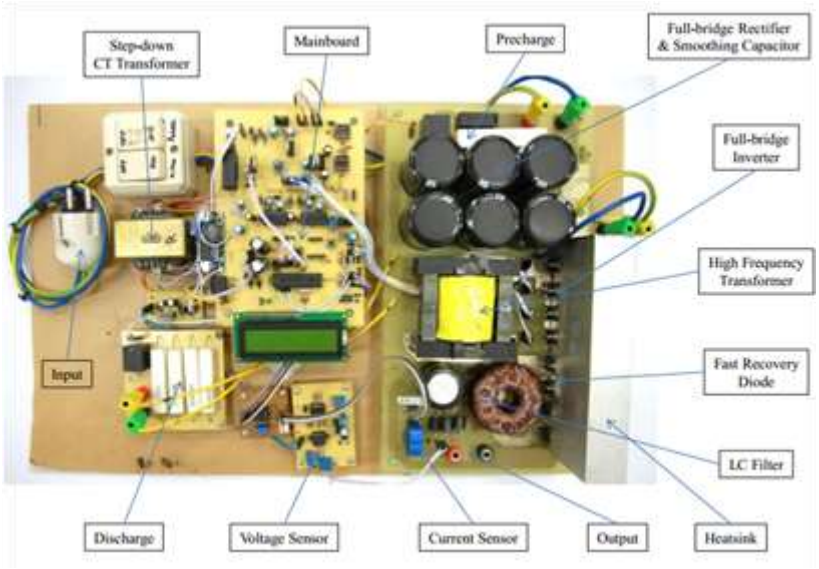


Figure 5. Hardware setup of full-bridge dc-dc converter

3. RESULTS AND ANALYSIS

3.1. Phase-shifted PWM

Microcontroller output PWM is designed in complementary mode. This means that between pairs of high and low PWM should be opposite each other and have different phases of 180^0. Thus, PWM1L contrary to PWM1H and PWM2H contrary to PWM2L. In a phase-shifted PWM method, the PWM duty cycle from the microcontroller is maintained at a value of 50%. While the duty cycle value of the inverter output is regulated by shifting the phase of the right side PWM pair (PWM2H and PWM2L) against the left side PWM pair (PWM1H and PWM1L) in accordance with the desired value. The microcontroller output PWM waveforms with the phase-shift of 70% are shown in Figure 6. In that figure, it appears that each pair of PWM reverses each other and the phases are shifted at 70% between the right side PWM pair to the left side PMW pair.

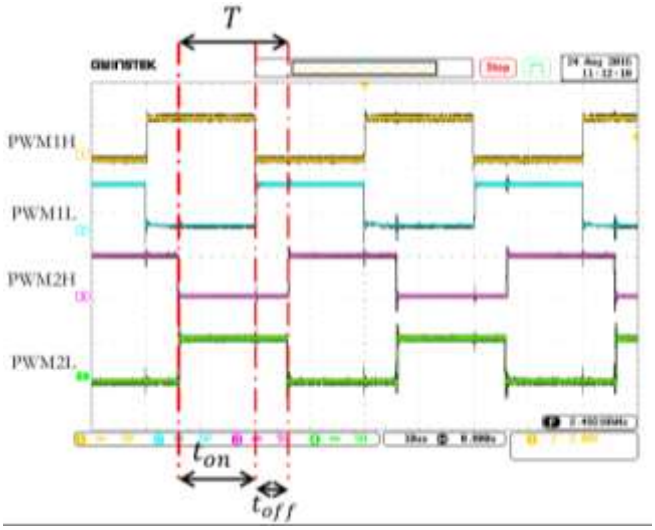


Figure 6. Output PWM from the microcontroller with phase-shifted 70%

3.2. Determining the value of deadtime

Deadtime intended to prevent a short circuit between the top and bottom switch pair at rise time and fall time. Therefore, there must be deadtime for each pair of PWM high and low as shown in Figure 7. Deadtime value should be as small as possible due to give a wider range of ZVS condition, but should still make sure to avoid short circuit. The deadtime is chosen at 250 ns as shown in Figure 7.

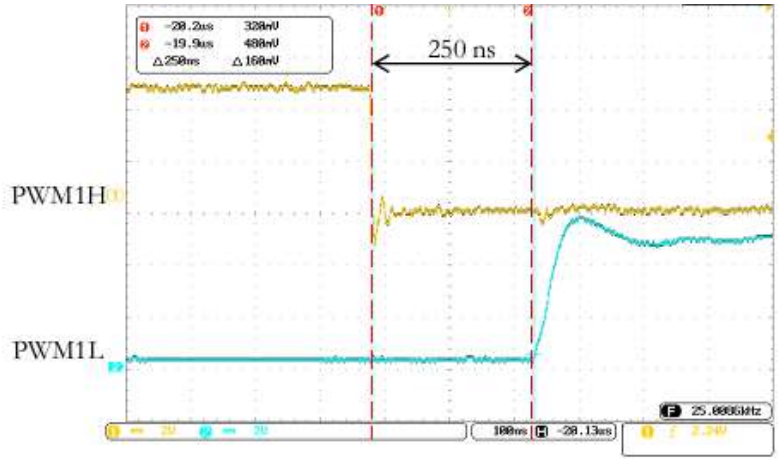


Figure 7. Pair of high and low PWM waveform with the deadtime of 250 ns

3.3. Calculation result

Transformer parameters are measured by using an LCR meter. The measurement results are shown in Table 1. One of the observed parameters is transformer leakage inductance which is 14.12 µH. In fact, regarding equation (5) and (6), with the value of the parasitic capacitance of 220 pF (see Table 2) and deadtime value of 250 ns (see Figure 7), the minimum leakage inductance value required is ± 38.41 µH. Therefore, an additional external inductance with the minimum value of 24.29 µH is required. By using the equation (7), to get the ZVS condition, then the minimum current of primary transformer required is about 1.289 A. This means that the ZVS condition can be occurred when the load power is greater than 280 watts for a duty cycle of 70% and a minimum of 360 watts when the duty cycle of 90%.

Table 1. Parameters of high frequency transformer

Parameters	Value
Transformation ratio	311:140
L_m	55.23 mH
$L_{leakage}$	14.12 µH
R_p	1.117 Ω
L_s	2.95 µH
R_s	0.2416 Ω

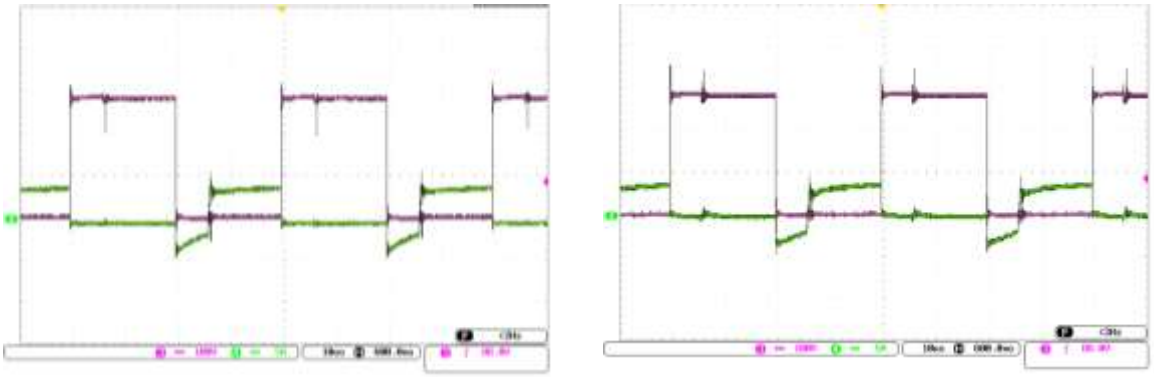
Table 2. Parameters of MOSFET with a series of IRF740

Parameters	Value
C_{oss}	220 pF
R_{ds}(on)	0.55 Ω
Turn-on delay t_d (on)	14 ns
Rise time (t_r)	27 ns
Turn-off delay td (off)	50 ns
Fall-time (t_f)	24 s

3.4. V_{ds} and I_d waveform

3.4.1. Without additional of external inductance

Observations of drain-source voltage (V_{ds}) and the drain current (I_d) of each MOSFET are carried out simultaneously. The aim is to see the characteristics of voltage and current in the MOSFET when phase-shifted method is used. It is also to see whether the conditions ZVS has occurred or not on each MOSFET. Figure 8 (a) and Figure (b) are the current and voltage waveform on the MOSFET pair top and bottom on the left side. The pair of the left side switch is a pair of switch which the phase is kept in fixed conditions. It can be seen that there is no intersection between voltage and current in the process of turn-on. It means the ZVS condition occured in these switches. The switches will active again when the gate voltage in the diagonal pair also active. So there is a delay time in accordance with the sum of the phase angle and the predetermined deadtime. Thus, the switching power loss on the left side switch can be reduced.

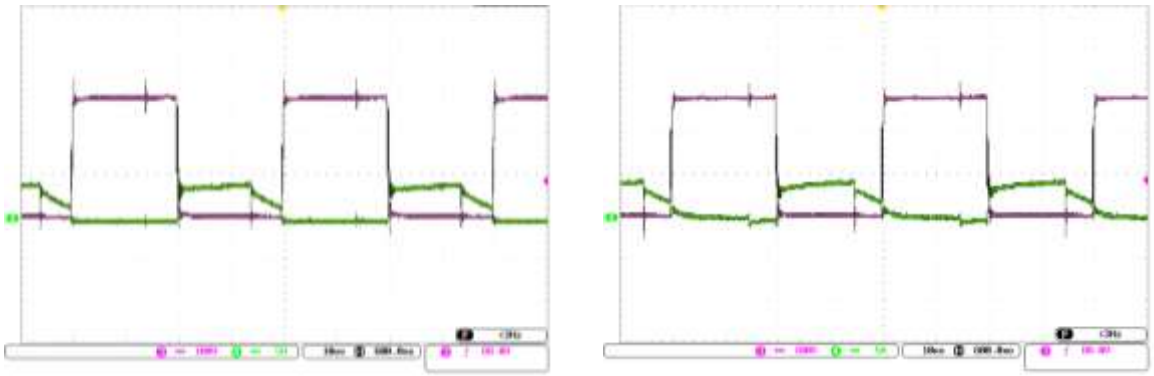


(a) (b)

Figure 8. (a) V_{ds1}(purple) vs I_{d1}(green) and (b) V_{ds2} (purple) vs I_{d2} (green) at duty cycle of 70% with the load of 700 W

Figure 9 (a) dan Figure (b) are current and voltage waveform on the right side switch. The pair of the right side switch are controlled by shifting the phase to determine the duty cycle of the inverter output. It is obtained that the switch will be activated immediately after the gate voltage is actived. Therefore, ZVS condition will only be achieved when the factors that influence the ZVS has been reached. These factors include the current and the transformer leakage inductance in a sufficient value.

It can be seen that there are intersection between current and voltage at the transition time of the MOSFET. It means that ZVS has not occurred on the both switches. To fix this problem, an external inductance which is installed in series with the transformer can be added to increase the transformer leakage inductance with a value of 24.29 µH as described previously.



(a) (b)

Figure 9. (a) V_{ds3}(purple) vs I_{d3}(green) and (b) V_{ds4} (purple) vs I_{d4} (green) at duty cycle of 70% with the load of 700 W

3.4.2. With additional of external inductance

By using a transformer without the addition of external inductance, ZVS condition on the right side switch will not be achieved. A simulation is conducted to show the differences in results of addition of an external inductance of 24.29 µH and a considerable load for making the primary current transformer more than 1.289 A as in the previous calculation. In the process, all parameters are set to approach the parameters on hardware especially MOSFET, control signals, deadtime, high-frequency transformers, LC filter components and the load. From the simulation results as shown in Figure 10, it shown that the current and voltage waveforms on the left side MOSFET pairs (S1 and S2) remain the same as before. While on the right side of the switch pair (S3 and S4), ZVS occurs due to the addition of the external inductance. Thus, the power loss due to the switching process can be reduced.

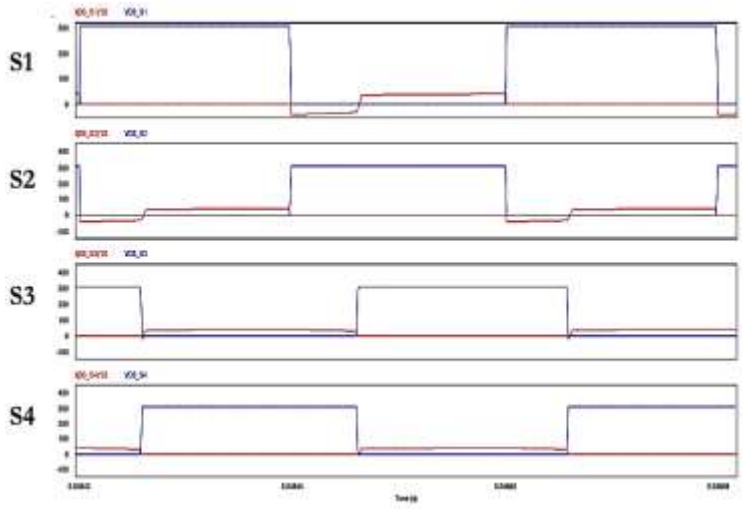


Figure 10. Simulation results of voltage and current waveforms in each MOSFET with additional external inductance of 24.29 µH

3.5. Converter efficiency

Converter efficiency is shown in the In Figure 11. The duty cycle is set 70%, 80% and 90%. It can be seen that the converter efficiency tends to decrease with increasing of the amount of load, because the power losses on each conversion process will increase along with increasing of the current flows. From the figure, it can be concluded that the converter efficiency over 90% for a duty cycle of 70% to 90% with the load of up to 900 watt. The highest converter efficiency is 96.74% that occur when the duty cycle of 90%.

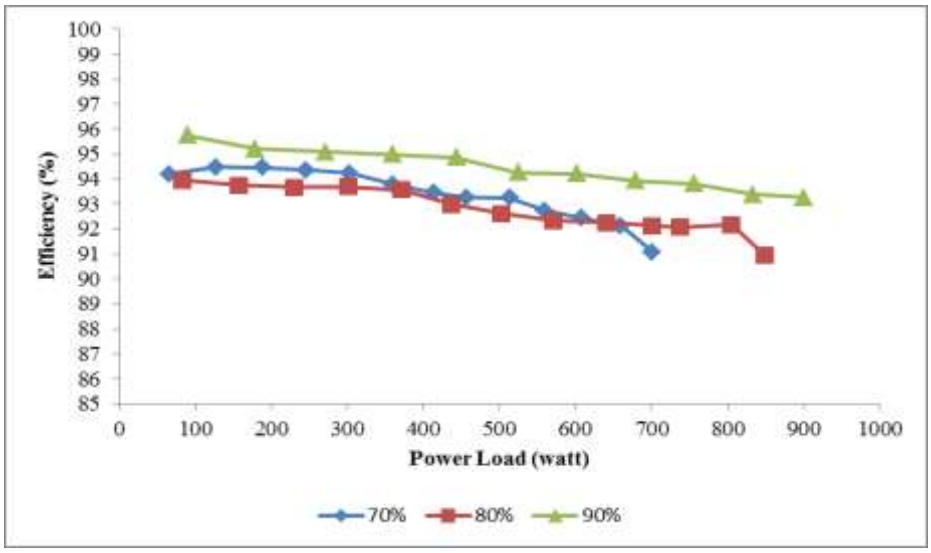


Figure 11. Efficiency of converter with various load and duty cycle value

4. CONCLUSION

Phase-shifted method can be used to reduce power loss in the switching process that is indicated by achieving ZVS condition. To obtain this condition, the terms of the ZVS such minimum leakage inductance, deadtime value, and transformer primary current must be satisfied. In this study, ZVS on the right side of the switch pair has not occurred due to the insufficient transformer leakage inductance. To fix this problem, an external inductance that is installed in series with the transformer can be added with a value of 24.29 μH and the minimum of transformer primary current of 1.289 A.

REFERENCES

[1] J. M. Choi, *et al.*, "Design of Leakage Inductance in Resonant DC-DC Converter for Electric Vehicle Charger," *IEEE Trans. Magn.*, vol/issue: 48(11), pp. 4417–4420, 2012.
[2] D. Gautam, *et al.*, "A Zero Voltage Switching Full-Bridge DC-DC Converter for An On-Board PHEV Battery Charger," pp. 0–5, 2012.
[3] U. Badstuebner, *et al.*, "Design of an 99% Efficient, 5kW,Phase-shifted PWM DC-DC Converter for Telecom Applications," 2008.
[4] I. Febriyandi, *et al.*, "DC-DC Converter as Powerof Battery Charger 100 V 300 W using 25 kHz Switching Frequency," no. November, pp. 302–307, 2014.
[5] M. S. K. Reddy, "Analysis Design and Implementation of VSI fed High Gain Full Bridge Isolated DC-DC Converter for Renewable Energy Applications," pp. 45–50, 2013.
[6] M. Ortega, *et al.*, "Novel Topology for DC-DC Full-Bridge Unidirectional Converter for Renewable Energies," vol/issue: 12(8), pp. 1381–1388, 2014.
[7] O. Lucía, *et al.*, "Induction Heating Technology and Its Applications : Past Developments, Current Technology, and Future Challenges," vol/issue: 61(5), pp. 2509–2520, 2014.
[8] T. M. Aiswarya and M. Prabhakar, "An Efficient High Gain DC-DC Converter for Automotive Applications," vol/issue: 6(2), pp. 242–252, 2015.
[9] S. Ray, *et al.*, "ZVZCS Based High Frequency Link Grid Connected SVM Applied Three Phase Three Level Diode Clamped Inverter for Photovoltaic Applications Part-II," vol/issue: 5(1), pp. 24–31, 2014.
[10] N. Mohan, "Mohan - Power Electronics.pdf," 1995.
[11] M. H. Rasyid, "Power Electronics Academic Press Series in Engineering," 2001.
[12] M. Kamil, "Switch Mode Power Supply (SMPS) Topologies," no. Part I, pp. 1–48, 2007.
[13] A. Bersani, "Switch Mode Power Supply (SMPS) Topologies (Part II)," no. Part II, pp. 1–108, 2009.
[14] E. Pepa, "Adaptive Control of a Step-Up Full-Bridge DC-DC Converter for Variable Low Input Voltage Applications Adaptive Control of a Step-Up Full-Bridge DC-DC Converter for Variable Low Input Voltage Applications," 2004.
[15] J. S. Prasad, *et al.*, "Regeneration of ZVS converter with Resonant Inductor," vol/issue: 1(1), pp. 21–28, 2011.
[16] B. Andreycak, "Application Note Phase-Shifted , Zero Voltage Transtion Design Consideration and the UC3875 PWM Controller," pp. 1–15, 1997.
[17] D. M. Joo, *et al.*, "Dead-time optimisation for a phase-shifted dc-dc full bridge converter with GaN HEMT," vol/issue: 52(9), pp. 769–770, 2016.
[18] D. Fu, *et al.*, "*Investigation on transformer design of high frequency high efficiency dc-dc converters,"* Appl.

Power Electron. Conf. Expo. APEC 2010 TwentyFifth Annu. IEEE, pp. 940–947, 2010.
[19] Z. Ouyang, *et al.*, "Calculation of Leakage Inductance for High-Frequency Transformers," *IEEE Trans. Power Electron.*, vol/issue: 30(10), pp. 5769–5775, 2015.
[20] C. W. M. T. Mclyman, "Transformer and Inductor Design Handbook," 2004.
[21] Toni, *et al.*, "Comparison of Two High Frequency Transformer Designs to Achieve Zero Voltage Switching in a Converter," pp. 1–5.