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Performance of Interconnection and Damping Assignment Passivity-Based Controller on Inverter Circuits

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ABSTRACT

This paper presents an extension work on the application of interconnection and damping assignment passivity-based controller (IDA-PBC) from the conventional H-bridge inverter to a 5-level Cascaded H-bridge Multilevel Inverter (CHMI). With the controller, the inductor current and the voltage capacitor track the desired reference of the inverter to ensure that the output voltage maintains its regulation while the Total Harmonic Distortion (THD) is kept at low levels with fast transient response. It is designed based on the Port-Control Hamiltonian theory exploiting the dissipation properties of the averaged model of inverter circuits. The results obtained have proven that the IDA-PBC previously developed for the H-bridge inverter can be easily extended and applied to the CHMI circuit. The simulation results showed that the IDA-PBC is able to maintain the output voltage regulation in both circuits in the case of no-load to full-load condition, load uncertainty, and structural uncertainty while maintaining THD of less than 5%. However, in all cases, CHMI has shown better performance in terms of THD percentage and transient response compared to the H-bridge inverter, which are 290 μs and 150 μs respectively.

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1. INTRODUCTION

Inverters are the simplest technology to convert DC to AC power and have been integrated in many applications, including uninterruptible power supplies (UPS), induction heating, high-voltage direct current (HVDC) transmission, electric vehicles, and various renewable energy applications [1],[2]. Inverters have gone through many technological improvements which include their capabilities in handling high power systems and reduction in switching losses. One of the improvement methods is by increasing the output voltage levels of the inverters that in turn reduce the Total Harmonic Distortion (THD) while also reducing the voltage stress on each component [3],[4]. The multilevel inverter topology, which was first introduced in 1975 [5], became popular over the years due to the fact that it was able to provide less disturbances and offered the possibility to function at lower switching frequencies compared to the ordinary three-level H-bridge inverters [6]. Various types of controllers such as hysteresis [7], sliding mode [8] and fuzzy logic [9] have been proposed for multilevel inverters over the years, mainly to maintain output voltage regulation and good dynamic performance. In recent years, there is an emerging interest on the development of a controller based on the concept of passivity that exploits the total energy of the system [10],[11]. There are two types of the so-called passivity-based controller (PBC) i.e the classical PBC and the interconnection and damping assignment PBC (IDA-PBC). The work presented in [12] shows that the performance of the IDA-

PBC on a single-phase H-bridge inverter is better than that of the classical PBC. The former has managed to maintain the inverter output voltage regulation with fast time response and low THD under load and parameters uncertainties. This paper extends the work presented in [12] for a 5-level Cascaded H-bridge Multilevel Inverter (CHMI). The performance of both the conventional H-bridge inverter and CHMI under IDA-PBC control are compared and analyzed.

2. INTERCONNECTION AND DAMPING ASSIGNMENT PASSIVITY-BASED CONTROLLER (IDA-PBC)

The IDA-PBC, introduced by Ortega et al. [13], is a physically-inspired control design methodology that invokes the principles of energy-shaping and dissipation and formulated for systems described by the Port-Controlled Hamiltonian (PCH) models. The main objective of this method is to stabilize the dynamical system by rendering the closed-loop system passive (by shaping its energy) with a desired storage function (which is a proper Lyapunov function) [11]. Apart from that, the system can be asymptotically stabilized if it can be rendered strictly (output) passive by means of damping injection [14]. This type of controller has been applied in many power electronic devices and shows remarkable results in controlling the respective system [12],[15]–[21].

In this paper, the IDA-PBC algorithm previously developed for a single-phase H-bridge inverter in [12] is used as a basis to develop the control algorithm of similar concept for a 5-level CHMI. The CHMI with five output voltage levels has been selected in this work because it owns the trade-offs of the advantages and disadvantages between the traditional H-bridge inverter and a higher output voltage level CHMI, i.e. seven, nine, eleven etc. In comparison to the H-bridge inverter, a 5-level CHMI can generate a higher output voltage magnitude by dividing the voltage between two H-bridges which results in reduced voltage stress in the circuit components. This results in a lower power losses and reduced harmonic contents in the output voltage. While higher output voltage levels of a CHMI may offer lower output voltage THD without the need for a filter circuit, the 5-level CHMI can produce a similar low output voltage THD with an added filter circuit, but at a lower cost, as it uses less number of components and switches [22].

The block diagram of an inverter with its controller is shown in Figure 1. It shows that the inverter output voltage is controlled using IDA-PBC. This is possible by feeding back the inductor current, i_L and the capacitor voltage, v_C from the low-pass LC filter into the controller. The IDA-PBC uses a d-q transformation technique and produces a sinusoidal reference signal, u. This signal is compared with a carrier signal and produces the PWM signals to accordingly turn on and turn off the inverter IGBTs as the switching devices. Detailed derivation of the controller algorithm is explained in the next section.

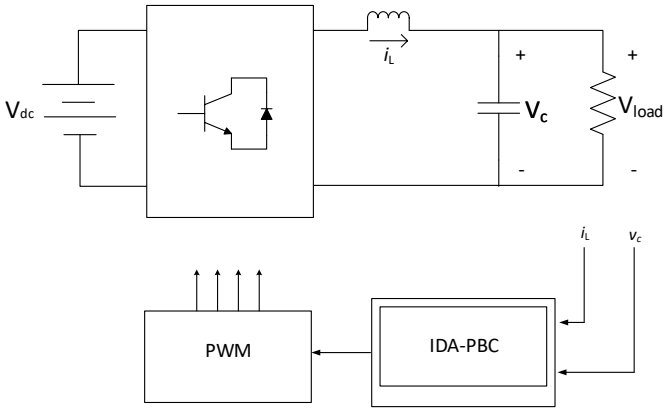


Figure 1. Inverter controlled by the IDA-PBC

3. AVERAGE MODELING OF THE 5-LEVEL CHMI

Figure 2 shows a 5-level CHMI circuit with a resistive load that is connected to an LC filter. Each H-bridge is connected to a separate DC voltage source that is used to generate the AC output voltage waveform. In general, the power circuit produces a 5-level output voltage waveform, including zero voltage as shown in Figure 3. The mathematical model of the CHMI is developed through an average modeling method as explained in [23], where each DC source is represented by a reduced cell denoted as $sw_1 \cdot V_{dc}$

and $sw_2 \cdot V_{dc}$ respectively. The simplified average circuit of the 5-level CHMI is shown in Figure 4. Each of the new, reduced cells can produce a 3-level output voltage waveform consisting of $+V_{dc}$, $-V_{dc}$, and 0. These voltages can also be represented by the sw_i switching function as +1, -1, and 0. The combination of both reduced cells can synthesize a 5-level output voltage waveform, represented by the sw_i switching function as -2, -1, 0, +1, and +2.

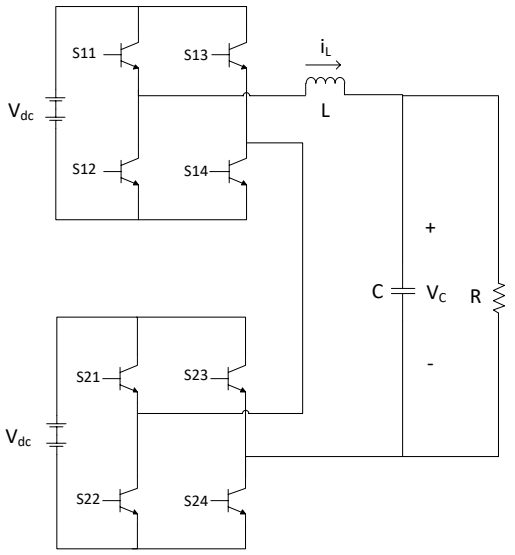


Figure 2. 5-level CHMI with LC filter

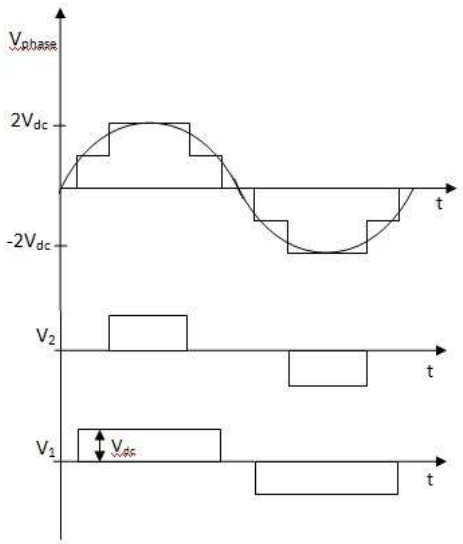


Figure 3. 5-level CHMI output voltage waveform

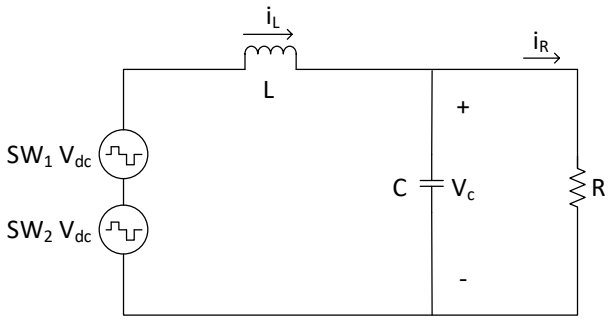


Figure 4. Simplified equivalent average circuit of the 5-level CHMI

By applying Kirchoff's Law, the mathematical model obtained for Figure 4 are as follows:

$$L\frac{di_L}{dt} = sw_1 \cdot V_{dc} + sw_2 \cdot V_{dc} - V_C \quad (1)$$

$$C\frac{dv_c}{dt} = -\frac{1}{R}v_C + i_L \quad (2)$$

Equations (1) and (2) showed that the system is operating in discontinuous mode. Considering that each DC bus feeds the same voltage to each cell, and that each control signal, u is assigned to each cell and is denoted as $u_1$and u_2, with $u = \{0, 1\}$, the equation (1) can be represented as:

$$L\frac{di_L}{dt} = \bar{u} \cdot V_{dc} - v_C \quad (3)$$

In this rearranged equation (3), the control signal is represented by $\bar{u}$, where the discrete set $\bar{u} = \{-2, -1, 0, +1, +2\}$ represents *u*, which defines the 5-level output voltage of the CHMI. This averaging derivation technique for the CHMI has been proposed and discussed in [23],[24].

4. THE PROPOSED CONTROLLER

Through the averaging technique, the control signal for a 5-level CHMI is extended to the discrete set of $\bar{u} = \{-2, -1, 0, +1, +2\}$. This averaging method can also be extended to a higher output voltage level multilevel inverter; given that the equation (2) and (3) are represented as:

$$L\frac{x_1}{dt} = -x_2 + \bar{u}V_{dc} \tag{4}$$

$$C\frac{x_2}{dt} = x_1 - \frac{1}{R}x_2 \tag{5}$$

where x_1 and x_2 are the average states corresponding to i_L and v_C respectively, while $\bar{u}$ is a continuous signal that belongs to the continuous set (-2, 2) or more. For the multilevel inverter model, equations (4) and (5) are constrained by the control law $\bar{u} = \bar{u}(x_1, x_2)$ such that:

$$\lim_{x\to\infty} x_1 - x_{1d} = 0 \;;\quad \lim_{x\to\infty} x_2 - x_{2d} = 0 \tag{6}$$

forcing internal stability and with prescribed behaviors for the average state of the system [25].

4.1. Port-Controlled Hamiltonian (PCH) System Details

In order to derive the IDA-PBC control algorithm, the Port Controlled Hamiltonian (PCH) description of the system is considered [25]:

$$\Sigma: \begin{cases} \dot{x} = [J(x) - R(x)]\frac{\partial H}{\partial x}(x) + g(x)u, \\ y = g^T(x)\frac{\partial H}{\partial x}(x), \end{cases} \tag{7}$$

where $J(x)$ and $R(x)$ are the interconnection structure and damping assignment respectively; $x \in R^n$ is the state variables vector; $u \in R^n$ is the input vector, and $y \in R^n$is the output vector. u and y are the power variables, which in this case, are the inductor currents, i_L and capacitor voltages, v_C. $H(x)$ is the energy (Hamiltonian) function. The $J(x) = -J^T(x)$ represents the interconnection structure, while $R(x) = R^T(x) \geq 0$ is the dissipation matrix due to resistances and frictions.

With the aim to represent the transformed model in PCH form, and applying the d-q transformation for the equivalent single-phase circuit, the state variables can be taken as i_{Ld}, i_{Lq}, v_{cd} and v_{cq}. The energy function is given as:

$$H(i_L, v_c) = \frac{1}{2}Li_{Ld}{}^2 + \frac{1}{2}Li_{Lq}{}^2 + \frac{1}{2}CLv_{Cd}{}^2 + \frac{1}{2}Lv_{Cq}{}^2 \tag{8}$$

The d-q model is developed as follows:

$$\begin{bmatrix} \dot{i}_{Ld} \\ \dot{i}_{Lq} \\ \dot{v}_{Cd} \\ \dot{v}_{Cq} \end{bmatrix} = \begin{bmatrix} 0 & \frac{\omega}{L} & -\frac{1}{LC} & 0 \\ -\frac{\omega}{L} & 0 & 0 & -\frac{1}{LC} \\ \frac{1}{LC} & 0 & -\frac{1}{RC^2} & \frac{\omega}{C} \\ 0 & \frac{1}{LC} & -\frac{\omega}{C} & -\frac{1}{RC^2} \end{bmatrix} \begin{bmatrix} Li_{Ld} \\ Li_{Lq} \\ Lv_{Cd} \\ Lv_{Cq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \bar{u}^d V_{dc} \\ \bar{u}^q V_{dc} \end{bmatrix} \tag{9}$$

In order to design the controller, these two important properties were taken into consideration:

i) Property 1: For the equilibria of equation (9) in the d-q frame, the desired capacitor voltage signal (a pure harmonic free sinusoidal signal with a fixed angular frequency and amplitude) is considered.

$$v_{C*} = V_P \sin \omega t \tag{10}$$

ii) Property 2: It is possible to formulate the control problem as follows, since the complete system is measurable.
   a. A control law is designed such that the voltage regulation is maintained under different load conditions, while maintaining a low THD value.

The energy equation for the 5-level CHMI can be defined as [12]:

$$H_d = \frac{1}{2}L(i_{Ld} - i_{Ld*})^2 + \frac{1}{2}L(i_{Lq} - i_{Lq*})^2 + \frac{1}{2}C(v_{Cd} - v_{Cd*})^2 + \frac{1}{2}C(v_{Cq})^2 \quad (11)$$

where $[i_{Ld*} \quad i_{Lq*} \quad v_{Cd*} \quad v_{Cq*}]^T = \left[\frac{V_P}{R} \quad \omega C V_P \quad V_P \quad 0\right]^T$ are the equilibrium points.

According to [25], it is necessary to assign the interconnection and damping matrices in order to transform the PCH model in equation (9) to the form,

$$\dot{x} = [J_d(x) - R_d(x)]\frac{\partial H_d}{\partial x}(x) \quad (12)$$

where $J_d(x) = -J_d^T(x)$ and $R_d(x) = R_d^T \geq 0$. The derivative of $H_d(x)$ can be expressed as:

$$H_d(x) = -\frac{\partial H_d^T(x)}{\partial x}R_d(x)\frac{\partial H_d(x)}{\partial x} \leq 0 \quad (13)$$

By considering the following properties,

i) (Integrability) $K(x)$ is the gradient of a scalar function:

$$\frac{\partial K}{\partial x}(x) = \left[\frac{\partial K}{\partial x}(x)\right]^T$$

ii) (Equilibrium Assignment) $K(x)$ at x_*, verifies:

$$K(x_*) = -\frac{\partial H}{\partial x}(x_*)$$

iii) (Lyapunov stability) The Jacobian of $K(x)$, at x_*, satisfies the bound:

$$\frac{\partial K}{\partial x}(x_*) > -\frac{\partial^2 H}{\partial x^2}(x_*)$$

Thus, the vector function $K(x)$ satisfies the following equation:

$$\left[J(x) + J_a(x) - \left(R(x) + R_a(x)\right)\right]K(x) = -[J_a(x) - R_a(x)]\frac{\partial H}{\partial x}(x) + g(x)\beta(x) \quad (14)$$

Under these conditions, the closed-loop system $u = \beta(x)$ will be a port-controlled Hamiltonian system as in equation (12). The functions $J_a(x)$ and $R_a(x)$ are given as:

$$J_a(x) = 0, R_a(x) = \begin{bmatrix} r_1 & 0 & 0 & 0 \\ 0 & r_2 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (15)$$

The control-law equations based on the PCH IDA-PB controller is obtained in terms of d-q rotation, which is [12]:

$$\bar{u}^d = \frac{1}{V_{dc}}\left[-r_1 L^2 \widetilde{i_{Ld}} + v_{Cd*} - \omega L i_{Lq}\right] \quad (16)$$

$$\bar{u}^q = \frac{1}{V_{dc}}\left[-r_2 L^2 \widetilde{i_{Lq}} + \omega L i_{Lq}\right]$$

where $\widetilde{\boldsymbol{i_{Ld}}} = \boldsymbol{i_{Ld}} - \boldsymbol{i_{Ld*}}$ and $\widetilde{\boldsymbol{i_{Lq}}} = \boldsymbol{i_{Lq}} - \boldsymbol{i_{Lq*}}$.

Finally, the control signal is given by

$$\bar{\boldsymbol{u}} = \bar{\boldsymbol{u}}^{\boldsymbol{d}} + \bar{\boldsymbol{u}}^{\boldsymbol{q}} \quad (17)$$

Comparing the control equation for the 5-level CHMI with a single-phase H-bridge inverter as in [12], the final control signal is rather similar, except for the fact that through average modeling of the CHMI previously explained in Section 2, the control signal for the 5-level CHMI is represented as,

$$\bar{\boldsymbol{u}} = \{-\mathbf{2}, -\mathbf{1}, \mathbf{0}, +\mathbf{1}, +\mathbf{2}\} \quad (18)$$

Instead of the three-level square wave voltage in a single H-bridge. This proves that the control equation in [12], can be easily extended to cater for CHMIs of higher output voltage levels and thus produces higher output voltage with reduced THD. The following sections present the implementation of the IDA-PBC control signal for the 5-level CHMI through simulation with a performance comparison study based on a single-phase H-bridge inverter.

5. SIMULATION RESULTS AND DISCUSSION

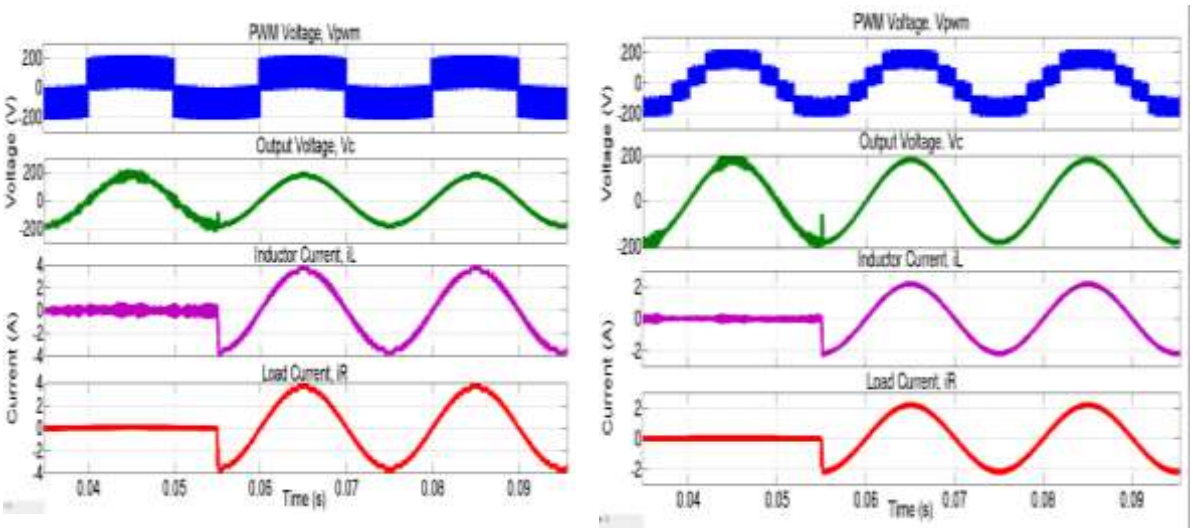
Both systems have been simulated using MATLAB/Simulink for validation purposes. The parameters used in the simulation are as shown in Table 1. The switching devices are IGBT modules commutated at a frequency of 20 kHz using the phase-shift PWM method for the CHMI circuit. The controllers are implemented at a sample time of 2 µs. In order to attenuate the high frequency ripple associated with the PWM pattern, a low-pass LC filter is connected at the output of the inverter. The L and C values have been calculated using the Butterworth filter equation and resulted in a 2.813 µF capacitor and a 0.5 mH inductor; given that the resistor value is marked at 50 Ω. The desired AC output voltage for both circuits is 180 V_{peak}. Hence, the DC voltage source of the H-bridge circuit is 200 V, while the voltage source of the CHMI is 100 V for each H-bridge.

Table 1. Simulation parameters

Symbol	Parameters	Value
V_{dc}	DC Source Voltage for H-bridge inverter	200 V
	DC source voltage for each cell in CHMI	100 V
fs	Switching frequency	20 kHz
Ts	Sample time	2 us
L	Inductor	2.81 mH
C	Capacitor	0.5 uF
m	Modulation index	0.9
f	Frequency	50 Hz
R	Resistor	50 Ω

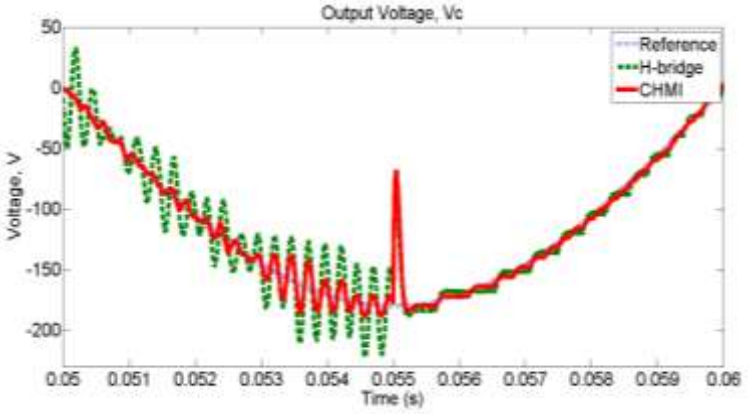
5.1. No Load to Full Load Condition

The first simulation is conducted to observe the dynamic transient response based on the IDA-PBC control algorithm for both inverters, taking into consideration the worst-case condition where a change of load is imposed at the negative peak of the reference output voltage. Initially, the inverter is operated at a no-load condition. Then, at 0.055 s, the resistor nominal value of 50 Ω is connected to provide full-load operation. Figures 5(a) and (b) show the output voltage waveform of the H-bridge inverter and the 5-level CHMI. It is noticed that in both circuits, output voltage regulation is achieved with low THD. Figure 6 shows the comparison made on the output voltage waveforms of both inverters with respect to reference during the load transition. It can be seen in Figure 6(a) that the ripples in the CHMI output voltage during unloading condition is smaller than that of the H-bridge inverter. This is reflected by the fact that the output voltage THD of the former is lower than that of the latter, which are 1.07% and 3.05% respectively. Figure 6(b) shows the transient times of the circuits. The transient time for the H-bridge inverter, t_1 is measured at 180 μs which is slightly longer than the transient time for the CHMI, t_2 that is measured at 160 μs.

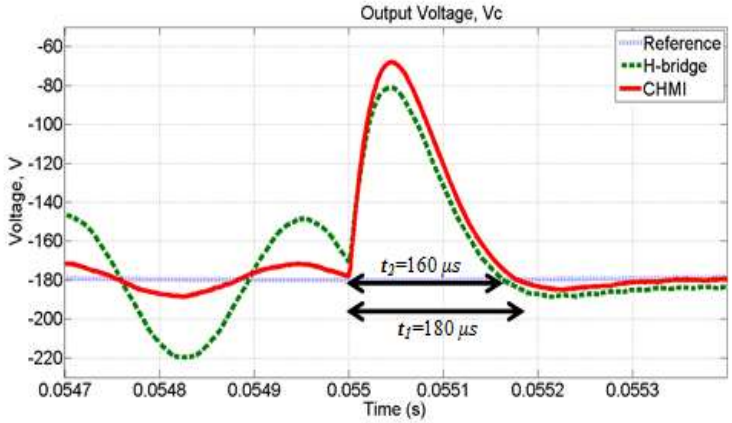


(a) (b)

Figure 5. No load to full load condition, top to bottom, PWM voltage V_{PWM}, output capacitor voltage V_C, inductor current i_L, and load current i_R (a) H-bridge Inverter and (b) 5-level CHMI



(a)

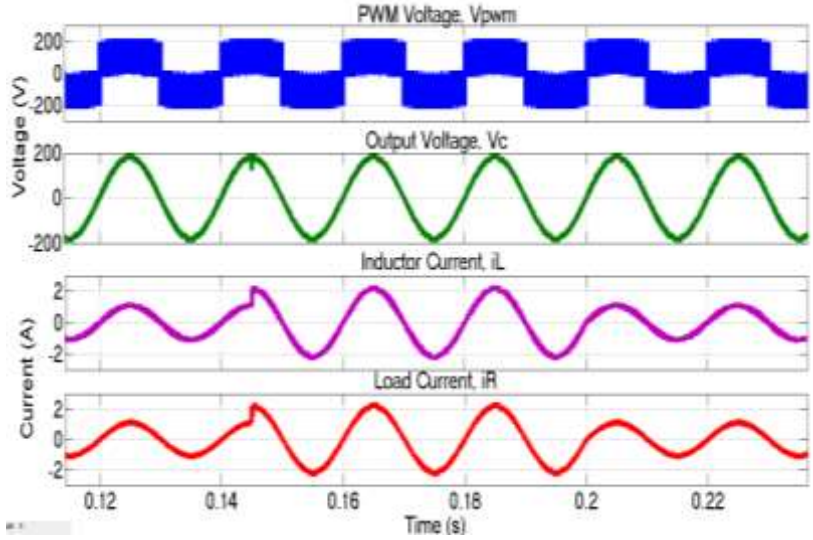


(b)

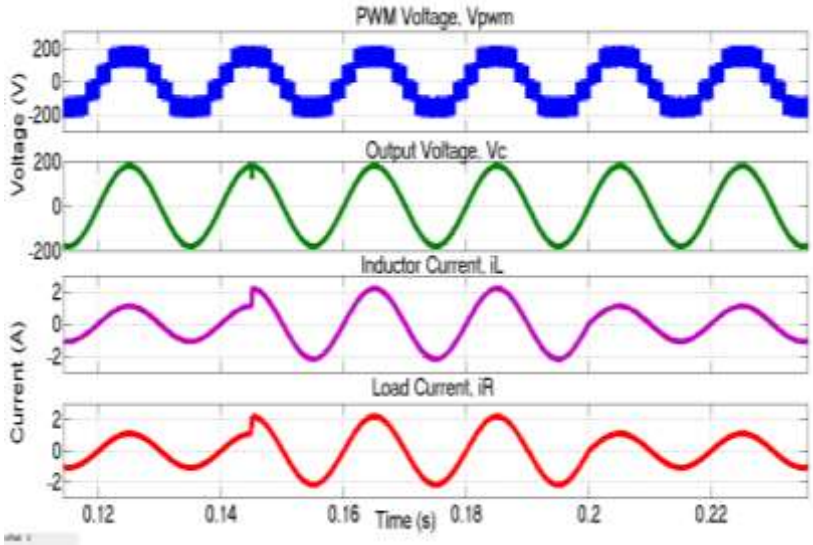
Figure 6. Comparison of output voltage waveform during no load to full load condition showing ripples and transient time, t_1 and t_2 (a) Ripples (b) Transient time

5.2. Load Uncertainty

The simulation is then conducted to evaluate the robustness of the controller with respect to the uncertainty in the load resistance value. A 100% instantaneous step change in the load resistance is applied by changing the resistance from 100 Ω to 50 Ω and vice-versa. The system response under load transition for the H-bridge inverter and the 5-level CHMI are shown in Figures 7(a) and (b) respectively. It is noticed that as the load resistance is reduced, the load and inductor current increase with time while maintaining its stability and high performance, and most importantly, the output voltage regulation is maintained. Comparison of the output voltage waveforms of the H-bridge inverter and the CHMI with the reference voltage waveform is shown in Figure 8. In Figure 8 (a), it is noticeable that the output voltage of the H-bridge inverter produces more significant ripples compared to CHMI's. This leads to higher output voltage THD for the H-bridge inverter which is 4.19 % and lower output voltage THD for the CHMI which is 1.59 %. Figure 8(b) shows the settling time of the inverter circuits during load change. The settling time for the H-bridge inverter, denoted as t_1 is measured at 185 μs while the settling time for the CHMI, t_2 is measured at 170 μs.

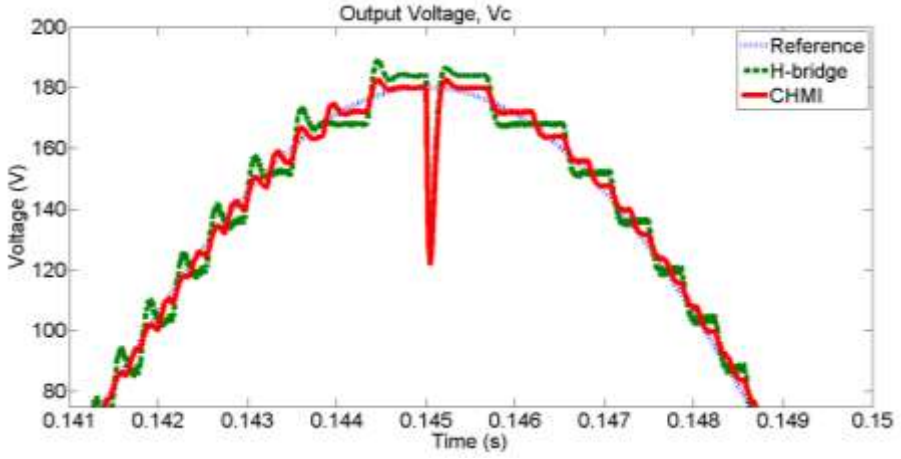


(a)

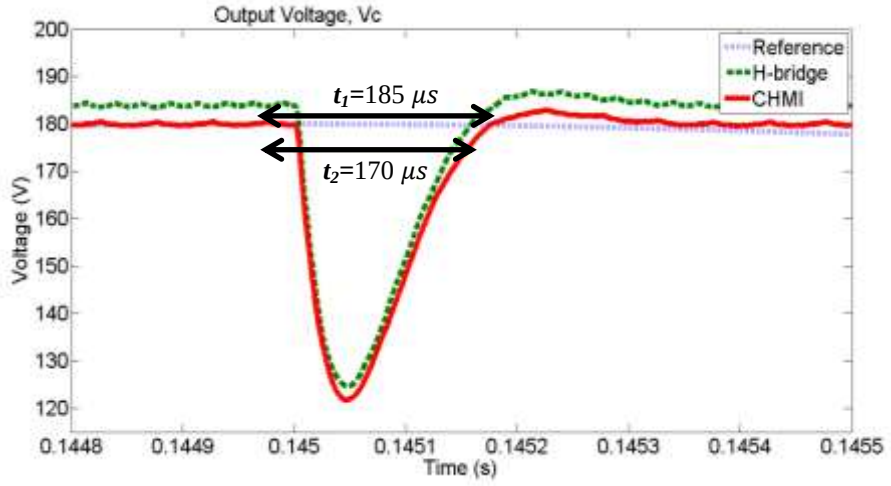


(b)

Figure 7. System response under transient operating conditions, top to bottom, PWM voltage V_{PWM}, output capacitor voltage v_C, inductor current i_L, and load current i_R (a) H-bridge Inverter and (b) 5-level CHMI



(a)



(b)

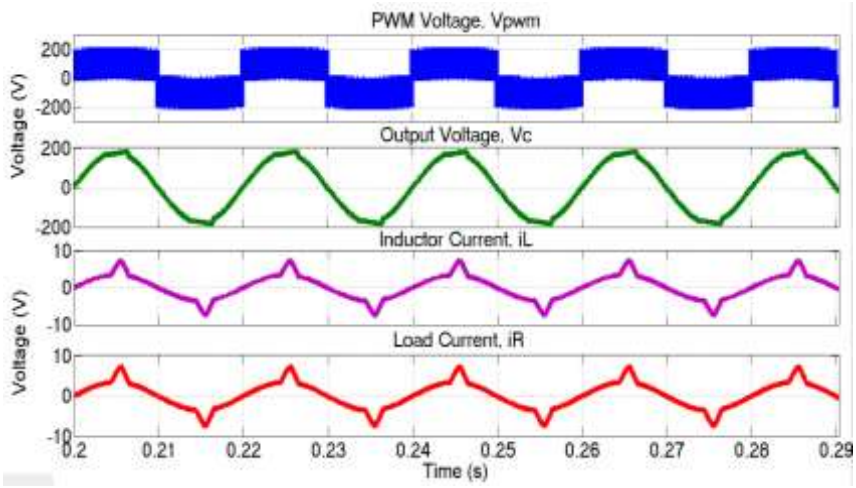
Figure 8. Comparison of output voltage waveform during load uncertainties showing ripples and response time, t_1 *and* t_2 (a) Ripples (b) Response time

5.3. Structural Uncertainty Test - Nonlinear Load

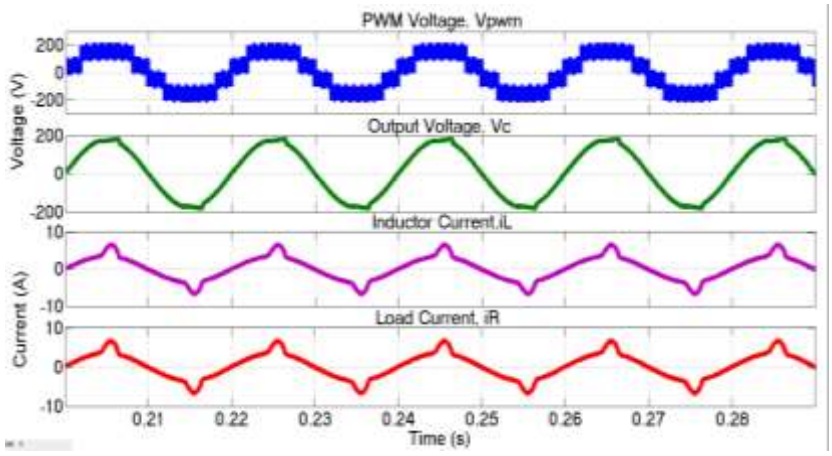
The final simulation study included in this paper is also related to the uncertainty on the load; specifically, the structural uncertainty. In this case, a nonlinear load consisting of a single-phase full-bridge rectifier circuit with a capacitor and a resistor is connected in parallel to the inverter circuits. The resistance is chosen as 50 Ω whereas the capacitance is set at 350 μF. The system response for both the H-bridge inverter and the 5-level CHMI is shown in Figures 9(a) and (b) respectively. The inductor and load currents are both distorted, as expected. However, output voltage regulation is remarkably achieved, even in the presence of the nonlinear load. The H-bridge inverter gives an output voltage THD of 3.94%, while a lower output voltage THD of 1.62% is obtained by the 5-level CHMI. Table 2 provides the summary of results obtained from the simulation study.

Table 2. Comparison between the H-Bridge Inverter and CHMI

Load	Measurement	H-Bridge Inverter	5-level CHMI
No load to full load condition	THD (%)	3.05	1.07
	Transient time (μs)	180	160
Load uncertainty	THD (%)	4.19	1.59
	Settling time (μs)	185	170
Structural uncertainty	THD (%)	3.94	1.62



(a)



(b)

Figure 9. System response structural uncertainty, top to bottom, PWM voltage V_{PWM}, output capacitor voltage v_C, inductor current i_L, and load current i_R (a) H-bridge Inverter and (b) 5-level CHMI

6. CONCLUSION

The IDA-PBC control algorithm previously applied to an H-bridge inverter in [12] can be extended for application in a 5-level CHMI, as detailed in Section 4. The newly derived control algorithm for the latter is validated through a series of simulation under various loading conditions. The controller has managed to achieve its objective in maintaining output voltage regulation while ensuring low THD in both types of inverters. However, the results obtained for the 5-level CHMI have shown a remarkably faster time response and a lower output voltage THD during all loading conditions compared to those of the H-bridge inverter. This is as expected due to the advantages offered by the multilevel inverter topology itself. For future work, new interconnections and damping matrices functions can be proposed to tune the controller for a much better output performance.

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