Quasi-Z-Source Inverter Topologies with Reduced Device Rating: a Review

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ABSTRACT

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Keyword:

Continuous input current Quasi Z-Source inverter Reduced device rating Quasi-Z-Source Inverter (QZSI) has introduced a new wave of interest in engineering industry and research. Reduction in device rating has been the main objective in introducing QZSI topologies. The introduced topologies in QZSI have proven to be feasible in a wide range for high power with medium voltage applications. This paper mainly focuses on QZSI topologies with continuous input current conduction and also power conditioning in the renewable energy system. Based on a detailed comparison of these topologies suitable QZSI can be arrived for a given application.

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1. INTRODUCTION

Quasi-Z-Source Inverter (QZSI) is derived from the original Z-Source Inverter (ZSI) where it can be utilized to all power converters i.e., DC-AC, DC-DC, AC-DC, AC-AC. ZSI can operate in boost inverter or buck inverter but not as buck-boost inverter [1]-[3].By introducing QZSI some of the disadvantages in traditional ZSI can be overcome. The QZSI has the wide range of applicability in the renewable energy system, where it gives a single stage power conversion with buck-boost characteristics and improve the reliability of the inverter [4]-[8]. In shoot through states, both power switches in a leg are turned on at the same time and it is used to step up the voltage and the output voltage in QZSI can be boost to designed value. Research based on these QZSI has concentrated on modelling and control, photovoltaic and other electrical applications. The QZSI can buck and boost the input voltage in single stage with two control variables; shoot through and modulation index. New topologies of QZSI which has been derived from original ZSI can be proposed for PV applications, because of continuous input current and reduced capacitor rating. QZSI has a prescribed application to combine with renewable energy system for a wide voltage range to distribute for power grid [9]-[12].

Moreover, the voltage stress on capacitors and current stress on inductors and diodes in QZSI are lower than traditional ZSI for same input and output voltage. QZSI avoids inrush current at starting, where destroy of the devices can be avoided and also these topologies are more viable for solar cell and fuel cell applications it may acquire high voltage gain to match the source voltage difference [13], where for the same input and output voltages, it can use lower duty cycle and higher modulation index, which results in less switching stresses, better output power and lower input current ripple. The advantage of including inductors in the QZSI network will limit the current ripple through the devices during boost conversion mode. During shoot-through, the inductor current increases linearly. By using the new QZSI topologies the inverter draws current with minimal ripple from the Solar PV panel by reducing the size of filtering capacitors. QZSI, produce the desired output voltage to the grid, regulate the battery state of charge and control the PV output power to maximize the energy production [14]. Several extended topologies are described in further sections, such as Switched Inductor QZSI (SL-QZSI), Switched Coupled Inductor QZSI (SCL-QZSI), two switched inductor QZSI. By using QZSI in Direct Matrix Converter (DMC) an additional input filter can be avoided [15]-[20]. Hence this QZSI topologies suit solar cell and fuel cell that may require high voltage gain to combine with source voltage difference.

2. QUASI Z-SOURCE INVERTER TOPOLOGIES

This section discusses the principle of operation of various QZSI topologies with reduced device rating. Traditional Z-Source inverter as shown in Figure 1 [1], provides both buck and boost operation. The impedance network consists of two inductors (L_1 and L_2) and two capacitors (C_1 and C_2) where it couples the main inverter circuit to the DC voltage source.



Figure 1. Basic Z-Source Inverter

The Quasi Z-Source inverter topologies have one big advantage, such as the DC power supply and the inverter has the same ground connection. This facilitates the design of the driver circuits and current sensing. Also, EMI problems are decreased. QZSI also has added advantage such as higher modulation index with lower component voltage stress.

QZSI is obtained from the basic framework of the ZSI. Hence QZSI can be used as a replacement for all the applications in which ZSI is used mainly because of the above mentioned advantages. In Figure 2 capacitor voltage of C_2 is much lesser than that of C_1 [3].



Figure 2. Basic Quasi Z-Source inverter

$$V_{c1} = \frac{1 - d_0}{1 - 2d_0} V_{dc}$$
(1)
$$V_{c2} = \frac{d_0}{1 - 2d_0} V_{dc}$$
(2)

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$$= V_{c1} + V_{c2} = \frac{V_{in}}{1 - 2_{d0}} = BV_{dc}$$
(3)

In the above equations $d_0=T_0/T_s$, where T_0 is the shoot-through interval among switching cycle Ts, where V_{c1} and V_{c2} are voltage of capacitors in qZI, \hat{v} is the peak voltage and B is defined as voltage boost factor [17].

2.1. Switched-Inductor Quasi-Z-Source Inverter (SL-OZSI)

The combination of inductors (L_2, L_3) and energy diodes (D_1, D_2, D_3) acts as a switched inductor that is the reason this topology is named SL-QZSI where the inductors and capacitors will resonate. Inductors, capacitors and diodes are to be added to the original ZSI to produce high DC link voltage for the main power circuit from a very low input DC voltage and also to improve the boost factor [21]-[24]. SL-QZSI gives a substantial boost inversion compared to classical ZSI/QZSI [25].

In Figure 3 [26], Switched-Inductor QZSI adds only three diodes and one inductor where it boost factor enhances from 1/1-2d to $(1+d)(1-2d-d^2)$. In non-shoot through state it has six active states and two zero states, where D_{in} and D_1 are ON, while D_2 and D_3 are OFF, with L_2 and L_3 connected in series. The capacitors C1 and C2 are charged while the inductor L1, L2, L3 transfers energy from DC source to the main circuit. During shoot- through state, D_{in} and D₁ are off, while D₂ and D₃ are on.L₂ and L₃ are connected in parallel, the capacitors C_1 and C_2 are discharged while inductors L_1 , L_2 & L_3 store energy [26].

Figure 3. Switched-Inductor quasi Z-Source Inverter

2.2. Two Switched- Inductor Ouasi-Z-Source inverter

The addition of inductor results in a continuous input current. Two switched SL-QZSI has a flatter input current where the DC source is directly connected to switched-inductor cell as L_1 , L_3 , D_1 , D_3 , D_5 or L_2 , L₄, D₂, D₄, D₆ [27]-[34]. In this topology, the inductor or switched inductor is connected to a DC source as shown in Figure 4 [30], when the switched inductor cell is connected to a DC source ripples will appear on the input current and hence it is abbreviated as rSL-QZSI. If the inductor is connected to the DC source then it is abbreviated as cSL-QZSI which is shown in Figure 5 [30].

Figure 4. ripple Switched-Inductor QZSI





3)



Figure 5. capacitor Switched-Inductor QZSI

2.3. Switched-Coupled-Inductor Quasi-Z- Source Inverter (SCL-QZSI)

SCL-QZSI shown in Figure 6 is achieved by replacing inductor L_2 in the original QZSI with a combination of switched capacitor C_3 and three windings N_1 , $N_2 \& N_3$. Windings N_1 and N_2 have same no. of turns i.e., $N_1=N_2$ and turns ratio of winding $n=N_3/N_1=N_3/N_2$.



Figure 6. Switched- Coupled Inductor Quasi Z- Source Inverter

The voltage spikes across the switch are caused due to energy stored in the leakage inductance of the coupled inductor, the leakage inductance of SCL utilized in series with C_3 and the capacitor C_2 will absorb the energy stored in the leakage inductance. It adds single capacitor and two diodes to the QZSI [35]-[36], achieves a boost factor 3/1-4D which is higher than that of existing QZSI. The input inductor current ripple and the flux density swing are smaller than QZSI, for the similar input values the inductor current is very low, the flux density and no. of turns or core size of inductor L_1 is smaller in the Switched-Coupled Inductor Quasi Z-Source Inverter [37]-[38].

During shoot through state, diode D_{in} is OFF while diodes D_1 and D_2 are on. Windings N_1 and N_2 will get charged by C_1 , while C_3 obtains energy from C_1 through winding N_3 . This enhances the boost factor and charging current C_3 is restricted by the leakage inductance of SCL. During non-shoot through state, D_{in} will conduct while D_1 and D_2 are OFF. C_1 and C_2 are charged whereas the windings N_1 , N_2 , N_3 and C_3 are in series, where C_2 will absorb the energy stored in the leakage inductance of SCL, where voltage spikes are not created which is recycled.

2.4. Tapped-inductor Quasi-Z-Source inverter (TL-QZSI)

The combination of L_1 , D_2 and D_3 acts as a tapped inductor QZSI. During shoot-through state the inductance of winding N_1 is effective, whereas in non-shoot through state both the windings N_1 and N_2 are effective [39]-[41]. By designing this topology, amplitude of the bus voltage can be significantly stepped up and the boost inversion ability of the whole inverter can be significantly improved by 16.5% compared to QZSI. Inheriting the shoot- through time interval of the traditional ZSI the reliability of the whole inverter can be improved. The input current is continuous, voltage stress is reduced and component count is minimized compared to traditional ZSI [42]-[44].



Figure 7. Tapped inductor Quasi Z-Source inverter

2.5. Quasi-Z-Source Direct Matrix Converter (QZSDMC Topology)

Z-Source Direct Matrix Converter (ZSDMC) is derived from traditional Direct Matrix Converter (DMC). By adding inductors, capacitors, switches (each three) QZSDMC is formed as shown in Figure 8 [45]. This addition can increase the voltage gain 4 to 5 times or higher than QZSDMC and also there is no phase shift [46]-[49].



Figure 8. Quasi Z-Source Direct Matrix Converter

Both ZSDMC and QZSDMC can boost power factor more than 0.866. However, QZSDMC has low input value, low output harmonics and higher power factor than ZSDMC. QZSDMC has a lower component rating, compact size, high efficiency and a wide range of buck-boost Matrix Converter [45],[50]-[53].

During shoot-through state S_a , S_b , S_c is OFF and output of Quasi Z-Source is shorted for boost operation. During non shoot-through S_a , S_b , S_c , is ON for normal DMC operation. Due to symmetry of the system, inductances of $(L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, L_{c2})$ have the same value , capacitors C_{a1} , C_{a2} , C_{b1} , C_{b2} , C_{c1} , C_{c2} also have the same value. In case of switching cycle T_s , the time interval of shoot-through is T and the time interval of non shoot-through state is T_1 . Hence $T_s = T + T_1$ and shoot through ratio is $D = T/T_s$.

2.6. Extended Boost Active Switched-Capacitor/ Inductor Quasi-Z-Source Inverter (ASC/SL-QZSI)

ASC/SL-QZSI gives higher boost ability and produces lower voltage stress across the switches in the inverter. If it requires high boosting rate it can be cascaded easily by adding a single inductor and three diodes. In this topology, capacitor and inductor given in QZSI are removed by adding one diode and one switch as shown in Figure 9 [54]. During shoot-through the load terminal is shorted by conducting the upper and lower switching devices on any phase leg, where switch S₇ is ON, diodes D₁ and D₂ are off. The capacitor C is discharged while the inductor L₁ stores energy from the input. During non shoot-through state switch S₇ is OFF, where diodes D₁ and D₂ are ON. Capacitor C is charged and inductor L₁ transfers from energy DC input source to inverter.





Figure 9. Basic Active Switched Capacitor QZSI

ASC/QZSI has cell that consists of one inductor and three diodes as shown in Figure 10 [54]. It provides higher boost ability and achieves lower voltage stress across the switching devices of main inverter [55]-[57]. In shoot-through state S_7 is turned on, the diodes D_1 and D_2 are also on whereas D_a , D_b and D_3 are turned OFF, inductors L_1 and L_2 are connected in parallel and they store energy from the DC input source V_{dc} and capacitor C is discharged through S_7 .



Figure 10. Active Switched Capacitor/ Switched Inductor QZSI

During non shoot-through switch S_7 is turned OFF, diodes D_a , D_b and D_3 are also ON where diodes D_1 and D_2 are OFF, inductors L_1 and L_2 connected in series. DC input voltage and two inductors transfer energy to both the inverter and capacitor through D_a , D_b and D_3 where capacitors are charged [54],[58]-[61].

3. RESULTS AND DISCUSSIONS

Based on the performance characteristics of different QZSI topologies discussed in previous section, Table 1 gives a brief description of their advantages and limitations for identifying a suitable topology for the prescribed application. From the review, it is observed that SCL-QZSI is a highly modular structure, whereas the QZSDMC topology can be appreciated for its sheer simplicity in terms of design. Structure such as SL-QZSI, Two Switched-Inductor QZSI, TL-QZSI and ASC/SL QZSI requires low input DC voltage. It can be said that when attempts are made to reduce the device rating, the following features may be hampered: continuous current conduction in input side and desired output voltage, because of which the topologies found restrictions for high voltage applications. The qualitative features of reduced device rating QZSI topologies are summarized in Table.2 in terms of boost factor and voltage gain.

3.1. Performance Characteristics

The performance characteristics of Duty Ratio (D) vs Boost Factor (B) of different QZSI topologies (discussed in section-2) is shown in Figure 11. As illustrated below in Figure 11, the boost factor increases respectively with increase in duty ratio, SCL-QZSI achieves highest boost factor of 40 for a duty ratio of 0.23. As boost factor increases efficiency also increases accordingly. The graph is plotted by using equations of boost factor specified in Table 2.



Figure 11. Plot of Duty Ratio (D) vs Boost factor (B)

The characteristics of Modulation Index (M) vs Voltage Gain (G) of different topologies is shown in Figure 12, As modulation index increases the voltage gain decreases by analyzing the below Figure 12 SCL-QZSI has a maximum voltage gain of 37.5 for a modulation index of 0.77. As voltage gain increases there will be reduction in current ripple. The graph is plotted by using equations of voltage gain specified in Table 2.



Figure 12. Plot of Modulation Index (M) vs Voltage Gain (G)

Tuble 1. Advanueses and Emmanons of Quasi 201 Topologies				
Topology	Advantages	Limitations		
SL-QZSI	Reduced voltage stress on capacitors, lower shoot-through current.Lower current stress on inductors and diodes.	• High voltage gain is not possible in higher modulation index.		
Two SL-QZSI	 Suppress inrush current at start-up. 	 High duty cycle ratio is not possible. 		
SCL-QZSI	Higher modulation index with lower component-voltage stresses.No. of turns and size of the input inductor can be	• Suitable for applications that require a single- stage high-step up boost inversion of low dc- voltage source.		
	reduced.			
TL-QZSI	• Lower current stress on inductors and diodes.	• Widening shoot through zero state will inevitably decrease modulation index and in turn reduce the output voltage amplitude, and will also increase device voltage stress.		
QZSDMC Topology	Less Component ratingLess input and output harmonics.Higher power factor and efficiency	• Voltage transfer ratio between input and output is constrained up to 0.866		
ASC/SL- QZSI	 Achieves lower voltage stress across the switching devices of main inverter If it requires high boost rating, cascading at the impedance network can be done easily by adding cells. 	• In some areas it require high voltage gains to obtain desired ac output voltages for low-voltage energy sources which is not possible		

Table 1. Advantages and Limitations of Quasi ZSI Topologies

Quasi Z Source Inverter Topologies with Reduced Device Rating (V. Raghavendra Rajan)

Table 2. Comparative Analysis of Quasi ZSI Topologies			
Topology	Literature	Boost Factor	Voltage gain
SL-QZSI	Proposed in [24]	$B = \frac{1+D}{1-2D-D^2}$	$G = \frac{8\pi^2 M - 6\sqrt{3}\pi M^2}{-8\pi^2 + 24\sqrt{3}\pi M - 27M^2}$
Two Switched Inductor QZSI	Proposed in [28]	$B_r = \frac{1+D}{1-3D}, B_c = \frac{1}{1-3D}$	$G_{\rm r} = \frac{2M - M^2}{3M - 2}, G_{\rm c} = \frac{M}{3M - 2}$
SCL- QZSI	Proposed in [36]	$B = \frac{3}{(1 - 4D)}$	$G = \frac{3M}{4M - 3}$
TL-QZSI	Proposed in[42]	$B = \frac{1 + D_0}{1 - 2D_0 - D_0^2}$	$G = \frac{M[(1 - M) + 1]}{2M - N(1 - M)^2 - 1}$
QZSDMC	Proposed in [18]-[19],[47]	$B = \frac{1}{\sqrt{3D^2 - 3D + 1}}$	$G = \frac{M}{2M - 1}$
ASC/SL-QZSI	Proposed in [58]-[59]	$B = \frac{1+D}{1-3D}$	$G = \frac{M(4 - \sqrt{3}M)}{3\sqrt{3}M - 4}$

4. CONCLUSION

QZSIs have gained its importance for high power, medium power and low power applications. Many researchers have introduced specific topology for deliberate solutions to a given application. Also, the topologies have been proposed with high output efficiency with a reduced device rating. In this paper, a review of six types of reduced device rating QZSI topologies is presented. Based on the review, it is suggested that capacitor voltage should be optimized so that voltage stress on switching devices can be minimized and also duty cycle on the input side should be varied which is important to protect from overvoltage on switching devices. In this paper, qualitative and quantitative features of QZSI topologies have been discussed and a comparative analysis has been made so as to make an easier selection of topology. In addition, the paradigm presented in the paper will help to evaluate the proposed QZSI topologies.

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