

Maximum Boost Control for 7-level Z-Source Cascaded H-Bridge Inverter

R. Palanisamy¹, K. Vijayakumar²

Department of Electrical and Electronics Engineering, SRM University, Kattankulathur, Chennai, India

Article Info

Article history:

Received Feb 14, 2017

Revised Apr 14, 2017

Accepted Apr 28, 2017

Keyword:

Cascaded H-Bridge inverter
Maximum boost control (MBC)
Pulse width modulation (PWM)
Z-source network

ABSTRACT

This paper proposes maximum boost control for 7-level z-source cascaded h-bridge inverter and their affiliation between voltage boost gain and modulation index. Z-source network avoids the usage of external dc-dc boost converter and improves output voltage with minimised harmonic content. Z-source network utilises distinctive LC impedance combination with 7-level cascaded inverter and it conquers the conventional voltage source inverter. The maximum boost controller furnishes voltage boost and maintain constant voltage stress across power switches, which provides better output voltage with variation of duty cycles. Single phase 7-level z-source cascaded inverter simulated using matlab/simulink.

Copyright © 2017 Institute of Advanced Engineering and Science.
All rights reserved.

Corresponding Author:

R. Palanisamy,
Department of Electrical and Electronics Engineering,
SRM University, Kattankulathur, Chennai, India.
Email: lsntl@ccu.edu.tw

1. INTRODUCTION

In recent years multilevel inverters are mostly prepared compare conventional voltage source inverters (VSIs). The main benefit of static power electronic converter is engendering ac output voltage from dc voltage [1]. In traditional three phase VSI has 6 switches and each leg consists of 2 switches. And it has totally 8 switching state vectors, in that 6 are active vectors and 2 zero vectors. Both switches of any leg can never switched ON at same time [2], which leads to short circuit (shoot-through state) and damage the inverter circuit. Also the VSI has more harmonic content compare to multilevel inverters. Generally the classical multilevel inverters are neutral point clamped, flying capacitor and cascaded h-bridge inverter. Each type of inverter has its own merits and demerits [3]-[4]. Mostly cascaded h-bridge inverter prepared for z-source network and variable source and renewable energy applications [5]. The limitations of VSI circuit is overcome by cascaded h-bridge inverter such as reduced harmonics, output is staircase (nearly sinusoidal) waveform, di/dt protection, improved output voltage & current control, common mode voltage reduction and electromagnetic interference [6]-[7].

The proposed z-source network has advantage, it can operate in shoot through state and which boost the output voltage level. The output voltage is boosted than applied dc bus input voltage and it avoids the usage of additional boost converter. The consistency of system can improved significantly and it has higher efficiency, which is able to buck or boost the applied input voltage [8].

The output voltage from an inverter system can be accustomed by implement the control inside inverter scheme itself. The PWM variable speed drive systems are increasingly for industrial applications and it has better performance in power electronic circuits and semiconductor devices [9]. Numerous pulse width modulation schemes are developed and tested with conventional VSI system. Many PWM schemes implemented to generate variable voltage and variable frequency. Based on these PWM scheme the width of

pulses are decided and reduce its harmonic content [10]-[11]. Maximum boost controller used to increasing the output voltage and induce the shoot through state condition to the power converters [12].

This paper exposes the maximum boost control for 7-level z-source cascaded h-bridge inverter and difference between boosted voltage and modulation index. Z-source network avoids the usage of external dc-dc boost converter and improves output voltage with minimised total harmonic distortion. Z-source network utilises individual L-C impedance network amalgamation with 7-level cascaded h-bridge inverter and it surmounts the conventional voltage source inverter. The paper includes, part-2 explains operation of 7-level cascaded h-bridge inverter, part-3 gives maximum boost control and part-4 describes simulation results and discussion.

2. Z-SOURCE CASCADED H-BRIDGE INVERTER

2.1. Cascaded H-bridge inverter

An alternative multilevel inverter structure with less power devices responsibility estimated to other a assortment of multilevel structures is known as cascaded H-bridge inverter (CHBI) and the structure is used on the sequence association of H-bridge cell with separate dc sources [13]. A single phase n-level cascaded h-bridge inverter is shown in Figure 1. Each individual dc source connected in full bridge or half bridge inverter circuit [14]. Each inverter circuit can have three different levels $+V$, 0 , $-V$ by linking dc output to the ac output by various combinations of switches are S_1 , S_2 , S_3 & S_4 . To acquire $+V$ output voltage, the switches S_1 & S_3 are turned ON. And to obtain the $-V$ voltage, the switches S_2 & S_4 are switched ON. When both switches in a leg are switched ON, the output is 0 .

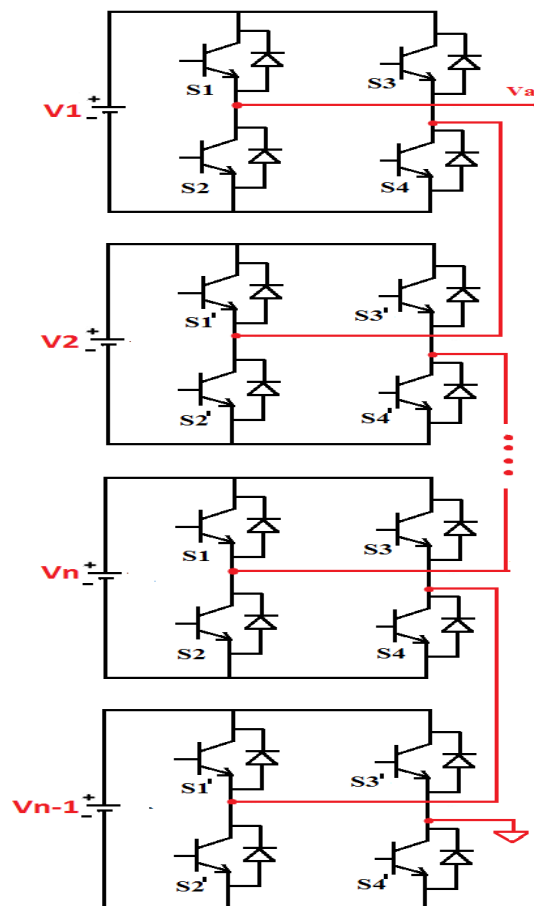


Figure 1. N-level cascaded h-bridge inverter

The ac output of different VSI full bridge inverters are connected in series to obtain the synthesized output voltage waveform from the proposed cascaded inverter scheme. For example if inverter has 9 level,

the 3 full bridge inverter are connected serially to acquire the 9-level output voltage. The multilevel cascaded inverter are applicable such as FACTS devices, static var application, connect with renewable energy sources and fixed battery application based converter system. The inverter could be controlled to regulate the power factor of the current drawn from the dc source or battery of electrical system where the cascaded inverter is connected. Mainly cascaded inverters are used in electric vehicle, grid connected applications, solar cells and fuel cells.

2.2. Operation 7-level z-source cascaded h-bridge inverter

The cascaded h-bridge multilevel inverter uses the numerous number of units to construct additional ac voltages by back to back correlation of h-bridge cells in sequence manner. Each h-bridge cell encloses 4 switches with dissimilar combinations of switch locations find the dissimilar voltage levels. Two switching amalgamations are contains for producing 0 output voltage. 7-level single phase z-source cascaded h-bridge inverter is shown in Figure.2. In that switches S1 and S3 are connected to generate maximum positive voltage and S2 & S4 are associated to engender maximum negative voltage from the proposed scheme. The number of output voltage level from a cascade H-bridge inverter depends on the number of individual dc sources located to the scheme. The voltage level in cascaded h-bridge circuit is shown in Equation 1.

$$J=2D+1 \quad (1)$$

Here, D-number of dc sources, J- number of levels.

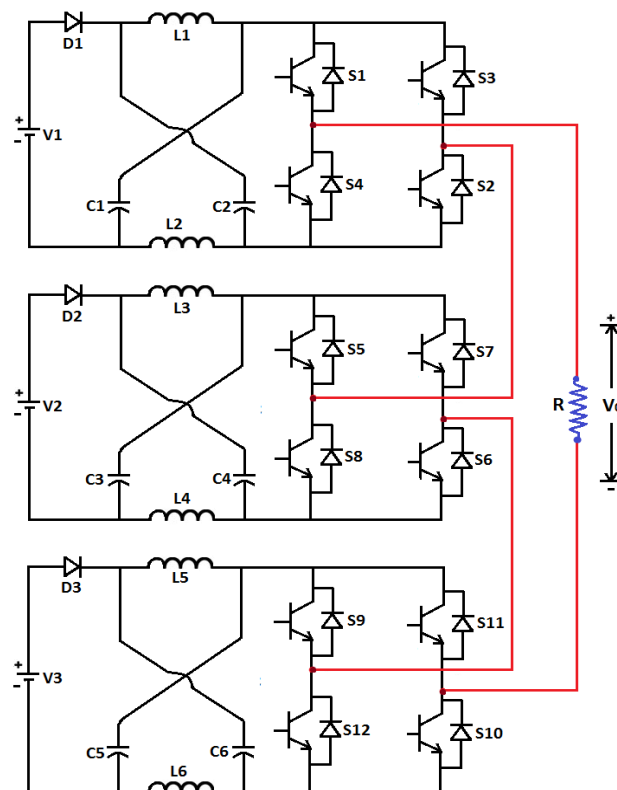


Figure 2. 7-level z-source cascaded h-bridge inverter

While preparing the multilevel converter system, the amount harmonic ripples in the meticulous system commence reducing and voltage stress in the each power switching devices begins to minimizing. To construct better output voltage level and developed output current control, z-source network is added in frontage of cascaded inverter system. By addition this impedance network scheme and using shoot through state principle the output voltage increased 2 times better than of traditional VSI scheme. The quantity of voltage across in the capacitors C1 & C2 will be similar in all the z-source impedance network scheme is,

$$V_{c1} = V_{c2} = \frac{1 - \frac{T_p}{T}}{1 - 2\frac{T_p}{T}} V_{out} \quad (2)$$

Then the boosting factor for the z-source network is,

$$H = \frac{1}{1 - 2\frac{T_p}{T}} \quad (3)$$

Where, H is the boosting factor, T_b be turns on time period and T is total time period of the system. Where the T_0 is the shoot through state condition and T is the total time period and D_0 duty ratio is defined as,

$$D_0 = \frac{T_0}{T} \quad (4)$$

The L-C network amalgamations are stated with equal conditions like $C1=C2$ and $L1=L2$ (ideal condition). Based on these conditions the quantity of output voltage production in the proposed scheme is resolute. In this projected scheme for engender the 7-level output voltages the 3 cascaded h-bridge cells are associated with individual z-source network scheme and disengage dc sources. Based on these projected state and L-C amalgamation the output voltage engendered is two times of the functional input and much greater than the conventional schemes.

3. MAXIMUM BOOST CONTROLLER (MBC)

In order to preserve or reduce system cost or structure, imperative to maintain the shoot through ratio as constant. At the same to reduce the voltage stress across the power switches, the boosted voltage with proper variation of modulation index. Figure 3 shows the maximum boost controller, which acquire better voltage gain with constant value of shoot through state. Based on the MBC control, the z-source inverter operated either on upper shoot through or lower shoot through mode. Constant boost ratio of the proposed system defined as,

$$B = \frac{\pi}{[3\sqrt{3}M] - \pi} \quad (5)$$

Where the B is boost ratio & M is modulation index. And the ripple content in the inductor is,

$$\epsilon L_1 = \frac{V * K}{2 * \pi * 6 * f * L} \quad (6)$$

Here V is applied voltage, K-constant, f-frequency, L- design value inductance.

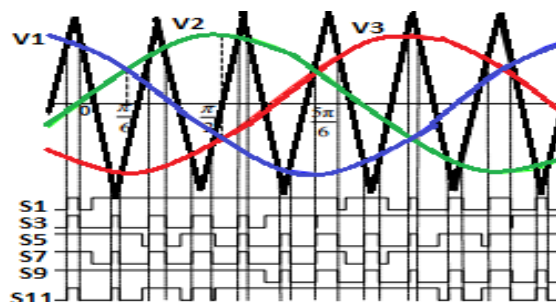


Figure 3. Maximum boost controller (MBC) gating pulse

A triangle carrier wave is evaluated with a three phase reference sine wave, each phase for a positive side switch shoot through state occurs every time the triangle peak value overshoots the sinusoidal peak amplitude, so twice for each phase in one cycle of operation. At other instants when the sinusoidal magnitude is greater, the inverter exhibits active vector switching states. Using minimum /maximum utility for the three

phase sinusoidal its upper and lower wrapper waveforms are compared alongside the same carrier to engender shoot through pulses for the positive and negative carrier peak values respectively, which added using OR gate circuit.

4. SIMULATION RESULTS

To verify the performance of the proposed system, this is simulated by matlab2016a. And it has the following simulation parameters are, $C1=C2=1000\mu\text{F}$, $L1=L2=1\text{mH}$, switching frequency of 10 kHz and modulation index of 1. Maximum boost controller performance is simulation is shown in Figure 4. The gating pulses generation for 7-level z-source cascaded h-bridge inverter is shown in Figure 5.

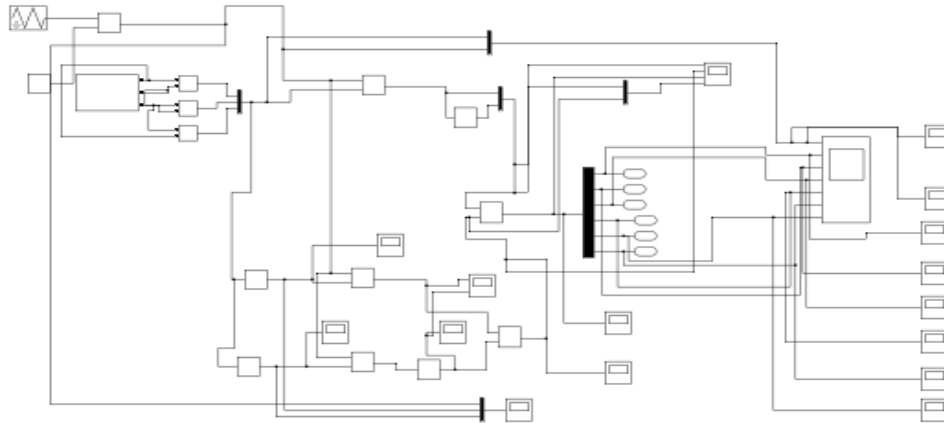


Figure 4. MBC matlab simulink performance

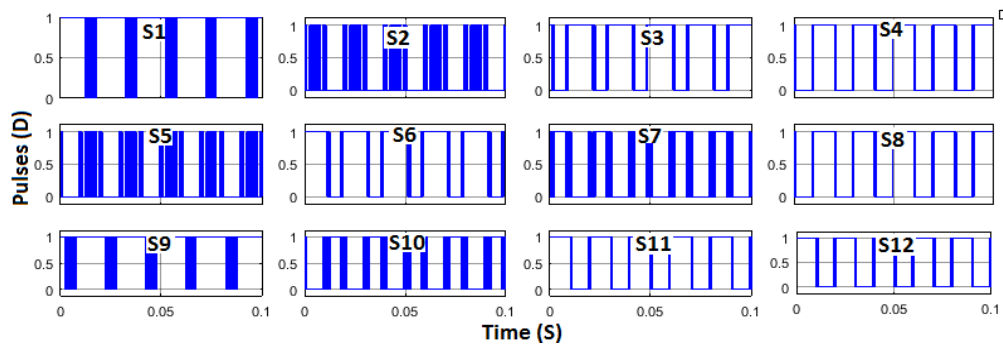


Figure 5. Gating pulses of 7-level z-source cascaded inverter

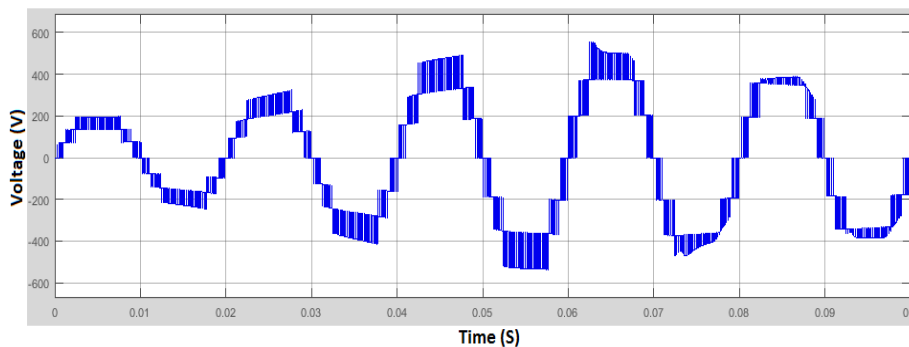


Figure 6. 7-level z-source cascaded inverter output voltage

In Figure 6 exposes proposed 7-level z-source cascaded inverter boosted output ac voltage with 463V from dc input voltage of 300V, which is boosted using the shoot through state by maximum boost controller. And Figure 8 shows the 7-level z-source cascaded inverter output current of 9.34A. The ripple contents present in the output voltage and current is eliminated by using second order filter, which is exposed in Figure 7 and Figure 9 correspondingly.

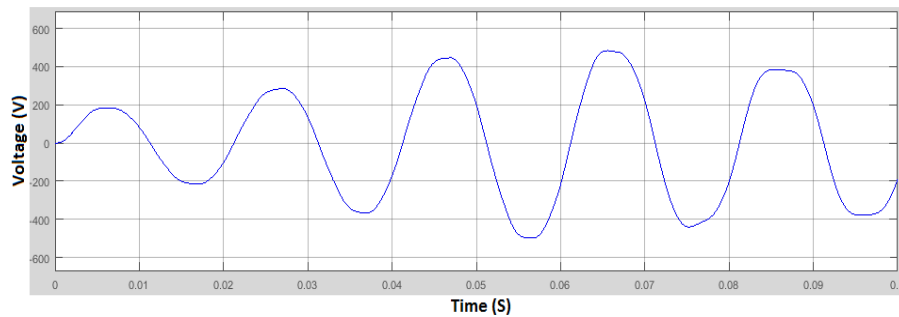


Figure 7. Filtered output voltage for 7-level z-source cascaded inverter

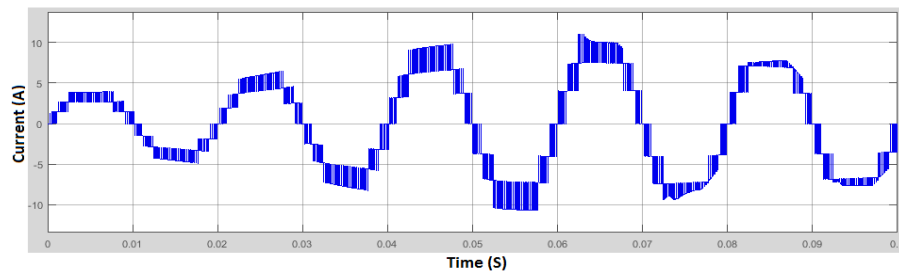


Figure 8. Output current of 7-level z-source cascaded inverter

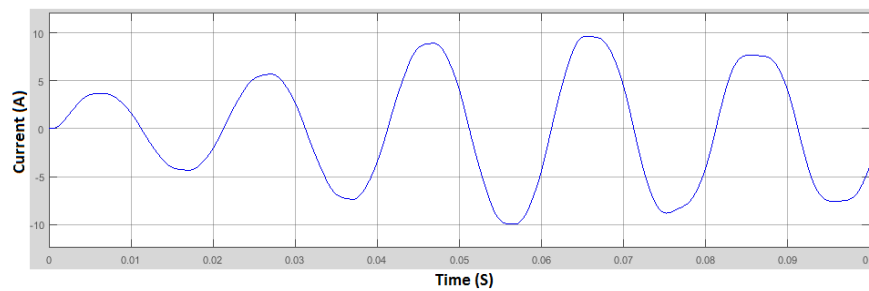


Figure 9. Filtered output current of 7-level z-source cascaded inverter

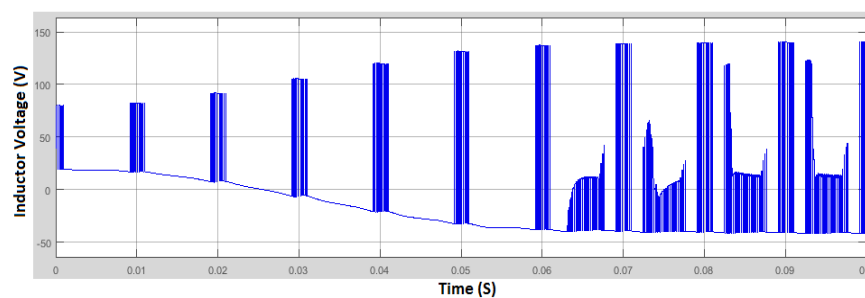


Figure 10. Voltage across the inductor (L1) of z-source network

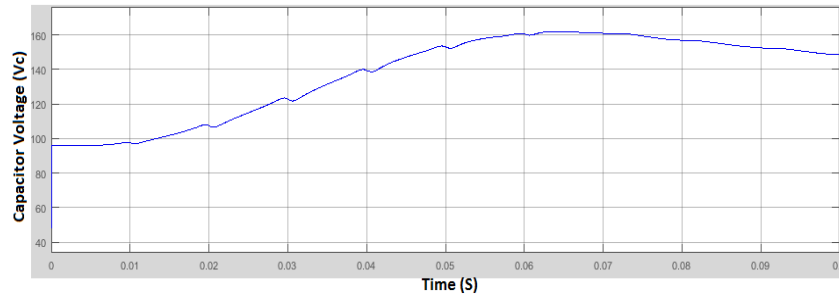


Figure 11. Voltage across the capacitor (C1) of z-source network

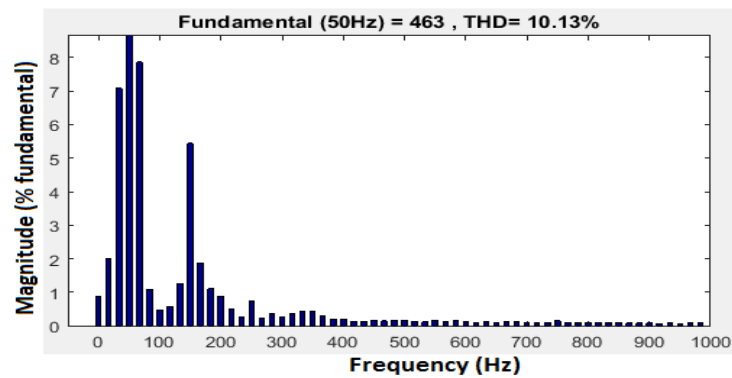


Figure 12. FFT analysis for output voltage of proposed scheme

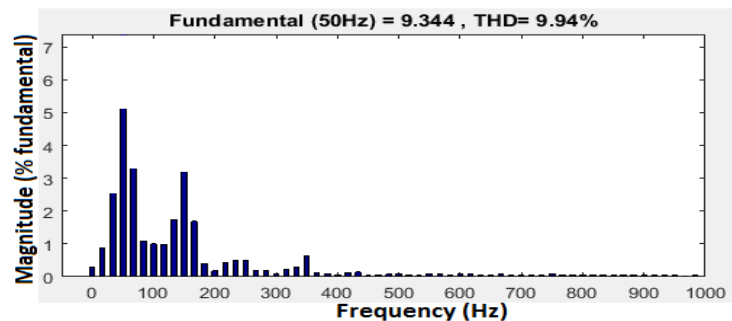


Figure 12. FFT analysis for output current of proposed scheme

In Figure 10 shows the voltage across the inductor (L1) of z-source network with value of 140V and Figure 11 shows the voltage across the capacitor (C1) of z-source network with maximum value of 162V. The harmonic analysis of output voltage and output current of 10.13% and 9.94% is shown in Figure 11 and Figure 12 respectively.

5. CONCLUSION

The projected scheme of 7-level z-source cascaded h-bridge inverter was simulated using matlab software, and it was assessment that the scheme efficiency and reliability was enhanced by situate the shoot through state condition by maximum boost control. The cascaded 7-level inverter has improved output voltage and controlled output current with reduced THD value. With help of MBC, the voltage stress across the power switches and improves the boost voltage gain with L-C combination of z-source network, which avoids the usage of conventional dc-dc boost converter. From the proposed system the THD of output voltage with 10.13% and for current with 9.94% which is less compare to traditional systems. It will comprehensive with 3D space vector modulation controller to minimize common mode voltage.

REFERENCES

- [1] F. Z. Peng, "Z-Source Inverter," *IEEE Transactions on the Industry Applications*, vol. 39, No. 2, pp. 504-510, March/April 2005.
- [2] J. Anderson and F. Z. Peng, "Four quasi Z source inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 2743-2749.
- [3] Li, Yuan, et al. "Modeling and control of quasi Z source inverter for distributed generation applications." *Industrial Electronics, IEEE Transactions on* 60.4 (2013): 1532-1541.
- [4] Peng, Fang Zheng, Miaosen Shen "Maximum boost control on the Z-source inverter." *IEEE Transactions on power electronics* 20.4 (2011): 833-838.
- [5] Effah, Francis Bofo, et al. "Space-vector-modulated three-level inverters with a single Z-source network." *Power Electronics, IEEE Transactions on* 28.6 (2013): 2806-2815.
- [6] Liu, Yushan, et al. "Overview of space vector modulations for three-phase Z-source/quasi-Z-source inverters." *Power Electronics, IEEE Transactions on* 29.4 (2014): 2098-2108.
- [7] Hemanthakumar, R., Raghavendrarajan, V., AjinSekhar, C.S., Sasikumar, M. "A novel hybrid negative half cycle biased modulation scheme for cascaded multilevel inverter", *International Journal of Power Electronics and Drive Systems*, vol 4, Issue 2, June 2014, Pages 204-211.
- [8] Bharatiraja, C., Raghun, Paliniamy, K.R.S. "Comparative analysis for different PWM techniques to reduce the common mode voltage in three-level neutral-point-clamped inverters for variable speed induction drives", *International Journal of Power Electronics and Drive Systems*, vol. 3, Issue 1, March 2013, Pages 105-116.
- [9] Gnana Prakash, M., Balamurugan, M, Umashankar, S. "A new multilevel inverter for reduced number of switches", *International Journal of Power Electronics and Drive Systems*, vol 5, Issue 1, September 2014, Pages 63- 70.
- [10] Alishah, R.S., Hosseini, S.H. "A new multilevel inverter structure for high-power applications using multi-carrier PWM switching strategy", *International Journal of Power Electronics and Drive Systems*, vol 6, Issue 2, 1 June 2015, Pages 318-325.
- [11] L. M. Tolbert, F. Z. Peng, and T. Habetler, Multilevel Converters for Large Electric drives. *IEEE Trans. Ind. Applicat.*, Jan./Feb. 2014. vol.35, pp. 36-44.
- [12] Poh Chiang Loh, Feng Gao, FredeBlaabjerg, and Sokweilim. Operational Analysis and Modulation Control of Three Level Z-Source Inverters with Enhanced Output Waveform Quality. *IEEE Transaction on Power Electronics*, July 2010. Vol.24, No.7.
- [13] SamirKouro, Pablo Lezana, Mauricio Angulo and José Rodríguez. Multicarrier PWM with Dc-Link Ripple Feed forward Compensation for Multilevel Inverters. *IEEE Transactions on Power Electronics*, Vol. 23, No.1, January 2010.
- [14] J. Prakash, Sarat Kumar Sahoo, K. R. Sugavanam. Design for Coordinated Control Scheme of Hybrid Resonant Boost Converter and Multi Level Inverter. *Indian Journal of Science and Technology*, 9(11), volume 9, Mar-2016.

BIOGRAPHIES OF AUTHORS



R. Palanisamy received B.E Degree in EEE from M. Kumarasamy engineering college (Anna University Coimbatore), Karur, Tamil Nadu, India in 2011 and received the M.Tech degree in Power Electronics and Drives from SRM University, Kattankulathur, Tamilnadu, India in 2013. And pursuing PhD degree in the area of Z source inverter with 3D-SVM. Presently working as Assistant Professor in the Department of Electrical Engineering, SRM University, Kattankulathur, and Chennai, India. His research interests include Power Electronics Multilevel inverters, Matrix converters, Various PWM Techniques and grid connected Photovoltaic system.



K. Vijayakumar received B.E degree in Electrical and Electronics Engineering and M.E degree in Power System Engineering both from Annamalai University, Tamil Nadu, India. & received P.hD in congestion Management in Deregulated Power systems from SRM University, Kattankulathur, Tamilnadu, India in 2013. His research interests include Power system: Deregulation, Modeling, Control and Operation, Optimization, FACTS, Power Quality. Presently working as Professor and Head of Department of Electrical & Electronics Engineering, SRM University, Kattankulathur, and Chennai, India.