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A PWM Strategies for Diode Assisted NPC-MLI to Obtain Maximum Voltage Gain for EV Application

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ABSTRACT

The projected diode assisted Neutral Point Diode Clamed (NPC-MLI) with the photovoltaic system produces a maximum voltage gain that is comparatively higher than those of other boost conversion techniques. This paper mainly explores vector selection approach pulse-width modulation (PWM) strategies for diode-assisted NPC-MLI to obtain a maximum voltage gain without compromising in waveform quality. To obtain a high voltage gain maximum utilization of dc-link voltage and stress on the power switches must be reduced. From the above issues in the diode assisted NPC-MLI leads to vector selection approach PWM technique to perform capacitive charging in parallel and discharging in series to obtain maximum voltage gain. The operation principle and the relationship of voltage gain versus voltage boost duty ratio and switching device voltage stress versus voltage gain are theoretically investigated in detail. Owing to better performance, diode-assisted NPC-MLI is more promising and competitive topology for wide range DC/AC power conversion in a renewable anergy application. Furthermore, theoretically investigated are validated via simulation and experimental results.

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1. INTRODUCTION

Solar energy, harnessed through solar cells, can be used extensively in various power electronic applications, such as power generation and distribution system. The most prominent advantage in these applications is the low dc source voltage supply and required high output ac voltage [2],[4]. The largest aid to the power grid will be based on the development of the photovoltaic generation system through which renewable energy is utilized. The main drawback of the existing solar photovoltaic panels is the wide range voltage drop and high investment cost [5]-[6]. Hence, there is a need to boost the low dc source voltage into a high constant ac voltage. Voltage source inverter is added to normalize the amplitude and frequency in order to obtain the necessary high ac voltage for power grid [7]. The initial cost can be minimized by decreasing the number of stages of inverter. Cuk and single ended primary inductor converter (SEPIC), which have both buck-boost conversion and bidirectional power processing [8]. For improved performance, the buck-boost converter is modulated by addition of an extension, where commutation count area is studied and improved efficiency is achieved [9].However, the switching devices used in the buck- boost circuit lead to large dc source current and high intermediate dc-link voltage when the boost duty ratio is extremely high [10]. Considering adding a power conversion stage, causing increase in system cost and reduction in efficiency, Peng [1] introduced impedance source inverter. Impedance source inverter consists of a unique impedance

network between the source and the main circuit to obtain both voltage buck and boost characteristics to overcome the limitations with voltage source inverter [13].

Shoot through mode is used to enhance the low ac output voltage. This circuit provides low- cost, reliable, and single-stage methodology for dc to ac power conversion when the voltage gain is low [12].This circuit incorporates an X-shaped diode-assisted capacitor network between the boost inductor and the inverter bridge. When S_1 is turned off, the two capacitors are connected in parallel through two forward-biased diodes and the transitional dc-link voltage V_i is equal to capacitor voltage. During this period, the three-phase voltage source inverter operates in null state and output ac voltage is zero. Sufficient utilization of intermediate dc- link voltage can improve the voltage transfer ratio and reduce the voltage rating of the capacitors. The Several PWM strategies are explained to obtain the maximum linear voltage gain as well as to minimize the voltage stress of the switching devices in theory [13]-[14]. Diode-assisted buck–boost VSI validates advantages in design cost and better performance in dc/ac power conversion for simultaneously much higher and wide range voltage regulation [15]. However, those methods are uses number of shoot through (ST) switching options and less bother on neutral point balancing.

Given that the neutral point balancing with minimal switching state usage was seldom investigated in the literature, this paper is demanding to cover the research gap.Within this context, in paper proposed the improved SVPWM schemes for Z-T-NPC-MLI with minimal ST state. The scheme exploits the redundancy switching vector option for both ST and regular switching, which good voltage profile and maintain the quarter symmetry and harmonic spectra.

2. EQUIVALENT CIRCUIT, VOLTAGE GAIN and VOLTAGE STRESS

Diode based buck-boost converter shown in the Figure 1 is having two operating modes based on the switching state of the switch S_1. For our convenience the capacitance and terminal voltage across the two capacitors C_1 and C_2 in the symmetrical X-shape network are assumed as same values.

$$C_1 = C_2, V_{C1} = V_{C2} = V_C \tag{1}$$

The Figure 2 shows the equivalent circuit for the diode based buck-boost converter when the switch S_1 is ON. In this time period the two diodes are reverse biased.

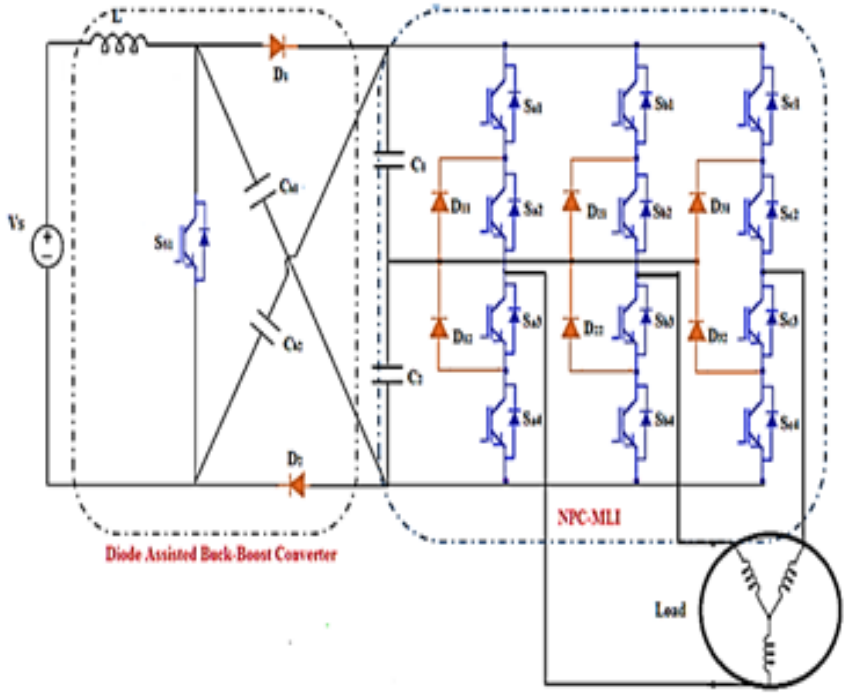

Figure 1. Circuit diagram of diode assisted buck-boost converter with NPC-MLI

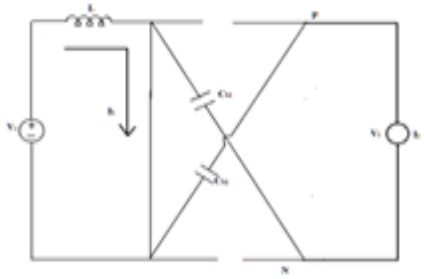

Figure 2. Equivalent circuit of diode assisted buck-boost converter during S_1 is ON

With this operation the inductor present in the circuit absorbs the energy from the dc source by maximizing the charging current and the dual capacitors are connected in series to feed the loads. The Equations during this time period are expressed as Equation.

$$V_L = V_S, V_{i(S_1=ON)} = V_{C1} + V_{C2} = 2V_C \tag{2}$$

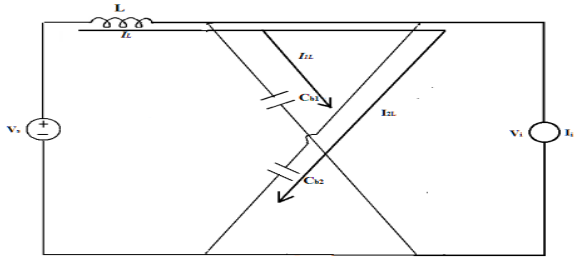

Figure 3. Equivalent circuit of diode assisted buck-boost converter during S_1 is OFF

The Figure 3 shows the equivalent circuit of diode based buck boost converter equivalent circuit when the switch S_1 is turned OFF. Then the two diodes in the circuit are forward biased the energy accumulated in the inductor is transferred to the two capacitors and both of the capacitors will be in parallel to supply the loads.

$$V_L = V_S - V_C . V_{i(S_1=OFF)} = V_{C1} = V_{C2} = V_C \tag{3}$$

The average voltage across inductor during one switching period in steady state is zero. From (2) and (3), the voltage of the inductor is

$$V_L = \frac{p_{on} T_s \cdot V_{in} + (1-p_{on}) T_s \cdot (V_s - V_c)}{T_s} \tag{4}$$

From the above equation, the voltage across the capacitor can be derived as

$$V_C = \frac{1}{1-p_{on}} V_s \tag{5}$$

Where V_s is the input supply voltage, p_{on} is the on-state duty ratio of the switch S_1, Ts is switching time period. In the similar way the average intermediate dc-link voltage across the converter can be written as follows

$$V_i = \frac{p_{on} \cdot T_s \cdot 2V_c + (1-p_{on}) T_s \cdot V_c}{T_s} = (1 + P_{on}) V_S \tag{6}$$

The switching stress across the two diodes and switch present in front of the boost circuit is equal to the voltage across the capacitor V_c and similarly the voltage stress across theswitchingdevices in the NPC-MLI is the maximum dc-link voltage of the inverter.

The bridge voltage which is twice the capacitor voltage $2V_C$

$$V_{Sf} = V_C, V_{Si} = \widehat{v_i} = 2V_C \tag{7}$$

The voltage transfer ratio of the diode based buck-boost NPC-MLI is defined as

$$G = \frac{\widehat{v_i}}{\frac{V_S}{2}} = \frac{\widehat{2V_{ac}}}{V_{dc}} \tag{8}$$

Where v_{ac} is the peak value of the output phase voltage

3. PROPOSED PULSE WIDTH MODULATION STRATEGIES

The space vector diagram for a 3-phase 3-level VSI is a hexagon, consisting of six sectors as shown in Figure 4, and each sector consists of four sub-triangles. Each inverter leg can have three switching states, which results in 27 voltage vectors. No power is delivered to the load for the switching states (111), (000), and (-1-1-1), which is referred to as the null voltage vector (NV). Hence, the 27 possible voltage vectors are classified as 18 effective voltage vectors and 1 null vector. The non-zero voltage vectors can have three phase voltage levels, which are 2/3Vs, $V_s/\sqrt{3}$, and V_s /3. Each voltage level corresponds to the vertex of the large hexagon called the large vector (LV), that on the middle side point of the large hexagon called the medium vector (MV) and that on the vertex of the small (inside) hexagon called the small vector (SV), respectively. The six LVs forms the vertices of the hexagon and the three NVs are located at the origin.For theoretical analysis a new concept introduced which is called as the natural point potential.

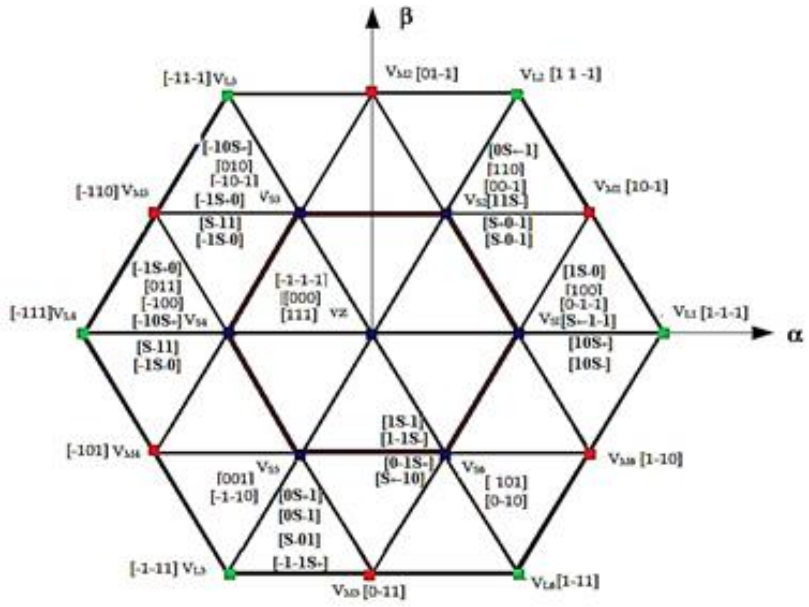

Figure 4. Space vector diagram for the proposed technique

In the stationary coordinate, a space vector of constant magnitude $|V_r|$ and angular velocity ω_r is introduced to represent the three-phase balanced voltage.

$$V_r = |V_r|e^{j\theta r} = \frac{2}{3}[V_{ao} + V_{bo}e^{j\frac{2}{3}\Pi} + V_{co}e^{-j\frac{2}{3}\Pi}] \tag{9}$$

The factor 2/3 includes in the amplitude of the voltage vector equals the peak value of the corresponding output phase voltage.$\theta_r = \omega_r t$ is the phase angle of reference vector, $\omega_r = 2\pi fN$ We know that,

$$V_{ON} = \frac{1}{3}(V_{aN} + V_{bN} + V_{cN}) \tag{10}$$

In the above equations V_{ao}, V_{bo}, V_{co} are the line to neutral voltages, V_{aN}, V_{bN}, V_{cN} are the line to zero voltages, V_{oN} is the neutral to zero voltage

$$V_{ON} = \frac{1}{3}V_c, V_{ao} = \frac{2}{3}V_c, V_{co} = V_{bo} = -\frac{1}{3}V_c \quad (11)$$

$$V_1 = |V_1| = \frac{2}{3}V_c \quad (12)$$

$$|V_1| = |V_3| = |V_5| = |V_7| = |V_9| = |V_{11}| = \frac{2}{3}V_c \quad (13)$$

$$|V_2| = |V_4| = |V_6| = |V_8| = |V_{10}| = |V_{12}| = \frac{4}{3}V_c \quad (14)$$

Based on the above PWM strategy there is a necessity for the new improved PWM strategy to take the full advantage on the small voltage vectors. The below figure shows the sequences of the voltage vectors in the first sextant compared with the existing PWM strategies. The active switching vectors are commanded during the both intervals when S_1 is ON and S_2 is OFF with one switching time period (T_s) to synthesize the reference wave vector (V_r). The vectors are symmetrically distributed during two switching time periods ($2T_s$) by inserting the interval of S_1=ON symmetrically in centre. If the switch S_1 turns ON and OFF once in two switching periods the switching loss of power devices in front of the boost circuit can be reduced to half. In order to minimize the half-switching frequency harmonics distortion, the second improved PWM strategy is presented to ensure a symmetrical placement of switching states in one switching time period. The main feature of this modulation strategy is that S_1 turns ON and OFF once with S_1=ON interval symmetrically inserted at the centre of one switching period T_s. There will be an additional switching state for small vector V_1. With this introduces an additional switching state in phase leg of the inverter bridge during S_1=OFF. With the same design approach the switching states in other sextants can be obtained. The modulation index of the inverter M_t is limited by the on-state duty ratio of the switching device S_1 of the front boost circuit.

$$G = \frac{2M_i}{1-p_{on}} (0 \le M_i \le P_{ON}) \quad (15)$$

The voltage stress across the switching devices in front of the boost circuit V_{sf} and that value is same as the capacitor voltage V_c

$$V_{Sf} = \frac{1}{1-p_{on}}V_S, V_{Si} = \frac{2}{1-p_{on}}V_S \quad (16)$$

For the traditional carrier wave based SPWM with third harmonic injection or SVM, dc voltage utilization of the inverter bridge is increased and the maximum modulation index of M_t=1.15 p_{on}.

$$G_{max} = \frac{4}{\sqrt{3}}\frac{p_{on}}{1-p_{on}} (M_i = \frac{2}{\sqrt{3}}P_{on}) \quad (17)$$

$$V_{sf} = \frac{4+\sqrt{3}G_{max}}{4}V_s, V_{Si} = \frac{4+\sqrt{3}G_{max}}{2}V_s \quad (18)$$

3.1. Shoot Through Mode

The shoot defined as the creation of the short circuit path to the inductor. The shoot through in NPC-MLI can be achieved using the triggering of all switches at a time. Three types of shoot through are available they are

a. In full shoot through state the switches the switches 1 and 4 will triggered simultaneously
b. In Top Shoot through state the upper half switches are triggered
c. In bottom Shoot through state the lower half of the switches are triggered

The three above mentioned shoot through can be observed from the following waveforms, and how the operation is being achieved

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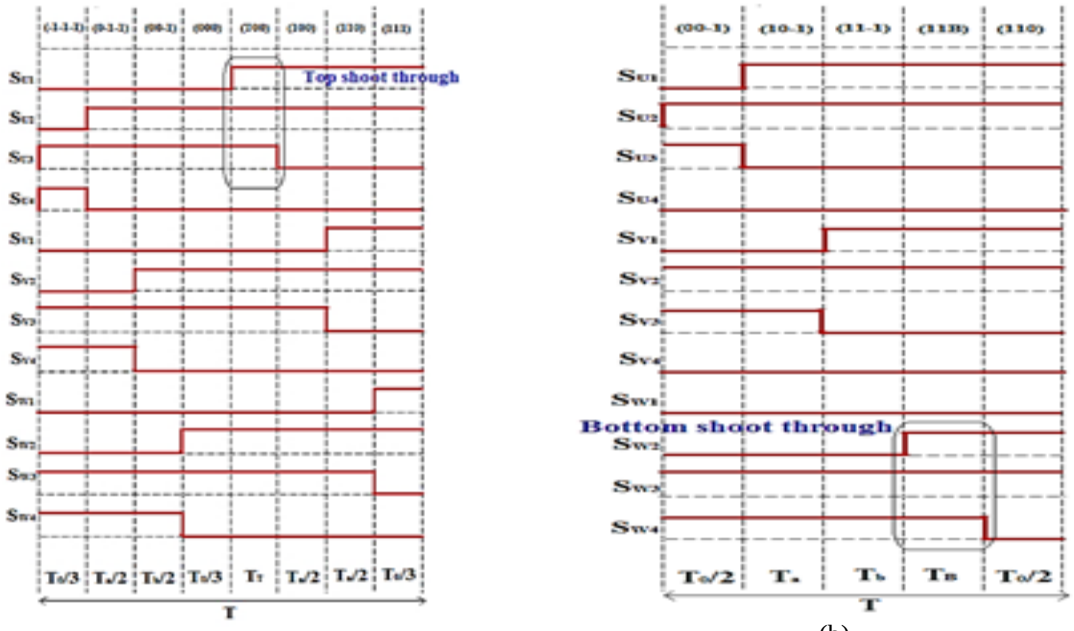

Figure 5. Switching operation of NPC-MLI (a) Top shoot through (b) Bottom shoot through

4. SIMULATION STUDY

Inverter is operated in the linear modulation range with the maximum modulation index of 0.907. The values of capacitance and inductance in the Z source network are 640 micro Farad and 10 mH respectively. The internal resistance of IGBT is considered as 1 mΩ and snubber resistance is 10 micro Ohm. Two equal capacitors are considered across the supply to split the supply voltage in to two equal half and to create a neutral point. In this Simulation circuit the source voltage is considered as 100 V DC and the output of the NPC-MLI is 180 V AC (maximum). Line voltage and THD for the modulation index (M_a) of 0.7 and 0.9 for the NPC-MLI is shown in the Figure 6 and Figure 7.

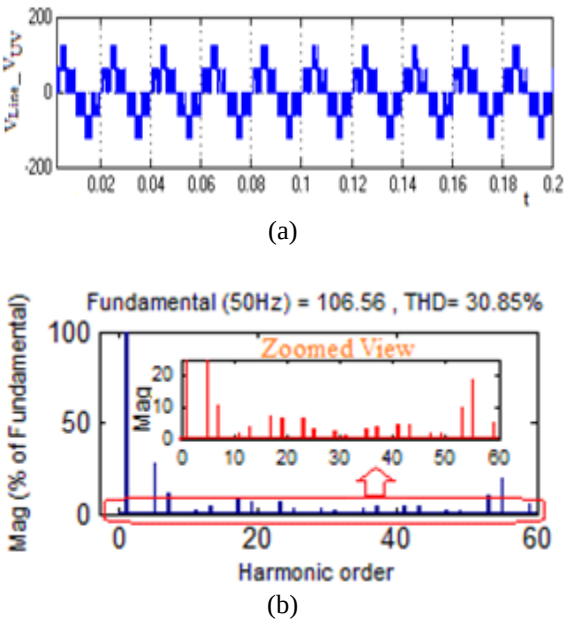

Figure 6. output performance characteristics for M_a=0.7 (a) Line voltage (b) THD spectra

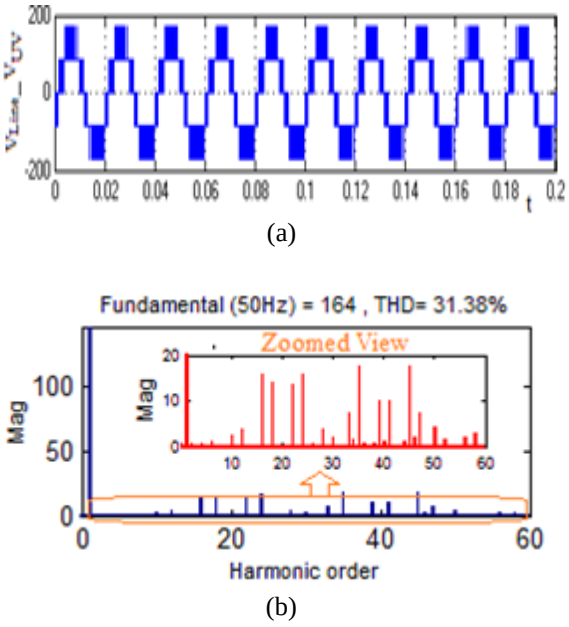

Figure 7. Output performance characteristics for M_a=0.9 (a) Line voltage (b) THD spectra

5. EXPERIMENTAL STUDY

The IM is driven by a Z-source NPC-MLI with 100V DC-link and two 100µF front-end DC-link capacitors. Z-source Network having two 10mH inductors and two 3400uF capacitors.FGA15N120ANTD and CT60AM 18F which has an in-built structure of IGBT and anti-parallel diodes is used in each phase leg which provides the basic structure of NPC Type-MLI. The gate pulses for the top and bottom shoot through of each leg are shown in the Figures 8. The bottom shoot through the switches 2, 3 and 4 are triggered simultaneously as shown in the Figure 9. The experimental results for entire modulation region are shown below for m_a=0.8. Here the line voltage and THD spectra is witnessed as 167V and 32.89% respectively. Based on the simulation and excremental results, it could understand that the proposed SVM for Z NPC-MLI is produced more line voltage and less THD compare to the previous work [12]. In addition the scheme uses less number of ST, which reducing the switching losses on the inverter.Here could understand that the conduction losses are low throughout the operating value of M_a, which lead the best efficiency of Z-T-NPC-MLI

Figure 8. Gate pulses of one leg in top shoot through

Figure 9. Gate pulses of one leg in bottom shoot through

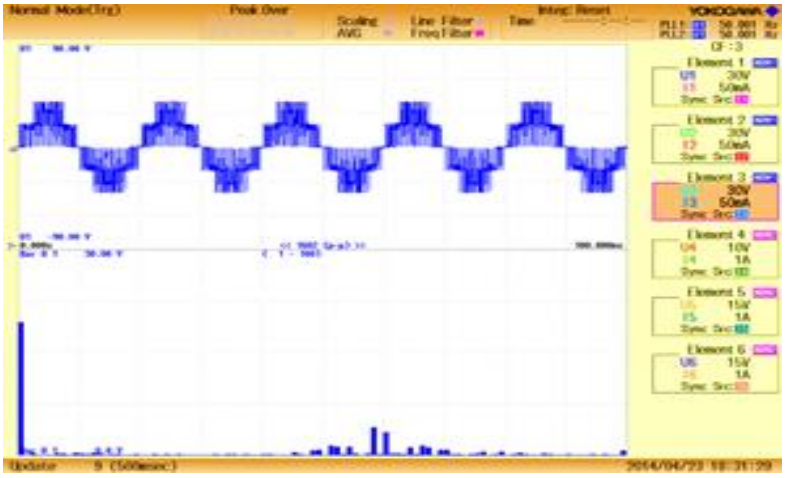

Figure 10. Experimental Line voltage (30v/div) THD spectra for M_a=9.0

6. CONCLUSION

This paper analyses the drawbacks of the existing PWM strategies for the diode assisted buck-boost VSI and then proposed new improved PWM strategy. The voltage gain and switching devise stress are improved compared to the existing PWM strategy. Simulation and experimental results are provided in order

to validate the theoretical results. The advantages are high voltage and the wide range of voltage regulation, because of these advantages this topology is using for a wide range of power conversion in renewable energy applications.

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