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Three-Phase Three-Level Soft Switching Dc-Dc Converter for Industrial Applications

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ABSTRACT

In high power DC applications, the single-phase DC-DC converter will face large voltage and current stress in each control switch and thereby the power handling capacity is less. To overcome this problem, three-phase DC-DC converter is used and it is suitable for high power applications with reduced number of switches as compared with the conventional topologies. The asymmetrical duty cycle control is considered to operate the switches under soft switching and hence the switching losses are reduced. The transformer leakage inductances are used along with junction capacitances in order to form resonance and hence ZVS commutation is possible in a wider load range. The modified phase shift control method is used for the proposed converter.The operational modes and design equations of the proposed converter have been observed. The simulation is carried out with a load of 1000W for validating the proposed work.

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1. INTRODUCTION

The controlled switches such as IGBTs and MOSFETs are having many advantages in terms of speed of response and system size but these switches are unable to operate at high voltages. The advantages of these smaller size, faster responses, different multi level topologies are been proposed [5]-[11] in order to reduce the voltage across each switching device. The different multi level topologies are flying capacitor, diode clamped and cascaded converters are providing for division of voltage across the switching devices [9]. During the switching instants, the losses in the switching converter will become increased by increasing the switching frequency. The soft switching converters are proposed in order to reduce the switching losses.

A Three-Level Full-Bridge Zero-Voltage Zero-Current Switching Converter with a Simplified Switching Scheme [4] is having eight control switches for generating three levels. The size of the filter elements in this paper is high and more number of switches is required for three level operation, hence the cost is high. The Three-Level Combined DC–DC Converter without Added Primary Clamping Devices contains six control switches for three level dc-dc converter operation [1]-[3].

The multi level inverter [9] is used to produce the stress across each switch. But this converter is not operating under soft switching scheme. Hence, the switching losses are high and efficiency becomes poor. To overcome all these problems, the proposed five level full bridge zero voltage zero current switching dc-dc converter is suitable.

The three level dc-dc topologies are well suited for high input voltage applications where the voltage across power switches are only the half of the input voltage. To reduce the voltage across power switches further, the three- phase three - level dc-dc topologies were proposed. But the drawback of these topologies are asymmetrical duty cycle, so the wider soft switching mechanism is not possible [12]-[13].

To simplify further, the modified dc-dc topology [14] is used and it is having the advantages of three-phase three-level features and also effective utilization of transformer and reduced the filter requirement. But this topology is controlled by symmetrical duty cycle and hence there is not a guarantee to operate switches under ZVS.

To overcome all these problems, proposed modified asymmetrical duty cycle controlled three-phase three-level dc-dc topology is used and it is having the advantages of existing topologies. In this topology, all the control switches are operating under soft switching. So, the overall efficiency of the converter will get increased and also the size of filter will get reduced to a greater value.

2. THREE-PHASE THREE-LEVEL SOFT SWITCHING DC-DC CONVERTER

The arrangement of three-phase three-level dc-dc soft switching converter is shown in Figure 1. The switches S_1-S_6 are to be triggered in such a way that the converter generates three line voltages and they are displaced by 120^o. The three-phase delta-star step down transformer is used to make an electrical isolation between source and dc load. The transformer leakage inductances L_{l1}, L_{l2} and L_{l3} are used along with junction capacitances C_1-C_6 in order to form resonance and hence ZVS commutation is possible in a wider load range. The rectifying diodes D_{R1}-D_{R6} are used to convert step down three-phase ac voltage into a rectifying dc voltage. The filter elements L_f and C_f are used to make the rectified dc voltage into pure dc voltage. There will be an equal delay is provided between the control switches S_1, S_4 and S_3, S_6 and S_2, S_5 in order to provide soft switching. The I_{p1}, I_{p2}, I_{p3} and V_{p1}, V_{p2}, V_{p3} are the primary currents and voltages of transformers 1, 2 and 3 respectively.

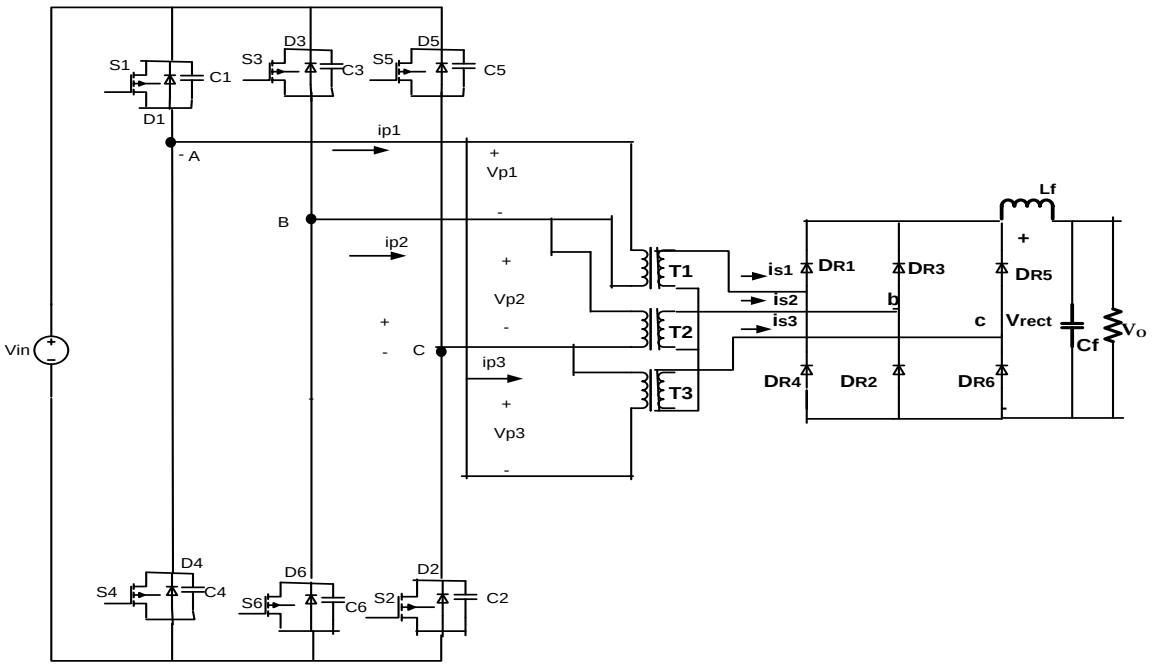

Figure.1. ZVS DC-DC Full bridge converter

3. OPERATION MODES

The operational waveform of the proposed dc-dc converter is shown in Figure 2. The various operating modes of the five level converter are as follows. The Figures of 3(a) to 3(k) show the operational modes of the ZVS DC-DC Full bridge converter. The following analysis is made based on the assumption that the blocking capacitors are large enough to act as a constant voltage source.

3.1. Operational Mode 0: $t \leq t_0$

Before time $t= t_0$, the switches S_1, S_5 and S_6 are operating then the primary winding of transformer 1 receiving a positive line voltage of V_{AB} and the primary winding of transformer 3 receiving a negative line voltage of V_{CA} and primary winding of transformer 3 does not receive any line voltage with respect to

currents I_{p1}, I_{p2} and I_{p3}. The rectifying diodes D_{R1} and D_{R2} are operating in order to supply continuous current to load and it is shown in Figure 3(a).

Vpa =Vdc Vpb = 0 Vpc = - Vdc

$$Vrec = Vsa - Vsc = k\,(Vdc + Vdc) = 2\,k\,Vdc \quad (1)$$

Where 'k' is the secondary to primary turns ratio of a transformer.

3.2. Operational Mode 1: $t0 \le t \le t_1$

At time t= t_0, the switch S_5 is turned off under ZVS. So, the capacitance C_5 starts charging where as the capacitance C_2 starts discharging with respect to currents in the circuit. Before time t=t_1, the capacitor C_2 is fully discharged to zero and the corresponding body diode of switch S_2 i.e, diode D_2 is on. Therefore the switch S_2 is ready to turn on under ZVS. The transformers 1 and 2 are operating along with rectifying diodes D_{R1} and D_{R2} in order to supply current to load and it is shown in Figure 3(b)

$$Vc5(t) = \frac{1}{Cp} k\, Io(t - to) \quad (2)$$

$$Vc2(t) = Vdc - \left(\frac{1}{Cp} k.Io(t - to)\right) \quad (3)$$

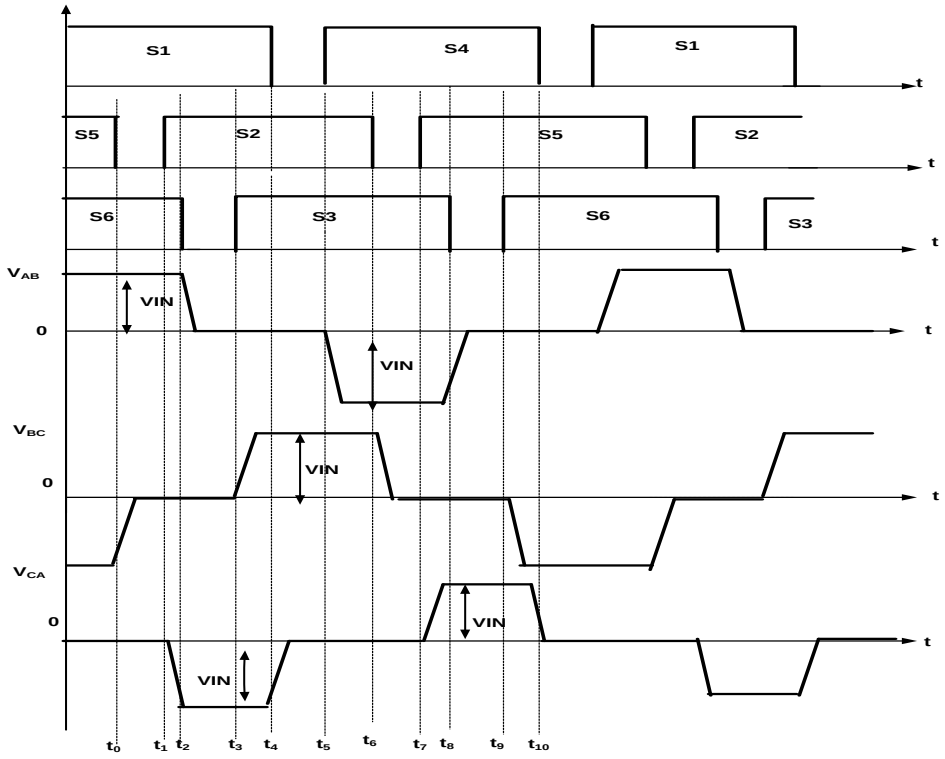

Figure 2. Operation waveforms of three-phase three-level dc-dc converter

3.3. Operational Mode 2: $t_1 \le t < t_2$

At time t=t1, the switch S2 is turned on under ZVS. The switches S1, S2 and S6 are operating then the primary winding of transformer 1 receiving a positive line voltage of V_{AB} and the primary winding of transformer 3 receiving a negative line voltage of V_{CA} and primary winding of transformer 3 does not receive any line voltage with respect to currents Ip1, I_{p2} and I_{p3}. The rectifying diodes D_{R1} and D_{R2} are operating in order to supply continuous current to load and it is shown in Figure 3(c).

3.4. Operation Mode 3: $t_2 \leq t < t_3$

At time t=t2, the switch S_6 is turned off under ZVS. So, the capacitance C_6 starts charging where as the capacitance C_3 starts discharging with respect to currents in the circuit. Before time t=t_3, the capacitor C_3 is fully discharged to zero and the corresponding body diode of switch S_3 i.e, diode D_3 is on. Therefore the switch S_3 is ready to turn on under ZVS. The transformers 1 and 3 are operating along with rectifying diodes D_{R1} and D_{R6} in order to supply current to load and it is shown in Figure 3(d).

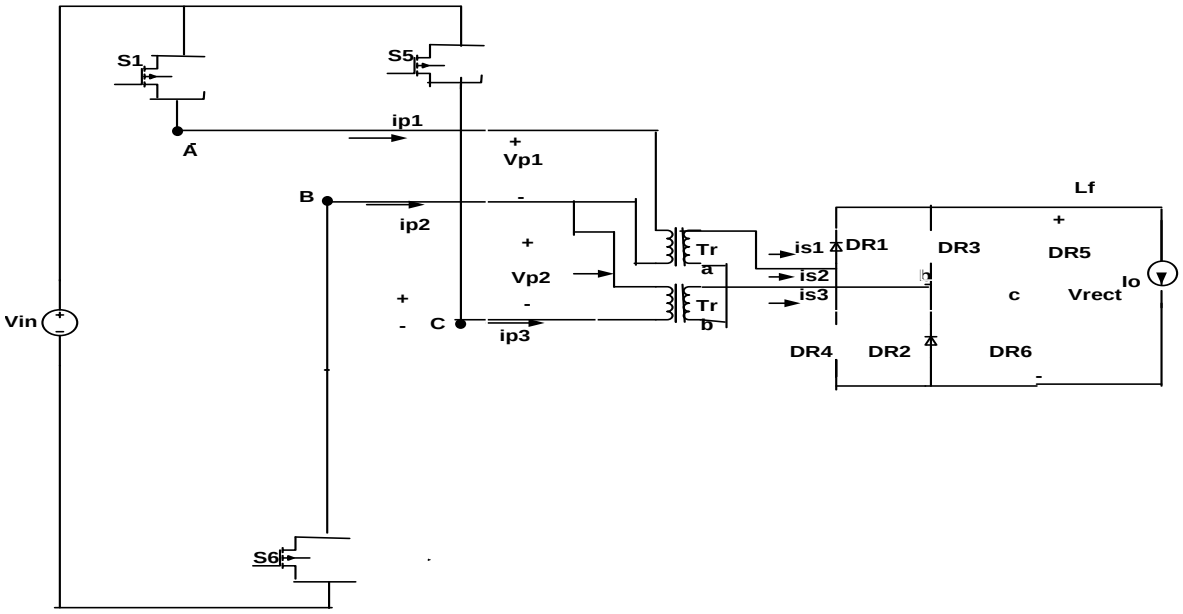

Figure 3(a). Operation mode0($t \leq t_0$)of the proposed converter

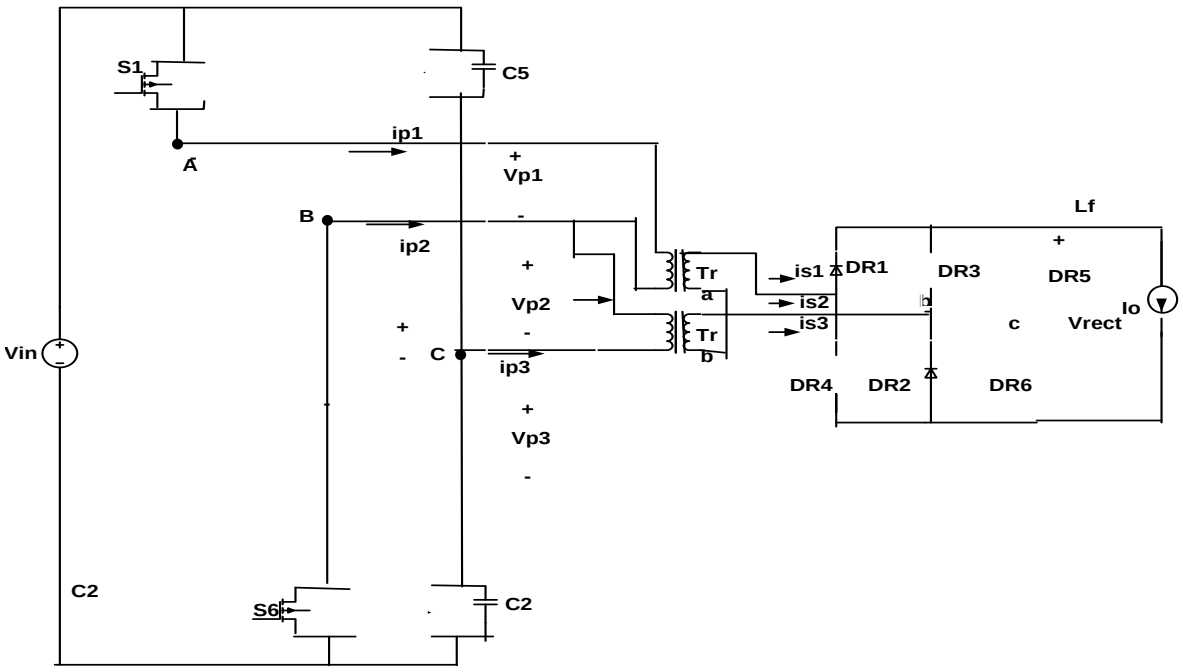

Figure 3(b). Operation mode1($t_0 \leq t \leq t_1$)of the proposed converter

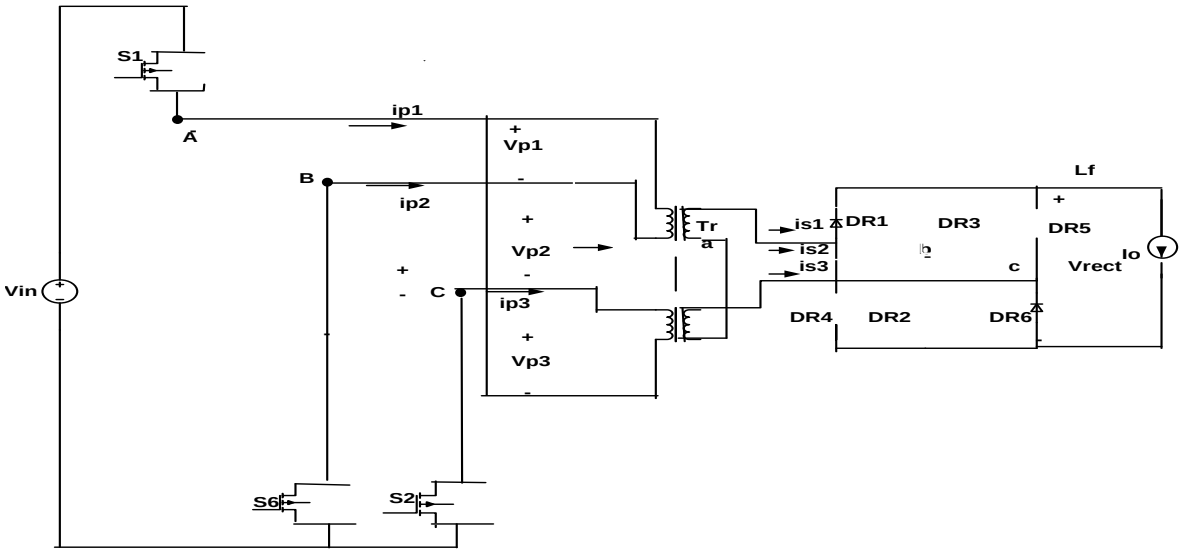

Figure 3(c). Operation mode2($t_1 \leq t \leq t_2$)of the proposed converter

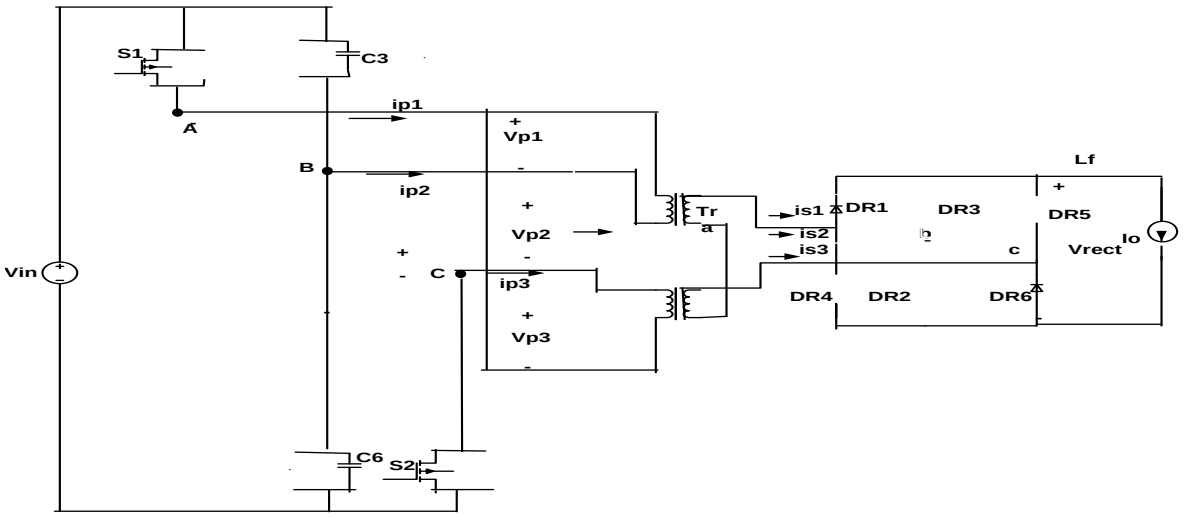

Figure 3(d). Operation mode 3($t_2 \leq t \leq t_3$)of the proposed converter

$$\mathrm{Vc3(t)} = Vdc - \frac{1}{2}k.Io.Zr.\sin[\omega r(t - \mathrm{t2})] \quad (4)$$

$$\mathrm{Vc3(t)} = Vdc - \frac{1}{2}k.Io.Zr.\sin[\omega r(t - \mathrm{t2})] \quad (5$$

3.5. Operation Mode 4: $t_3 \leq t < t_4$

At time t=t3, the switch S3 is turned on under ZVS. The switches S1, S2 and S3 are operating then the primary winding of transformer 2 receiving a positive line voltage of V_{BC} and the primary winding of transformer 3 receiving a negative line voltage of V_{CA} and primary winding of transformer 1 does not receive any line voltage with respect to currents Ip1, I_{p2} and I_{p3}. The rectifying diodes D_{R3} and D_{R6} are operating in order to supply continuous current to load and it is shown in Figure 3(e).

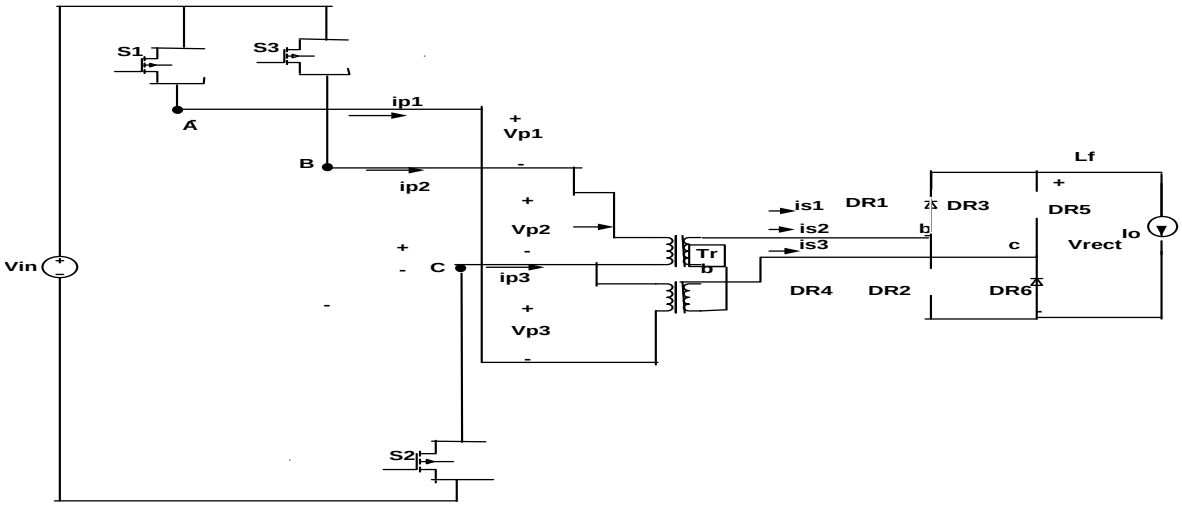

Figure 3(e). Operation mode4($t_3 \leq t \leq t_4$)of the proposed converter

3.6. Operation Mode 5: $t_4 \leq t < t_5$

At time t=t4, the switch S_1 is turned off under ZVS. So, the capacitance C_1 starts charging where as the capacitance C_4 starts discharging with respect to currents in the circuit. Before time $t=t_5$, the capacitor C_4 is fully discharged to zero and the corresponding body diode of switch S_4 i.e, diode D_4 is on. Therefore the switch S_4 is ready to turn on under ZVS. The transformers 2 and 3 are operating along with rectifying diodes D_{R3} and D_{R6} in order to supply current to load and it is shown in Figure 3(f).

$$Vc1(t) = \frac{1}{Cp} k\ Io(t - t4) \tag{6}$$

$$Vc4(t) = Vdc - \left(\frac{1}{Cp} k.Io(t - t4)\right) \tag{7}$$

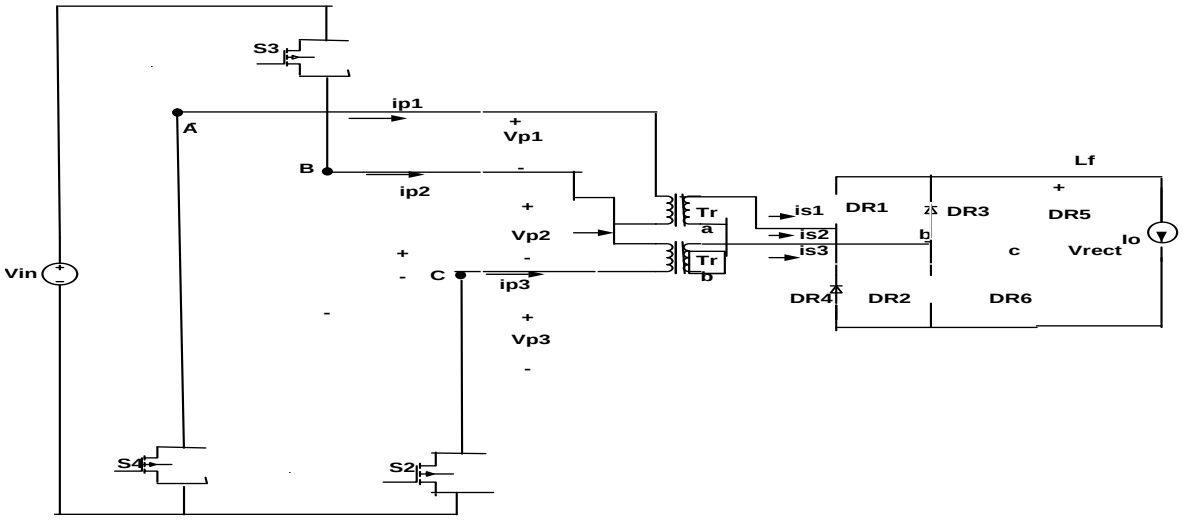

Figure 3(g). Operation mode6($t_5 \leq t \leq t_6$)of the proposed converter

3.6. Operation Mode 7: $t_6 \leq t < t_7$

At time t = t6, the switch S_2 is turned off under ZVS. So, the capacitance C_2 starts charging where as the capacitance C_5starts discharging with respect to currents in the circuit. Before time $t=t_5$, the capacitor C_5

is fully discharged to zero and the corresponding body diode of switch S_5 i.e, diode D_5 is on. Therefore the switch S_5 is ready to turn on under ZVS. The transformers 1 and 2 are operating along with rectifying diodes D_{R3} and D_{R4} in order to supply current to load and it is shown in Figure 3(h).

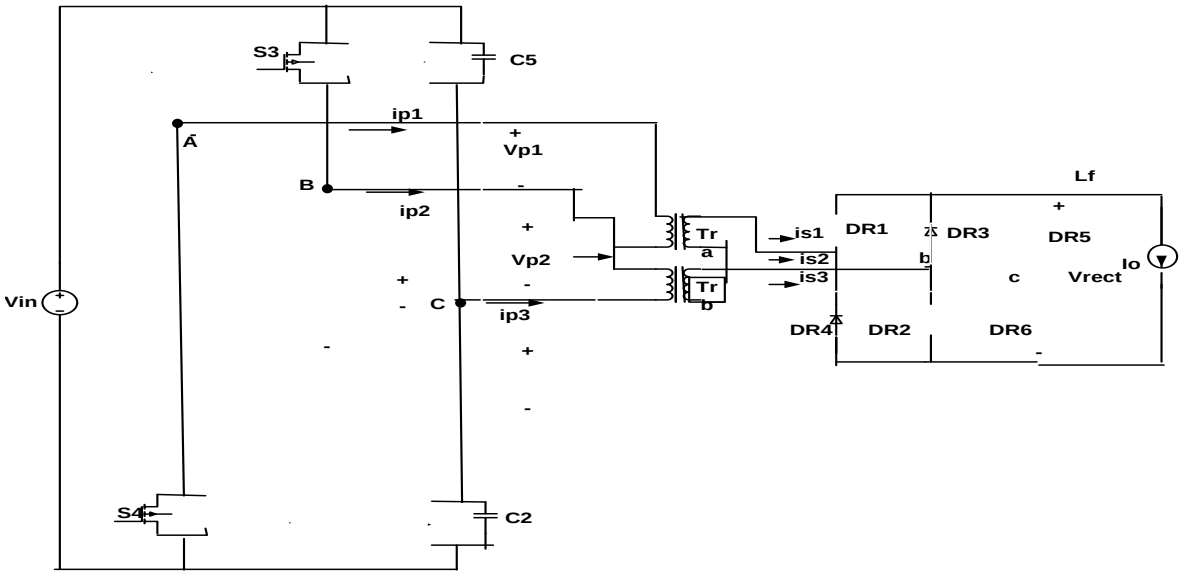

Figure 3(h). Operation mode7($t_6 \leq t \leq t_7$) of the proposed converter

$$\text{Vc5(t)} = Vdc - \frac{1}{2}k.Io.Zr.\sin[\omega r(t - \text{t6})] \quad (8)$$

$$\text{Vc2(t)} = \frac{1}{2}k.Io.Zr.\sin[\omega r(t - \text{t6})] \quad (9)$$

3.7. Operation Mode 8: $t_7 \leq t < t_8$

At time t=t7, the switch S5 is turned on under ZVS. The switches S3, S4 and S5 are operating then the primary winding of transformer 1 receiving a negative line voltage of V_{AB} and the primary winding of transformer 3 receiving a positive line voltage of V_{CA} and primary winding of transformer 2 does not receive any line voltage with respect to currents Ip1, I_{p2} and I_{p3}. The rectifying diodes D_{R5} and D_{R4} are operating in order to supply continuous current to load and it is shown in Figure 3(i).

3.8. Operation Mode 9: $t_8 \leq t < t_9$

At time t=t8, the switch S_3 is turned off under ZVS. So, the capacitance C_3 starts charging where as the capacitance C_6 starts discharging with respect to currents in the circuit. Before time t=t_9, the capacitor C_6 is fully discharged to zero and the corresponding body diode of switch S_6 i.e, diode D_6 is on. Therefore the switch S_6 is ready to turn on under ZVS. The transformers 1 and 2 are operating along with rectifying diodes D_{R6} and D_{R4} in order to supply current to load and it is shown in Figure 3(j).

$$\text{Vc3(t)} = Vdc - \frac{1}{2}k.Io.Zr.\sin[\omega r(t - \text{t8})] \quad (10)$$

$$\text{Vc6(t)} = \frac{1}{2}k.Io.Zr.\sin[\omega r(t - \text{t8})] \quad (11)$$

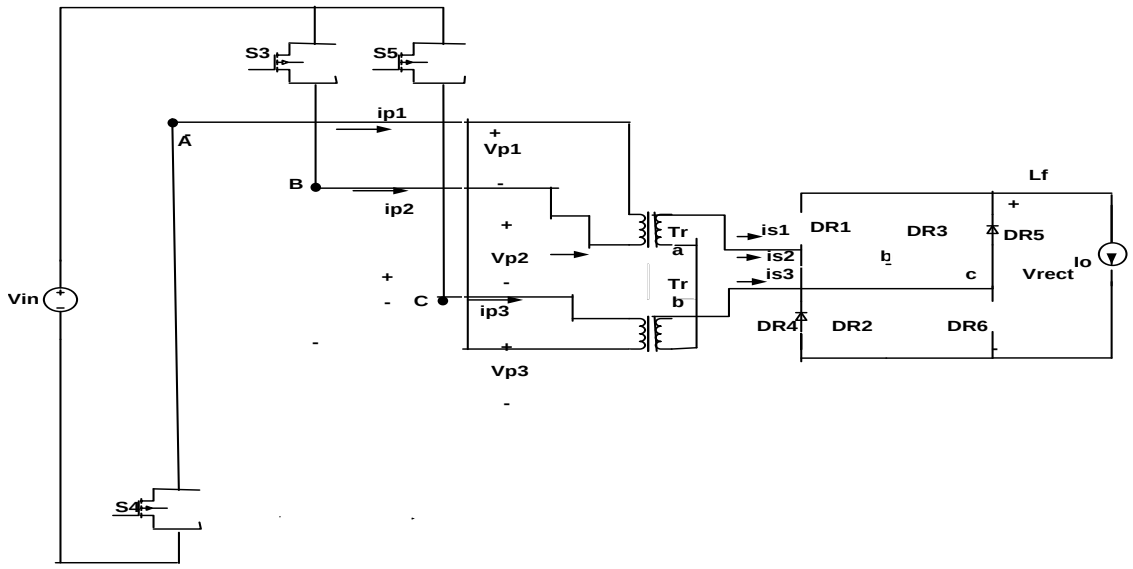

Figure 3(i). Operation mode 8($t_7 \leq t \leq t_8$) of the proposed converter

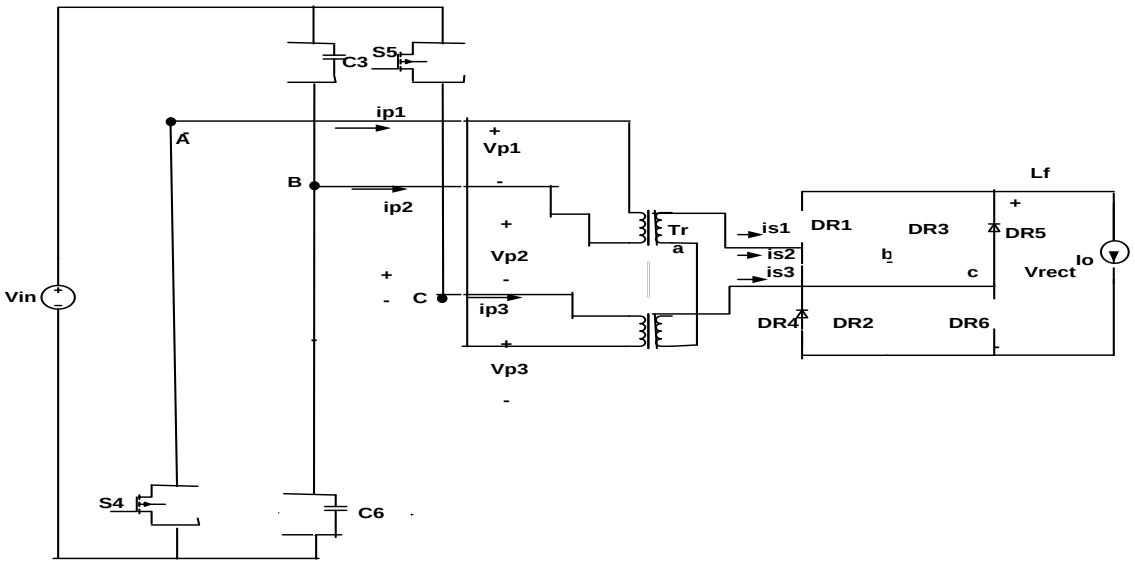

Figure 3(j). Operation mode 9($t_8 \leq t \leq t_9$) of the proposed converter

3.9. Operation Mode 10: $t_9 \leq t < t_{10}$

At time t=t9, the switch S6 is turned on under ZVS. The switches S4, S5 and S6 are operating then the primary winding of transformer 2 receiving a negative line voltage of V_{BC} and the primary winding of transformer 3 receiving a positive line voltage of V_{CA} and primary winding of transformer 1 does not receive any line voltage with respect to currents Ip1, I_{p2} and I_{p3}. The rectifying diodes D_{R5} and D_{R2} are operating in order to supply continuous current to load and it is shown in Figure 3(k).

4. SIMULATION RESULTS OF THREE-PHASE THREE-LEVEL DC-DC CONVERTER

The parameters of the proposed converter are shown in the table I. The dead band is created between the signals $S_1$and S_4, $S_2$and S_5 and $S_6$and S_3 to achieve ZVS condition. ZVS is accomplished when primary current discharges the parallel capacitors across the leading switches during dead band time.

$$I_{p0,min} = C_p * \frac{V_{dc}}{t_{dead}} \quad (12)$$

Figure 4 shows the transformer primary voltages of the converter circuit. If switches S1, S6 are in conduction then the primary winding of transformer 1 receiving positive line voltage VAB and similarly if the switches S3 and S4 are in conduction then the primary winding of transformer 1 receiving negative line voltage VAB. In similar manner, the other two primary windings of transformers 2 and 3 receiving line voltages VBC and VCA with the help of switches S2 and S3 for positive VBC and the switches S5 and S6 for negative VBC of transformer 2 and similarly the switches S4 and S5 for positive VAC and switches S1 and S2 for negative VAC of transformer 3 respectively.

Figure 4(a) shows the gate pulse, voltage across and current passing through switch S3.If the switch S3 is on at time t=11.38msec, the voltage across the switch is zero before time t=11.38msec If the switch S3 is off at time t=11.86msec, the voltage across the switch is reached zero before time t=11.86msec. So, it indicates that the switch S3 is operating under ZVS condition.

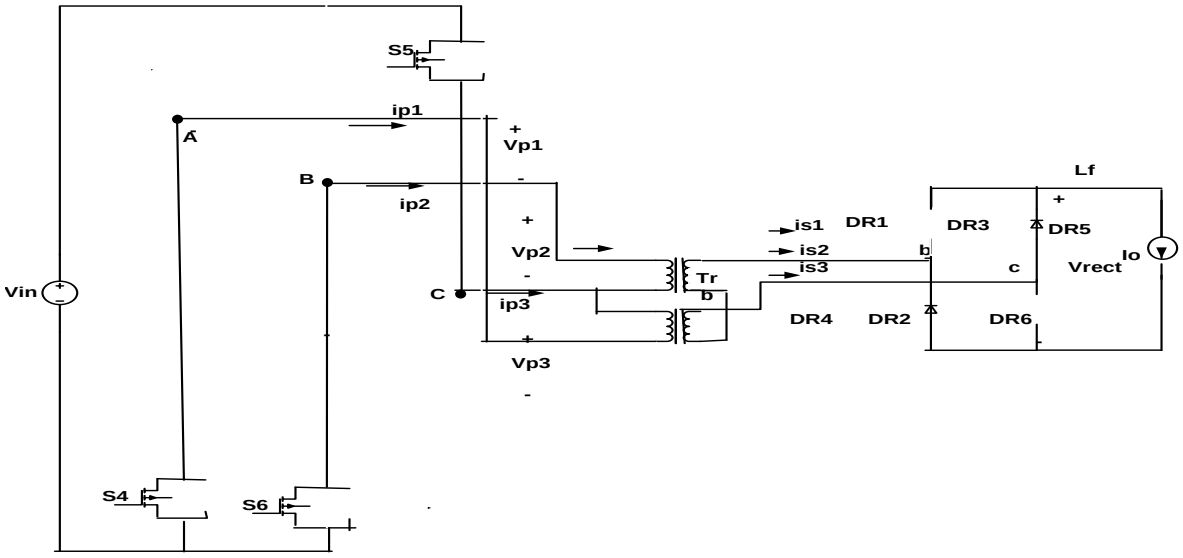

Figure 3(k). Operation mode 10($t_9 \leq t \leq t_{10}$) of the proposed converter

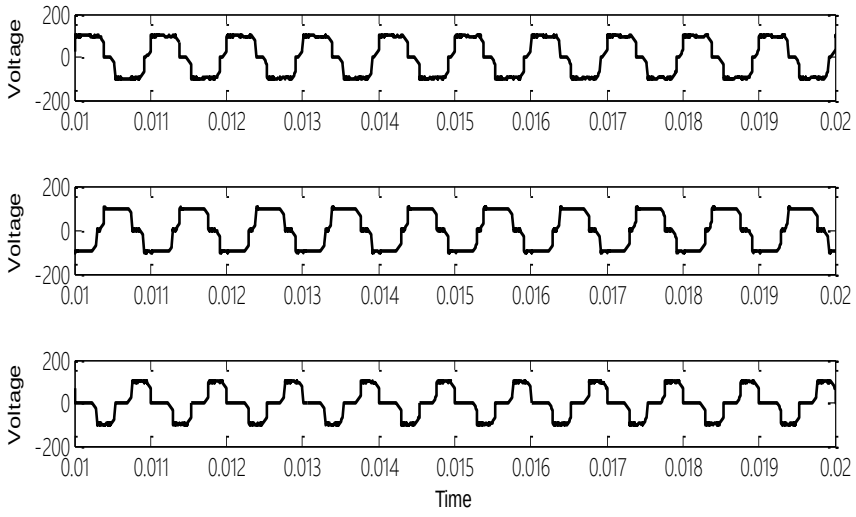

Figure 4. Transformer primary voltages

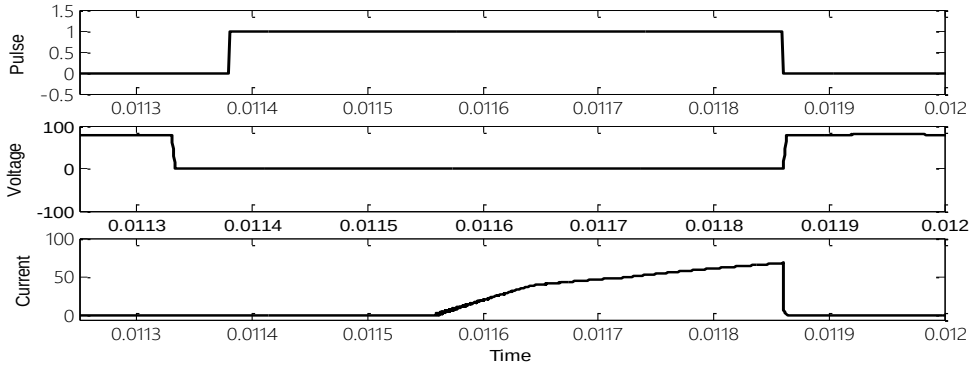

Figure 4(a). Gate pulse, Voltage and current of switch S3

5. CONCLUSION

This paper proposed a modified asymmetrical duty cycle control three-phase three-level dc-dc converter in which all the main switches are operating under soft switching. Hence, the switching losses are reduced. The leakage inductances of the transformers and junction capacitances are used to develop the resonance condition and hence ZVS commutation is possible in the switches with wider load range. The control signals for the proposed converter was generating from field programmable gate array. The proposed work has been implemented and it was verified through simulation and experimentation. Hence, there is scope for developing soft switching mechanism for various three-phase multi level topologies. The proposed topology has been suitable for high power applications.

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