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Cascaded Symmetric Multilevel Inverter with Reduced Number of Controlled Switches

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ABSTRACT

Multilevel inverters have become popular among high power converters for the past few years due to their high quality output waveform and low total harmonic distortions (THD). In addition, the filter size also reduces significantly to achieve a pure sine wave output. Cascaded H-Bridge topology has been recognized as the most promising among various classical topologies for multi-level inverters on the basis of its modular form and ease of design, troubleshooting, packaging and high power capabilities. However, a large number of switches are required in cascaded H-Bridge multilevel inverter that leads to larger system losses and an increase in cost. In this paper the modified cascaded topology is proposed to reduce the number of controlled switches without affecting the resolution of output waveform or the number of voltage levels. We achieved this by replacing some of the high cost controlled transistor switches with diodes, in the cascaded H-Bridges. Furthermore, equal voltage source sharing is also possible by using the proposed topology. Hence the proposed inverter is a type of cascaded multilevel inverter with reduced switches, better modular structure, low cost and high efficiency. The inverter design is validated using simulations and tested on hardware prototype.

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1. INTRODUCTION

Multilevel inverters have been a topic of much research interest since 1960s [1]-[3]. A good literature on various topologies such as Flying Capacitor, Diode clamped and Cascaded H-Bridge can be found in [4]-[5]. Every topology has its own limitations and advantages. For example, flying capacitor topology was ignored due to unequal charging of capacitors [6-7]. Similarly, the clamped diode topology lost the importance due to the unequal losses across semiconductor devices and requirement of a large number of components for higher number of output levels [8]. Due to these and some other similar limitations, the classical cascaded H-Bridge topology got the importance and took the maximum share in the market [9]-[10]. Furthermore equal voltage source sharing is also considered to be a unique feature of the classical cascaded H-Bridge inverters [11], which others lack. Although, classical cascaded H-bridge has many advantages as compared to other classical multilevel inverters, but this research showed that classical cascaded H-bridge converter can be further modified to better modular form resulting in reduced cost and lesser in system losses without effecting resolution of the output wave form.

Another limitation for a cascaded H-Bridge multilevel inverter is it requires multiple isolated DC sources [12], but this drawback in some applications becomes an advantage when multiple voltage sources are easily available like solar panels etc. In such cases, the requirement of step up transformer can be eliminated when these sources are cascaded by multilevel inverter. Another, advantage of using isolated DC

voltage sources is a stable output voltage levels as compare to Flying Capacitor and Diode Clamped methods. All these features are also inherited in the proposed cascaded multilevel inverter.

The focus of our research is to reduce the number of high cost semi-conductor transistor switches (cost in terms of price and power losses). All this is achieved by replacing some of the controlled switches (transistors) in classical H-bridge topology with diodes. Consequently the design also has simple and minimizes the driving circuitry. The unit cell of a classical H-Bridge topology as shown in Figure 1(a) uses four semi-conductor switches like IGBTs or MOSFETs to generate positive and negative stairs in the output waveform [14]-[15]. In our modified design as depicted in Figure 1(b) we have replaced two of the four high cost transistors in each bridge (unit cell) with diodes, the replaced two transistor switches were responsible for generating negative cycle of the waveform. We generated this negative cycle by using additional Inversion Bridge as shown in Figure 4.

The major advantages of the resultant inverter are small number of controlled switches, low cost, less in system losses, better modular form and simplicity of control as compared to classical cascaded H-bridge inverter. Furthermore the pulse width modulation technique can be implemented within the proposed inverter. Additionally the complexity of modulation decreases as less number of switches needs to be controlled as compare to the classical Cascaded H-Bridge Multilevel inverter. The real benefit of the modified inverter comes out by cascading three or greater number of H-bridges. We have justified the working of our technique by using simulations and experimentation.

By cascading H-bridge unit cells, a multilevel inverter commonly known as classical cascaded H-bridge multilevel inverter [2] can be designed. As discussed in [14]-[15] to obtain output with 3, 5, 7 and 9 levels, a single, two, three and four unit cells are required to be cascaded respectively. The number of bridges "B" required to be cascaded for generating "L" number of output levels can be computed as:

$$B = \frac{L-1}{2} \tag{1}$$

Where L is number of output levels can be 3, 5, 7, 9, 11, 13, …, n. Similarly, the number of transistor switches "N" needed can be found as:

$$N=4B \tag{2}$$

A nine level inverter with its switching mechanism can be found in [16]. For convenience, its switching scheme is tabulated here in Table 1, while the output according to the switching scheme is shown in Figure 3. The schematic of the resultant nine levels classical H-bridge is shown in Figure 2. For simplicity the gate driving circuitry is not shown here.

Table 1. Switching Mechanism for Classical H-Bridge Multilevel Inverter

Time		Positive Half Cycle				Negative Half Cycle			
output		V1	V1+V2	V1+V2+V3	V1+V2+V3+V4	V1	V+V2	V1+V2+V3	V1+V2+V3+V4
	Sa1	1	1	1	1	0	0	0	0
Bridge	Sa2	0	0	0	0	1	1	1	1
A	Sa3	0	0	0	0	1	1	1	1
	Sa4	1	1	1	1	0	0	0	0
	Sb1	0	1	1	1	0	0	0	0
Bridge	Sb2	0	0	0	0	0	1	1	1
B	Sb3	0	0	0	0	1	1	1	1
	Sb4	1	1	1	1	0	0	0	0
	Sc1	0	0	1	1	0	0	0	0
Bridge	Sc2	0	0	0	0	0	0	1	1
C	Sc3	0	0	0	0	1	1	1	1
	Sc4	1	1	1	1	0	0	0	0
	Sd1	0	0	0	1	0	0	0	0
Bridge	Sd2	0	0	0	0	0	0	0	1
D	Sd3	0	0	0	0	1	1	1	1
	Sd4	1	1	1	1	0	0	0	0

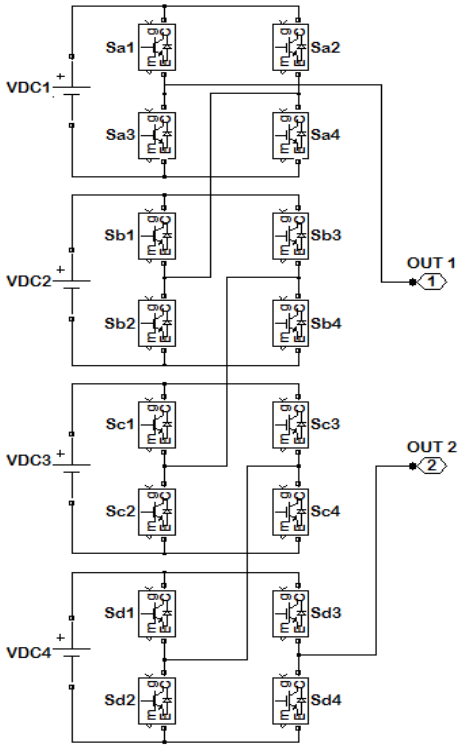

Figure 2. Classical H-Bridge MLI Circuit

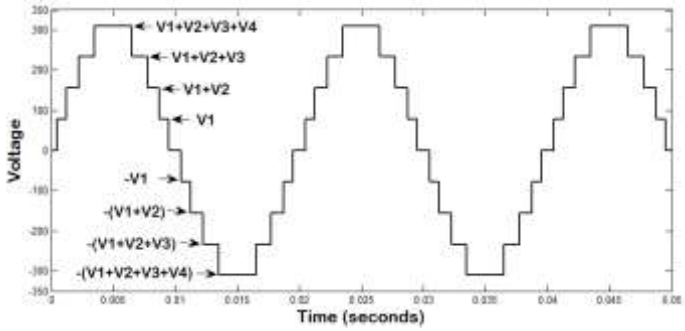

Figure 3. Nine Levels of Classical Casecaded H-bridge Topology

2. PROPOSED TOPOLOGY

In this section we have explained our proposed topology for reducing number of controlled switches. Our research is motivated by a similar work reported in [17]-[21], where authors reduced the switches by using inversion bridge. Although the number of switches in aforementioned references is lesser than our proposed design but there are two limitations associated with those topologies: First is the use of bidirectional switches which increases the cost and second is the lack of equal voltage source sharing feature. In addition to these features, our topology gives a simple and better modular form to symmetrical multilevel inverter by replacing the costly transistor switches and drivers with diodes only. The equal voltage source sharing and PWM technique is also possible to be implement within the proposed inverter.

Figure 4 depicts our proposed topology of a cascaded symmetric multilevel inverter. As compared to classical cascaded H-bridge, we have only used two transistor switches and two additional power diodes instead of four transistor switches in a single cell in order to obtain multilevel output. By using this arrangement a positive or negative multilevel half cycle can be generated. In order to generate the remaining half cycle we used an Inversion Bridge. The inversion bridge as shown in Figure 4 is used to produce an inverted output for generating both positive and negative half cycles.

In the circuit diagram of Figure 4, Sa1, Sa2, Sb1, Sb2, Sc1, Sc2 Sd1 and Sd2 denote the IGBTs of cells A, B, C and D respectively, while D1 to D8 denotes the power diodes which are used to replace the transistors switches. Similarly S1 to S4 are the IGBTs of Inversion Bridge. The isolated DC sources used are denoted by VDC1, VDC2, VDC3 and VDC4. The IGBTs does not need the driver circuitry in simulator. While in hardware HCPL 3120, TLP 250 or IR2110 driver ICs can be used as gate drivers for transistors. The number of switches "NS" required for generating L number of levels according to our topology can be found as:

$$Ns = 2B + 4 , \quad (3)$$

where B is required number of H-bridges and is given by

$$Nd = 2B , \quad (4)$$

where Nd is required number of diodes

$$B = \frac{L-1}{2} \tag{5}$$

where L is number of levels having values 3, 5, 7, 9, 11, 13, , n.

As a case study, we considered a nine level inverter with modified topology, for justifying the working of our design. We simulated and build a hardware prototype for this purpose. For nine levels according to Equations 3, 4 and 5, we require twelve transistor switches and eight power diodes instead of sixteen transistor switches as required for classical topologies [14]-[15].

Table 2. Switching Mechanism for Proposed Multilevel Inverter

Time		Positive Half Cycle				Negative Half Cycle			
output		V1	V1+V2	V1+V2+V3	V1+V2+V3+V4	V1	V1+V2	V1+V2+V3	V1+V2+V3+V4
Bridge A	Sa1	1	1	1	1	1	1	1	1
	Sa4	1	1	1	1	1	1	1	1
Bridge B	Sb1	0	1	1	1	0	1	1	1
	Sb4	1	1	1	1	1	1	1	1
Bridge C	Sc1	0	0	1	1	0	0	1	1
	Sc4	1	1	1	1	1	1	1	1
Bridge D	Sd1	0	0	0	1	0	0	0	1
	Sd4	1	1	1	1	1	1	1	1
Inversion Bridge	Sp1	1	1	1	1	0	0	0	0
	Sp2	0	0	0	0	1	1	1	1
	Sp3	0	0	0	0	1	1	1	1
	Sp4	1	1	1	1	0	0	0	0

The switching scheme required for the proposed topology is given in Table 2 and resultant simulated waveform is shown in Figure 5. The simulated output waveform closely resembles with the output waveform obtained using classical H-bridge as given in Figure 3.

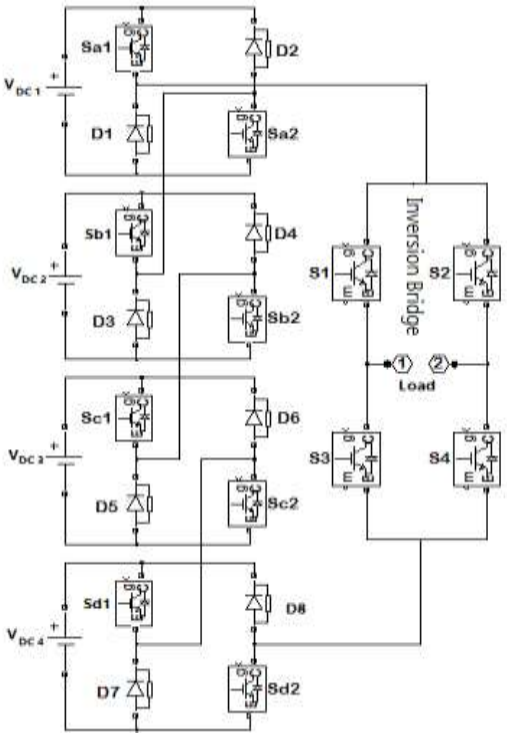

Figure 4. Proposed nine levels Multilevel Inverter

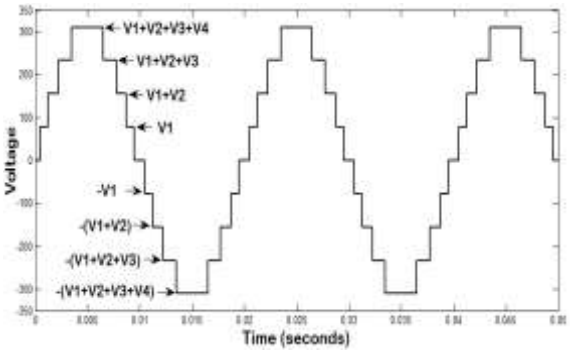

Figure 5. Output wave form of a proposed Multilevel Inverter

3. MODULATION TECHNIQUE

The harmonics spectral density of output waveform is found using simulation tool for resistive load. Also, it is found that the spectral density is concentrated around low frequencies with Total Harmonic Distortion of 12.98%. The result of simulation is given in Figure 6. Modulation can be used to control and stabilize the output waveform of an inverter. To shift low frequency harmonics to high frequencies, a high frequency carrier based Pulse Width Modulation technique is used. It is done to reduce the size of a filter required for generating pure sine wave. In our case study we used a triangular wave of 20 kHz as a carrier. The modulated signal used is of 50Hz. The pulse width modulated switching signal is generated by comparison of these two signals [20]. The resultant modulated multilevel inverter output is given in Figure 7.

After modulation the low frequency harmonics are shifted to higher frequency, this helps to separate and extract the fundamental components from output by using a filter with smaller values of components. The shifted spectral density of the modulated inverter is shown in Figure 8, where the spectral density of harmonics is located near 20 kHz with Total Harmonic Distortion of 13.77 %. In order to get pure sine wave from the modulated signal of Figure 7, the output modulated wave form is subjected to the LCL filter. The LCL values are computed using [20]. The computed values for the LCL filter Figure 9 using the equations given in [20] are Li= 4mH, Lg= 2.4mH, fres=2.3kHz, and Rsd=7.5 Ω. The simulated filtered output is shown in Figure 10.

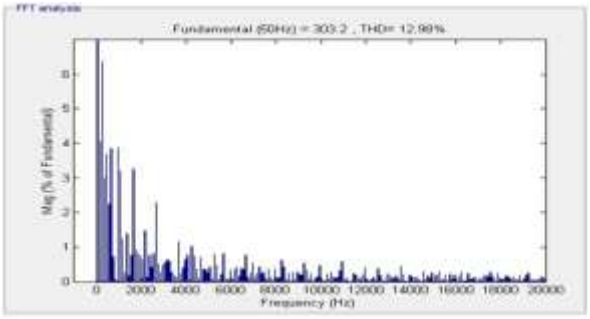

Figure 6. Spectral density of harmonics without modulation

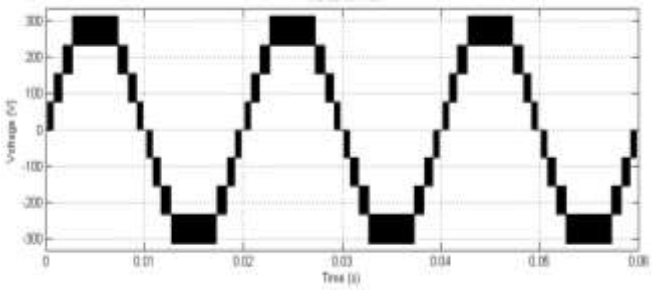

Figure 7. Modulated output of the proposed inverter output

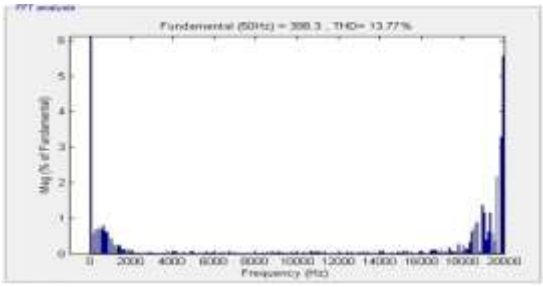

Figure 8. Harmonics in the modulated

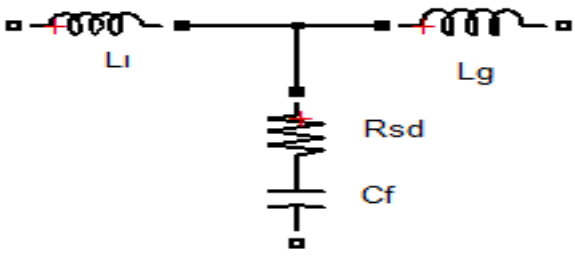

Figure 9. LCL filter

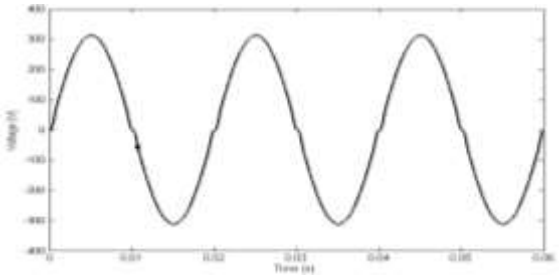

Figure 10. Filtered output

4. EQUAL SOURCE SHARING

The series connection of sub multilevel inverter [19] and many other topologies reported in [17]-[18] lack the ability of equal voltage source sharing, while only classical cascaded H bridge inverter topology has this feature [11]. This feature in the inverter equally distributes stress on the power providing sources and can also be used to drain the power from a specific source as desire. In our proposed topology equal source sharing can be implemented. The switching scheme used for equal voltage sources sharing is listed in Table 4 and the corresponding output waveform produced is shown in Figure 11. The sources used for a specific level are also marked along the steps in Figure 11.

Table 4. Switching Mechanism for equal voltage source sharing

Time		Positive Half Cycle				Negative Half Cycle			
output		V1	V1+V2	V1+V2+V3	V1+V2+V3+V4	V1	V1+V2	V1+V2+V3	V1+V2+V3+V4
Bridge	Sa1	1	1	1	1	0	0	0	1
A	Sa4	1	1	1	1	1	1	1	1
Bridge	Sb1	0	1	1	1	0	0	1	1
B	Sb4	1	1	1	1	1	1	1	1
Bridge	Sc1	0	0	1	1	0	1	1	1
C	Sc4	1	1	1	1	1	1	1	1
Bridge	Sd1	0	0	0	1	1	1	1	1
D	Sd4	1	1	1	1	1	1	1	1
Inver-	Sp1	1	1	1	1	0	0	0	0
sion	Sp2	0	0	0	0	1	1	1	1
Bridge	Sp3	0	0	0	0	1	1	1	1
	Sp4	1	1	1	1	0	0	0	0

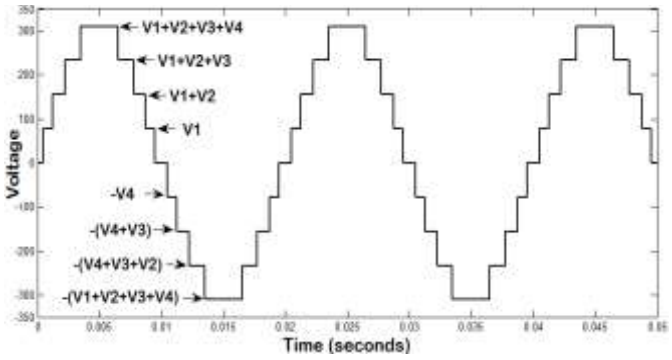

Figure 11. Output with equal voltage source sharing

5. INDUCTIVE LOAD TESTING

The modified topology is tested for inductive loads as well. Inductive loads produce back e.m.f. which inserts stress on switches when there is no path for reverse current. The multilevel inverter decreases the total harmonic distortion which is 12.98% in the case of 9 level output wave form. The reduction of harmonics reduces stress on the motor winding and also decreases vibration and audible noise of motor. It also increases the efficiency and life of motor. The proposed inverter is tested for inductive load using simulation and the result of simulation is given in Figure 12.

6. COST EFFECTIVE TOPOLOGY

In this section we have computed the cost effectiveness of our topology. We have found that the benefit of our topology starts when the inverter output levels exceed five. The comparison between the number of switches required for our and classical cascaded H-bridge topology is computed by using equations 1 to 4. The result is tabulated in Table 5 against various number of output levels. From the Table 5 it can be seen that reduction in transistor switches starts after number of levels are increased from 5 levels. For more elaboration we have also demonstrated our results as a graph shown in Figure 13. By reducing switches its associated circuits such as drivers are also reduced by the same number as transistors, which further reduces the cost of inverter. In addition to cost reduction, the complexity of control is also reduced.

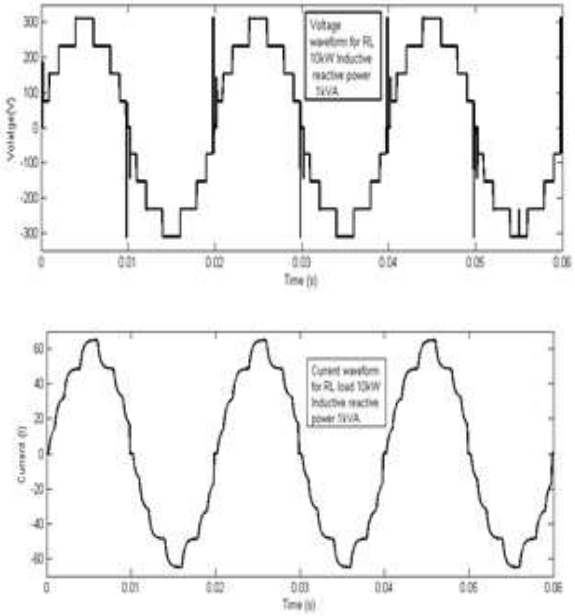

Figure 12. Inductive load testing results

Table 5. Comparison of Components for Classical and Proposed Multilevel Inverter.

Number of levels	Classical Cascaded H-Bridge Topology		Proposed Cascaded H-Bridge Topology	
	Number of transistors	Number of drivers	Number of transistors	Number of drivers
5	8	8	8	8
7	12	12	10	10
9	16	16	12	12
11	20	20	14	14
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N	2n-2	2n-2	n+3	n+3

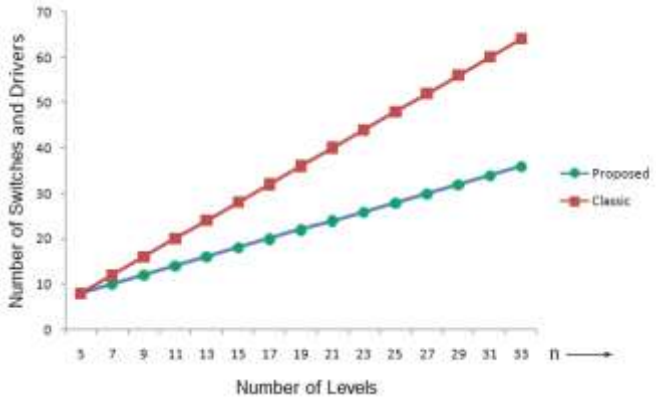

Figure 13. Comparison of the Switches in CHB and Proposed Inverter

7. HARDWARE IMPLEMENTATION

In order to validate our design we have also tested it by building a prototype as shown in Figure 14. By using the prototype with a switching pattern given in Table 3 an output of nine levels obtained is shown in Figure 15. The details of prototype are: It consists of four H-bridges, each consisting of two IGBTs, two power diodes and each IGBT has its driver along with the essential peripheral components. The hardware has been tested to generate output voltage of 220V RMS. The generated output is measured using oscilloscope and after scaling the output is shown in Figure 15 for resistive load.

Figure 14. Prototype of the Designed Inverter

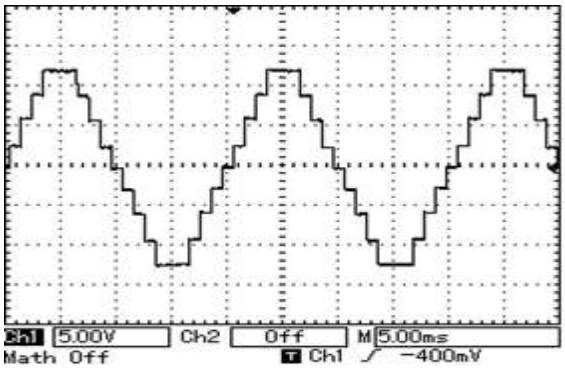

Figure 15. Output Waveform of Prototype

8. CONCLUSIONS

Multilevel inverters are preferred due to their high quality output waveform resolution, low total harmonic distortion and reduced filter size for generating pure sine wave output. Cascaded H-bridge topology is known to be the best among various topologies introduced in the early years of multilevel inverters. However the number of switches requires has been a major problem associated with the Cascaded H-Bridge topology. No remarkable work was done in order to reduce the number of switches in the cascaded H-bridge topology for many years, only recently interest developed in this area. In this paper, we have proposed a new topology which has a basic design based upon the cascaded H-bridge topology but with capability of reducing number of transistor switches and there associated drivers. Reduction of switches is achieved by replacing switches with diodes. The resultant topology without compromising output number of levels results in a cost effective design. Another feature of our design is that it also supports equal source sharing. The topology is validated using simulations and with hardware prototype.

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