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Performance Analysis of Modified SVPWM Strategies for Three Phase Cascaded Multi-level Inverter fed Induction Motor Drive

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ABSTRACT

This paper presents new modified space vector pulse width modulation techniques (Phase disposition-Space vector pulse width modulation, Alternative Phase Opposition disposition- Space vector pulse width modulation and Phase Opposition disposition-Space vector pulse width modulation) are analyzed for three-phase cascaded multi-level inverter fed induction motor from the point of view of the Phase voltages, line voltage, stator current,speed,torque and Total harmonic distortion.in the proposed modified technique the reference signals are generated by adding offset voltage to the reference phase voltages.This modified SVPWM technique does not involve region indentification,sector identification for switching vector determination as are required in the conventional multi level SVPWM technique,it is also reduces the computation time compared to the conventional space vector PWM technique.The necessary calculations for generation of new modified SVPWM for the modulation strategies have presented in detail. It is observed that the modified SVPWM modulation ensures excellent, close to optimized pulse distribution results and THD is compared to for five-level, seven-level, nine-level and eleven-level Cascaded H-Bride Multi-level Inverter fed to Induction motor. Theoretical investigations were confirmed by the digital simulations using MATLAB/SIMULINK software.

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1. INTRODUCTION

In the late 1990s, multilevel inverters are the most attractive solution for high power and medium voltage drive when high power IGBTs is commercially available in the market. Multilevel inverters are implemented to overcome the disadvantages of traditional two-level inverter [1]. More on the various multilevel topologies and their applications can be found in [2]. Since the concept of the multilevel PWM inverter was introduced [3]. Various modulation strategies have been developed and studied in great detail [4]-[6].

Several multicarrier techniques have developed to reduce the distortion in multilevel inverter, based on the classical SPWM with triangular carriers, some methods use carrier disposition and others use phase shifting of multiple carrier signals [7]-[9]. Multilevel inverter structures have been developed to overcome shortcomings in solid-state switching device ratings so they can be applied to higher voltage systems. The multilevel voltage source inverters [10].

In this paper the Modified SVPWM (Phase disposition-Space vector pulse width modulation, Alternative Phase Opposition disposition- Space vector pulse width modulation and Phase Opposition disposition-Space vector pulse width modulation) strategy of five-level, seven-level, nine-level and eleven-level inverters are compared for THD. The paper mainly deals with the computation and the comparison of the motor harmonic losses of different PWM solutions and with the selection of the solutions providing the best results. Finally, the drive harmonic losses will be compared for each technique.

2. THREE-PHASE N LEVEL CASCADED MULTI-LEVEL INVERTER

The three phase N-level cascaded multilevel inverter (CMI) or Series H-bridge Multi-Level Inverter topology shown in Figure 1. Each cell contains four active switching device and a minimum of one dc capacitor to form a single-phase H-bridge inverter.The different cells are connected as depicted in Figure 1 to construct a three-phase configuration. With this configuration, each cell in a leg will provide three-level output phase voltages (V_{aN}, V_{bN} and V_{cN}) and five level line voltages (V_{ab}, V_{bc} and V_{ca}). The number of incremental voltage step is increased by connecting additional cell in series, where the number of phase voltage is formulated as (n^{th}-cell*2)+1, and the number of levels in line voltage are 2M-1, where M is the number of level in phase voltage [11].

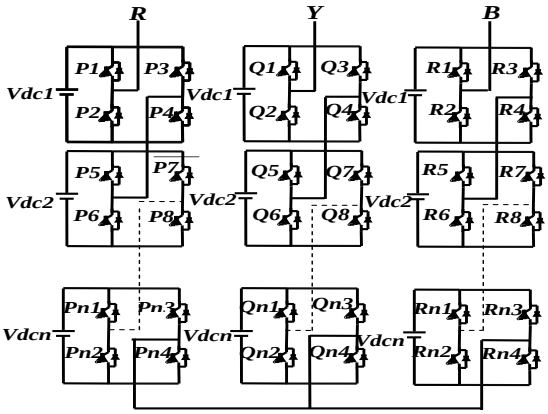

Figure 1. N-level cascaded inverter

3. PROPOSED MODIFIED SVPWM TECHNIQUE

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [12]. To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, T_{offset}, is added to the reference phase voltages. where the magnitude of T_{offset} is given by

$$T_{offset} = \frac{-(Tmax+Tmin)}{2} \quad (1)$$

In Equation, T_{max} is the maximum magnitude of the three sampled reference phase voltages, while T_{min} is the minimum magnitude of the three sampled reference phase voltages, in a sampling interval. The addition of the common mode voltage, T_{offset}, results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the modified reference PWM technique. Above Equation is based on the fact that, in a sampling interval, the reference phase which has lowest magnitude (termed the min-phase) crosses the triangular carrier first, and causes the first transition in the inverter switching state. While the reference phase, which has the maximum magnitude (termed the max-phase), crosses the carrier last and causes the last switching transition in the inverter switching states in a two level modified reference PWM scheme [13]. Thus the switching periods of the active vectors can be determined from the (max-phase and min-phase) sampled reference phase voltage amplitudes in a two-level inverter scheme [14]-[15].

To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, the procedure for this is given in [16], an offset time, offset T, is added to the reference phase voltages where the magnitude of T_{offset} given Equation (2)-(7).

$$T_a = \frac{-(Va * Ts)}{Vdc} \quad (2)$$

$$T_b = \frac{-(Vb * Ts)}{Vdc} \quad (3)$$

$$T_c = \frac{-(Vc * Ts)}{Vdc} \quad (4)$$

T_a,T_b and T_c are the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages.

$$T_{offset} = \left[\frac{To}{2} - T_{min}\right] \quad (5)$$

$$T_o = [Ts - T_{offeset}] \quad (6)$$

$$T_{offset} = [Tmax - T_{min}] \quad (7)$$

Shown in Figure 2. Modified Phase disposition-Space vector pulse width modulation pulse generation, Figure 3. Modified Phase Opposition disposition-Space vector pulse width modulation pulse generation and Figure 4. Modified Alternative Phase Opposition disposition- Space vector pulse width modulation pulse generation.

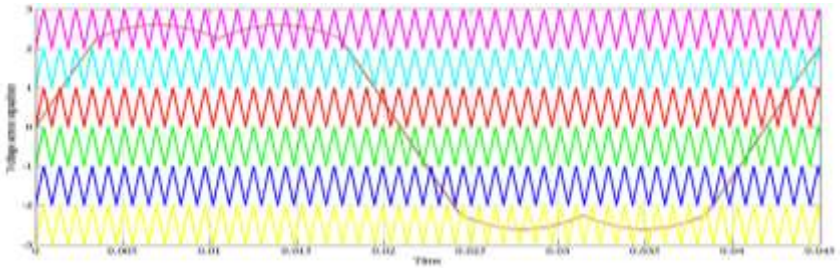

Figure 2. Modified PD-SVPWM pulse generation

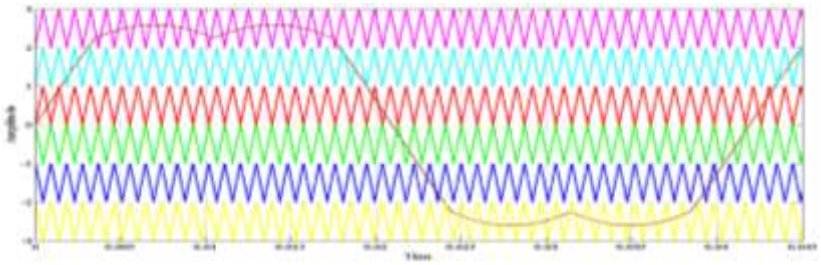

Figure 3. Modified POD-SVPWM pulse generation

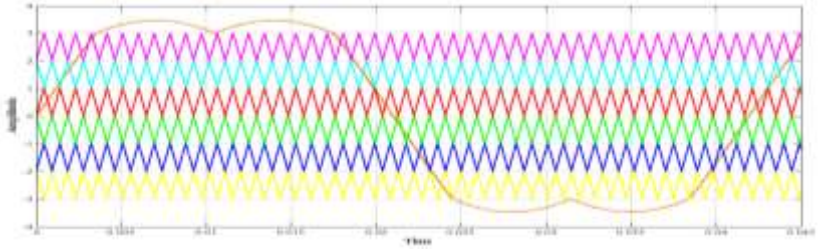

Figure 4. Modified APOD-SVPWM pulse generation

4. SIMULATION RESULTS

An five level,seven level nine level and eleven level cascaded multilevel inverter fed with Induction motor is simulated. The carrier frequency fc is 1 kHz. The modulating pulses are generated by the comparing the reference wave with the triangular waves. For m level cascaded multilevel inverter m-1 carrier waves required and the simulation study is carried out using MATLAB/SIMULINK.

4.1. Five-level Modified SVPWM Technique

The output voltage of the inverter for line to line is about 410V when using Modified SVPWM.The total harmonic distortion of the output voltage is about 12.43% (PD-SVPWM), 12.72% (POD-SVPWM) and 13.29% (APOD-SVPWM) Figure 5, Figure 6, and Figure 7. Shown in the harmonic spectrum for the Line voltage of the inverter. It is observed that the significant harmonics are located around the carrier frequency fc for the line voltage waveform in PD-SVPWM and POD-SVPWM. It is observed that the total harmonic distortion is less in PD-SVPWM technique with comparison to other modified space vector PWM and SPWM techniques. Figure 8 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.1 sec. Due to transient behavior of the system at the starting from 0.1 sec. System has attained steady state conditions.The speed and torque characteristics of induction motor fed to five-level inverter has shown in Figure 9 from the Figure it can be seen that the steady state operation of system has achieved at 0.15 sec.

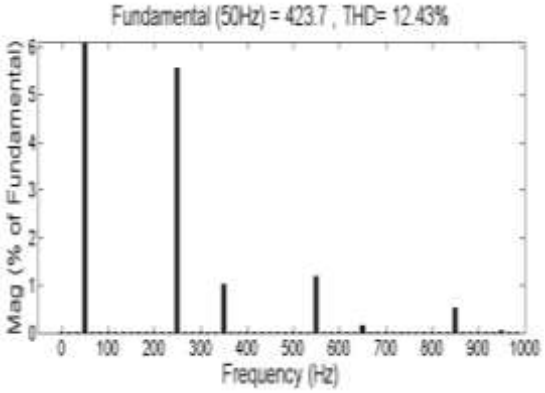

Figure 5. THD for five level modified PD-SVPWM

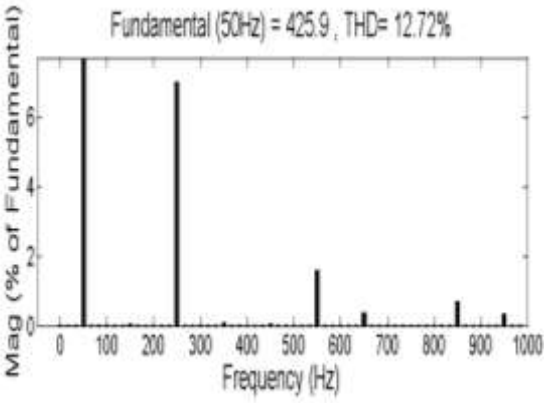

Figure 6. THD for five level modified POD-SVPWM

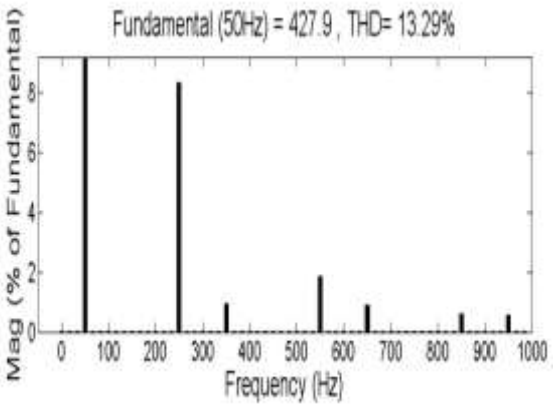

Figure 7. THD for five level modified APOD-SVPWM

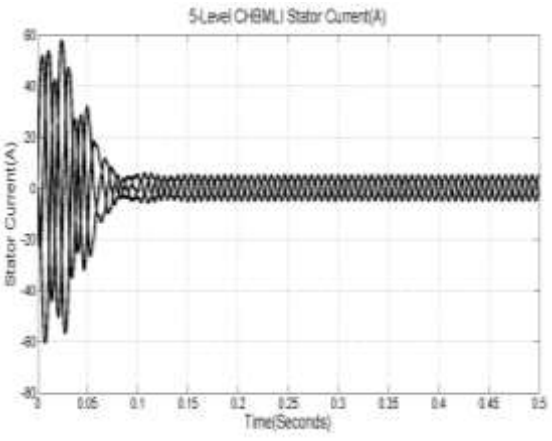

Figure 8. Five level output stator current of the inverter

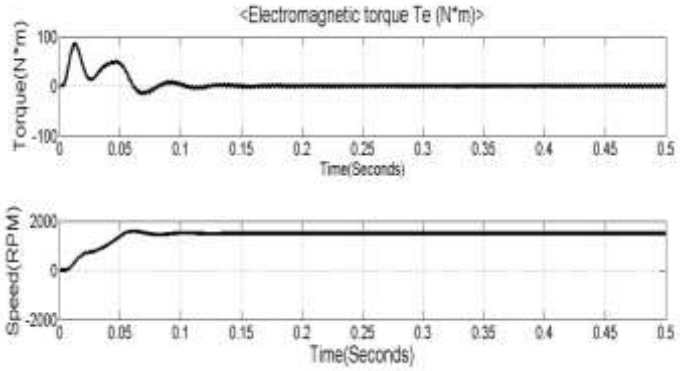

Figure 9. Five level output torque and speed of the inverter

4.2. Seven-level Modified SVPWM Technique

The output voltage of the inverter for line to line is about 410V when using Modified SVPWM.The total harmonic distortion of the output voltage is about 9.08% (PD-SVPWM), 9.23% (POD-SVPWM) and 9.89% (APOD-SVPWM). Figure 10, Figure 11, and Figure 12. Shown in the harmonic spectrum for the Line voltage of inverter.It is observed that the most significant harmonics are centered as sidebands around the carrier frequency fc and therefore no harmonics occur at fc for APODSVPWM technique. It is observed that the total harmonic distortion is less in PD-SVPWM technique with comparison to other modified space vector PWM and SPWM techniques.

Figure 13 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.2 sec.Due to transient behavior of the system at the starting from 0.2 sec. System has attained steady state conditions.The speed and torque characteristics of induction motor fed to seven-level inverter has shown in Figure 14 from the Figure it can be seen that the steady state operation of system has achieved at 0.25 sec.

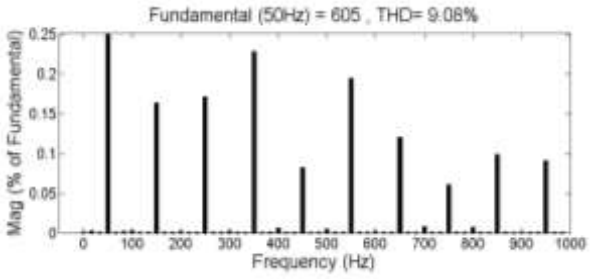

Figure 10. THD for seven level modified PD-SVPWM

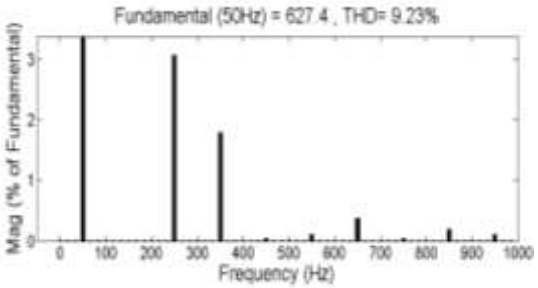

Figure 11. THD for seven level modified POD-SVPWM

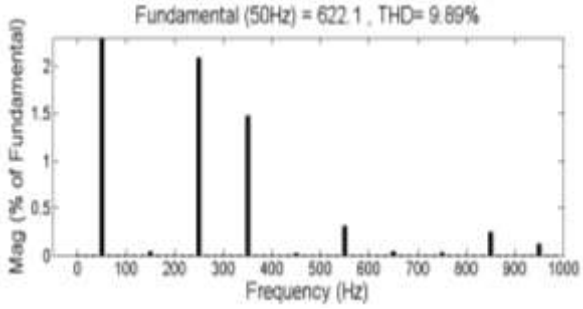

Figure 12. THD for seven level modified POD-SVPWM

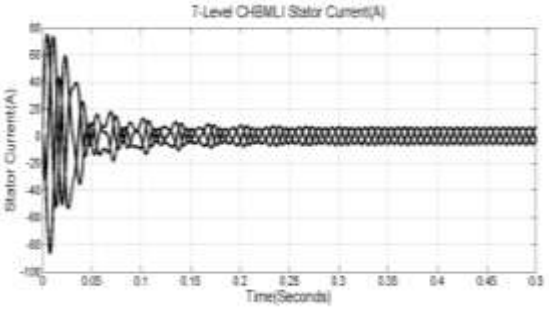

Figure 13. Seven level output stator current of the inverter

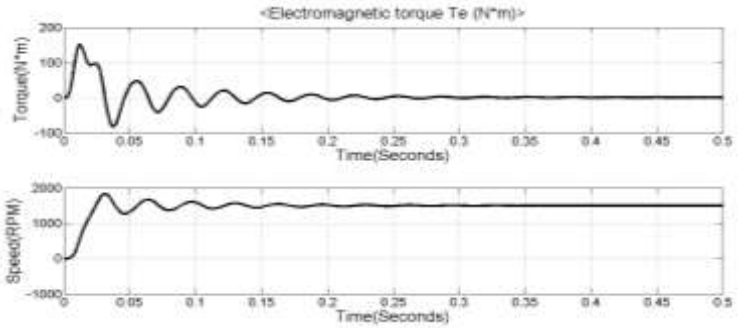

Figure 14. Seven level output torque and speed of the inverter

4.3. Nine-level Modified SVPWM Technique

The output voltage of the inverter for line to line is about 410V when using Modified SVPWM.The total harmonic distortion of the output voltage is about 7.67% (PD-SVPWM),8.00% (POD-SVPWM) and 8.62% (APOD-SVPWM) when using Modified SVPWM technique on nine-level cascaded multi-level inverter. Figure 15, Figure 16, and Figure 17. Shown in the harmonic spectrum for the Line voltage of inverter. It is observed that the total harmonic distortion is less in PD-SVPWM technique with comparison to other modified SVPWM and SPWM techniques.

Figure 18 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.4 sec.Due to transient behavior of the system at the starting from 0.4 sec. System has attained steady state conditions.The speed and torque characteristics of induction motor fed to nine-level inverter has shown in Figure 19 from the Figure it can be seen that the steady state operation of system has achieved at 0.35 sec.

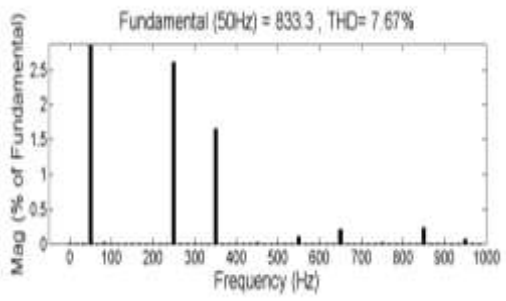

Figure 15. THD for nine level modified PD-SVPWM

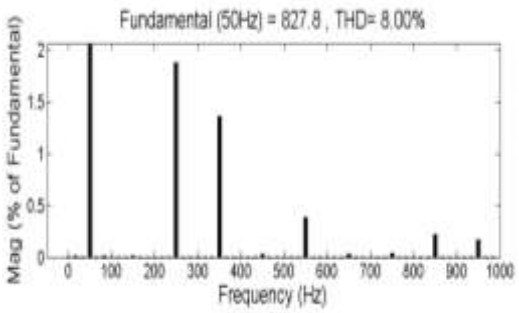

Figure 16. THD for nine level modified POD-SVPWM

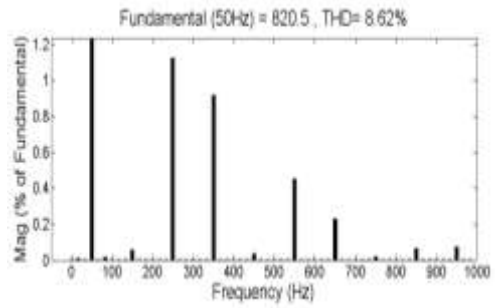

Figure 17. THD for nine level modified APOD-SVPWM

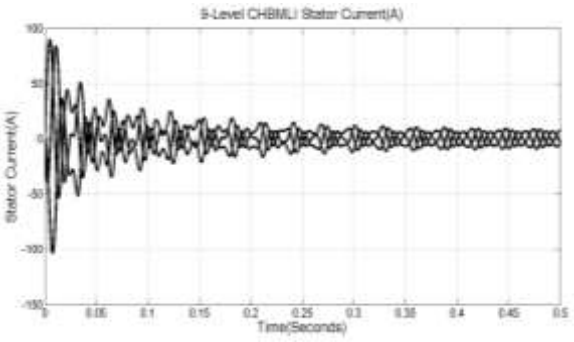

Figure 18. Nine level output stator current of the inverter

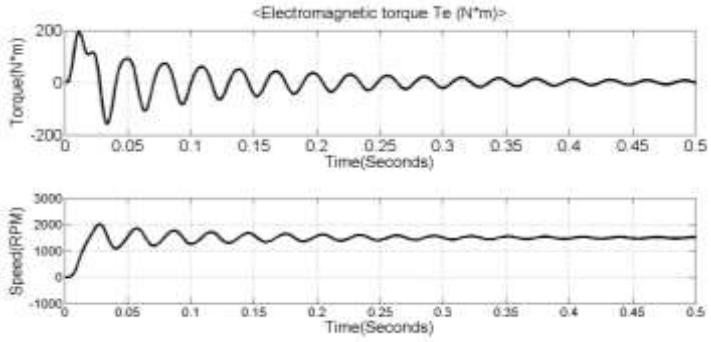

Figure 19. Nine level output torque and speed of the inverter

4.4. Eleven-level Modified SVPWM Technique

The output voltage of the inverter for line to line is about 410V when using Modified SVPWM.The total harmonic distortion of the output voltage is about 5.42% (PD-SVPWM), 7.19% (POD-SVPWM) and 7.80% (APOD-SVPWM) when using Modified SVPWM technique on eleven-level cascaded multi-level inverter. Figure 20, Figure 21 and Figure 22. Shown in the harmonic spectrum for the Line voltage of inverter.It is observed that the total harmonic distortion is less in PD-SVPWM technique with comparison to other modified space vector PWM techniques and SPWM techniques.

Figure 23 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.35 sec.Due to transient behavior of the system at the starting from 0.35 sec.System has attained steady state conditions.The speed and torque characteristics of induction motor fed to eleven-level inverter has shown in Figure 24 from the Figure it can be seen that the steady state operation of system has achieved at 0.35 sec.

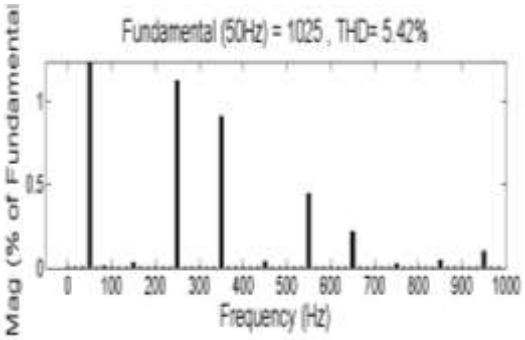

Figure 20. THD for Eleven level modified PD-SVPWM

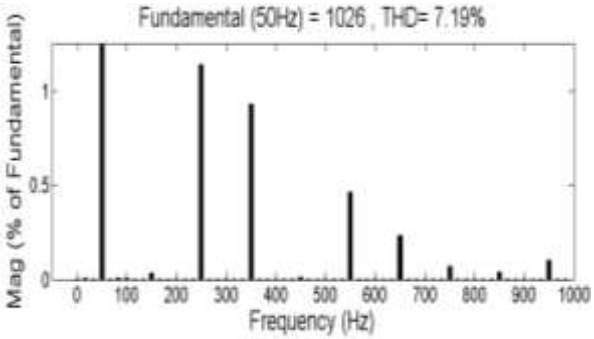

Figure 21. THD for Eleven level modified POD-SVPWM

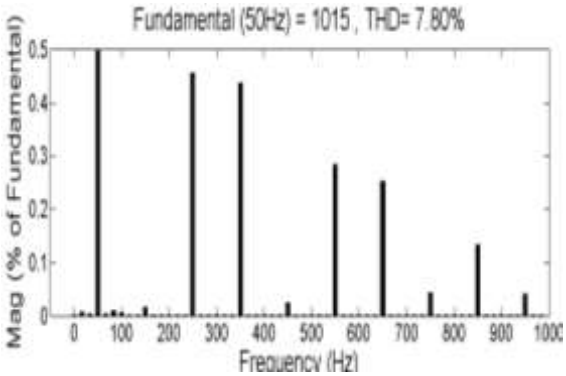

Figure 22. THD for Eleven level modified APOD-SVPWM

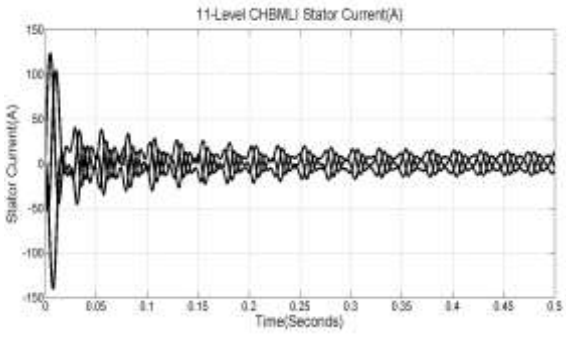

Figure 23. Eleven output stator current of the inverter

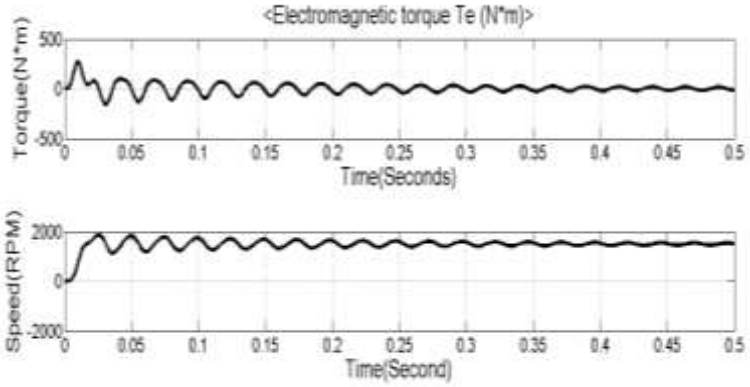

Figure 24. Eleven output torque and speed of the inverter

This proposed modified SVPWM signal generation does not involve region identification, sector identification or look up tables for switching vector determination required in the conventional multilevel SVPWM technique. This scheme is computationally efficient when compared to conventional multilevel SVPWM scheme.we can observed that all level(five-level,seven-level,nine-level and eleven-level) of the cascaded multi level inverter the total harmonic distortion is less in PD-SVPWM technique with comparison to other conventional space vector PWM techniques and all other SPWM techniques.The comparisons of total harmonic distortion of the output voltage using Modified SVPWM (PD-SVPWM, POD-SVPWM and APOD-SVPWM) technique on five-level, seven-level, nine-level and eleven-level cascaded multi-level inverter shown in Table 1.

Table 1. The Comparisons of THD for Five, Seven, Nine and Eleven Cascaded Inverter.

Outputvoltagelevel	Modifiedsvpwmtechnique	%THD(V)
Five-level	PD	12.43
	POD	12.72
	APOD	13.29
Seven-level	PD	9.08
	POD	9.23
	APOD	9.89
Nine-level	PD	7.67
	POD	8.00
	APOD	8.62
Eleven-level	PD	5.42
	POD	7.19
	APOD	7.80

5. CONCLUSION

The reference signals generated by using modified svpwm techniques.this method does not involes region iditifications,sector iditifications for switching vector determention requied in conventional SVPWM technique.In this paper the comparison of modified SVPWM most proffered control strategies applied to three phase Cascaded inverter are presented. The waveforms clearly depicting that almost all the control strategies are functioning well in controlling the line voltage, phase voltage, stator current, speed and torque. The THD of the pd-svpwm,pod-svpwm,apod-svpwm strategies when compared all levels(five,seven,nine and eleven),it is obvious that pd-svpwm is the most efficient control strategy for all levels(five,seven,nine and eleven).It is obvious that pd-svpwm(eleven-level) is the most efficient control strategy with low THD of about 5.42% among those control strategies. The output line voltage quantity is better when using PD-SVPWM.

ACKNOWLEDGMENT

We thank the University Grants Commission (UGC), Govt. of India, New Delhi for providing Major Research Project to carry out the Research work on Multi-Level Inverters.

APPENDIX

Table 2. System parameters of the induction motor

Parameters	Specifications
Input voltage	400VRMS(PhasePhase)
Inverter voltage	100(Volts)
Rotor speed	1440(RPM)
Fundamentalfrequency	50(Hz)
Switching frequency	1K(Hz)
Modulation index	0.866

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