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Voltage Ripple Reduction in Voltage Loop of Voltage Source Converter

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ABSTRACT

In order to achieve a good dynamical response of a full-bridge AC-DC voltage source converters (VSC). The bandwidth of PI controller must be relatively wide. This leads to the voltage ripple produced in the control signal, as known that its ripple frequency has twice of the line frequency and cause the 3rd harmonic of an input current. A Ripple Voltage Estimator (RVE) algorithm and Feed-Forward Compensation (FFC) algorithm are proposed and added to the conventional control. The RVE algorithm estimated the ripple signal to subtract it occurring in the voltage loop. As a result, the 3rd harmonic of the input current can be reduced, and hence the Total Harmonic Distortion of input current (THDi) are improved. In addition, the FFC algorithm will offer a better dynamical response of output voltage. The performance evaluation was conducted through the simulation and experiment at 110Vrms/50Hz of the input voltage, with a 600 W load and 250 Vdc output voltage. The overall system performances are obtained as follows: the power factor at the full load is higher 0.98, the harmonic distortion at AC input power source of the converter is under control in IEC61000-3-2 class A limit, and the overall efficiency is greater than 85%.

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1. INTRODUCTION

Undoubtedly, using diode-bridge rectifier to assemble a single phase AC-DC Converters leads to pollution in electrical system [1]. The line input current is non-sinusoidal and cause voltage distortion at the Point of Common Coupling (PCC) which deviate from sinusoidal waveform. Consequently, high Total Harmonic Distortion of current (THDi) and low power factor are occurred. A simple method [2] to reduce those problems are to add a passive LC filter into AC input line voltage, but the input current is still far from sinusoidal.

In order to compliance with necessary harmonic standards such as IEC 1000-3-2, an AC-DC Power Factor Correction (PFC) converters using a Single Switch Topology (SST) such as Boost, Buck-Boost, CUK and SEPIC has been introduced and widely popular [3]-[6]. These converters produce very low current harmonic which injected into the line due to quasi-sinusoidal input current waveform. However a diode-rectifier module is needded for installing to SST, and also the power can be flowed only one direction, from AC side to DC side.

In [7]-[10], Voltage Source Converters (VSC) based on the full-bridge AC-DC converter circuit as shown in Figure 1 are widely used in medium and high-power applications. Controlling of the VSC has the same maner as the SST; nevertheless, it has advantage over SST in term of capability to control the power

flow to be bi-directional. For this reason, they play an important role in renewale energy such as energy from solar cell or wind turbine for injecting energy into utility grid of a AC power system.

The normal simple cascade control structure has been presented in [7]-[9], where outer loop is a output voltage controller and inner loop is an input current controller. To achieve a good dynamical response of the output voltage, the crossover frequency which is set in the PI controller must be relatively high. The current loop forces the input current to track the reference current signal, which is obtained by multiplying a sinusoidal signal template by a amplitude signal from feedback voltage in the voltage loop. Thus, if the feedback voltage is a DC value, the reference input current signal will be sinusoidal. Then, the input current can be forced to sinusoidal if the input current is perfectly controlled to track this reference signal. In practical, a ripple signal at twice of the line frequency (100Hz for 50Hz line frequency) in the voltage error signal is natural exist. Consequently the 3rd harmonic signal in the reference input current is occurred which causes the distortion of reference input current and also the input line current. In order to reduce the ripple voltage, an easy solution is to add a bulk-electrolytic capacitor at the output. However, this capacitor causes to increase size and cost of the VSC, but cannot get rid of the double line frequency component in the voltage control loop.

A standard design of voltage loop to reduce the THDi is placed a Low-Pass Filter (LPF) next after an output voltage sensor. The LPF is tuned to offer cutoff frequency or bandwidth around 10Hz-20Hz, then the ripple flowing from output voltage is attenuated. Although this design has improved the THDi of the system, but the main disadvantage is lack of output voltage response. Conversely, if the LPF is loosened or higher bandwidth, the responsibility will improve but the THDi will be increased. In some paper [10], the voltage loop was controlled by the fuzzy controller, but the THDi was more 5%.

The power-balanced control algorithm or Feed-Forward Compensation (FFC) proposed by [4], the main aim of them is to add the load information which is the disturbance before current loop. As a result the output voltage dynamic response is improved, but the THDi will not be improved by this technique.

In [4] has been proposed the method for reducing the 3rd harmonic in PFC type CUK topology. The output voltage is sampled to voltage loop. The sample period is at every zero crossing point of the input voltage. So that only a DC value is collected to be multiply with the sinusoidal template. Therefore the reference current signal will be perfectly sinusoidal. However the response of output voltage is still poor because if the updating reference is occurred only 2 times in a line periode.

This paper will consider the situation in which the bandwidth of the LPF and the crossover frequency of the PI controller is high value. The first part of paper presents an analysis of the conventional cascade control VSC. Then propose the simple method to reduce a ripple voltage in voltage loop of the VSC by using a Ripple Voltage Estimation (RVE) algorithm but offer better responsibility by using the FFC algorithm. The output ripple is estimated by the RVE algorithm and subtract it from voltage error signal. The result of this, the 3rd harmonic of the input current is reduced, and hence the THDi is improved. The concept of the FFC technique is the same as the power balance control technique in feeding load information into control system. These algorithms are implemented based on a microcontroller. Finally, the simulation and experimental resuls are shown.

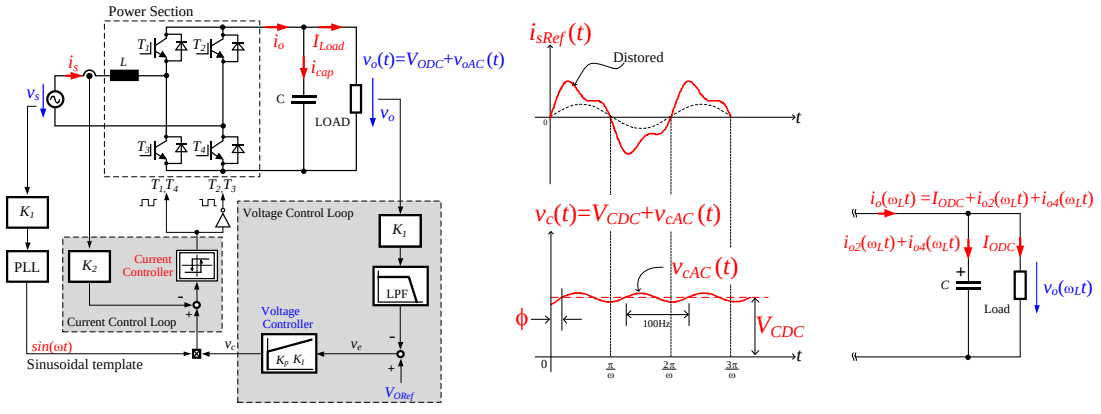


Figure 1. (a) The power circuit is a Voltage Source Converter (VSC) built from full-bridge AC-DC converter and its cascade control. (b) The ripple in voltage loop which is the cause of distorted-reference input current (c) Analysis the direction of output current.

2. ANALYTICAL MODEL OF THE CASCADE CONTROL VSC

The controlling objectives of the VSC are to

a. Maintain the output voltage VO to the desired value
b. Control the input current is to nearby sinusoidal waveform and meets the necessary harmonic standards
c. Control the phase of the input current is to synchronize with the phase of the input voltage vs in order to succeed in unit power factor.

The conventional control configuration, which comprises two feedback loop as shown in Figure 1(a). The control system has the outer voltage loop regulating output voltage VO, to aspire a value of reference output voltage VORef and sending a controlled signal vc to the inner current loop (remark that the vc is a value of peak reference input current). Inner current loop, the is is controlled to track the reference current by a hysteresis controller. A Phase Lock Loop (PLL) generates a purely sinusoidal signal sin (ωt) which synchronizes with the phase of vs. In steady state condition, the controlled-signal vc should be a DC signal so that the isRef obtained from the product of the vc and sin (ωt) remains perfectly sinusoidal signal. In practical, there is a ripple voltage which rides on the vc. The fundamental reason is widely known that the output voltage (vo) compose of an average DC voltage and a ripple voltage which has twice of line frequency. Then after the vo is sensed, the vo will be subtracted from the VORef, which is a constant value. The result of subtraction is an error signal (ve) where that ripple still remain as shown Figure 2(a). Consequently, the signal from high bandwidth voltage controller, will not constant but comprise the ripple as well. However, if low cutoff frequency of voltage controller is used, the will be a DC value. Therefore, the input current can be controlled to be sinusoidal as the input current reference signal as shown in Figure 2(b).

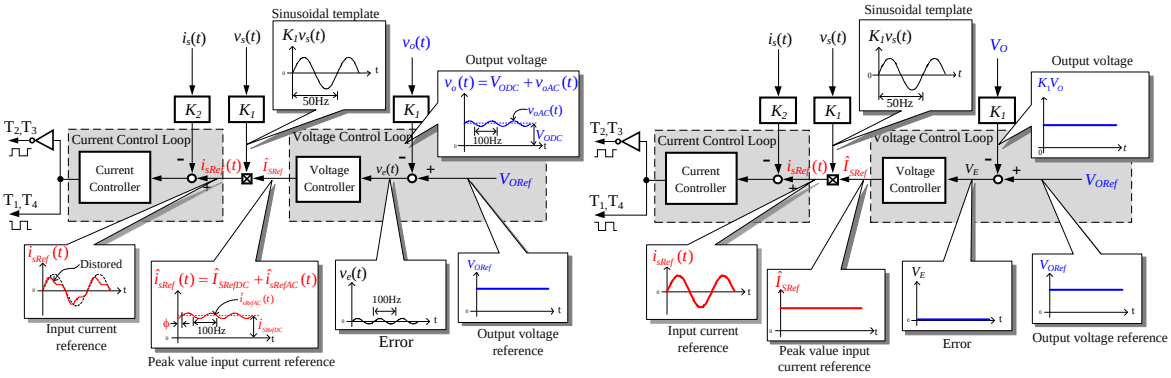


Figure 2. The effect of the ripple output voltage in case of conventional control technique when: (a) there is the ripple in voltage loop. (b) there is not the ripple in voltage loop

2.1. The Input Current

Assume that, the power circuit is controlled, then the input voltage $v_s(\omega_L t) = \hat{V}_S \sin(\omega_L t)$. Where $\hat{V}_S$ is the peak value of input voltage $v_s(\omega_L t)$ ω_L is its angular frequency. If the controlling of VSC force the input current $i_s(\omega_L t)$ to nearby sinusoidal, then the $i_s(\omega_L t)$ can be obtained

$$i_s(\omega_L t) = i_{sRef}(\omega_L t) = K_1 \cdot \hat{V}_S \sin(\omega_L t) \cdot v_c(\omega_L t) \quad (1)$$

The controlled signal $v_c(\omega_L t)$ composes of DC Component V_{CDC} and AC Component $v_{cAC}(\omega_L t)$, ripple in voltage loop. So the $v_c(\omega_L t)$ can be obtained

$$v_c(\omega_L t) = V_{CDC} + v_{cAC}(\omega_L t) \quad (2)$$

As described earlier, it is known that the $\hat{I}_{sRef}$ has twice of line frequency, thus the $v_{cAC}(\omega_L t)$ can be supposed

$$v_{cAC}(\omega_L t) = \hat{V}_{CAC} \sin(2\omega_L t - \phi) \quad (3)$$

Substituting (2) and (3) into (1), then the $i_s(\omega_L t)$ can be obtained

$$i_s(\omega_L t) = K_1 \cdot \hat{V}_S \sin(\omega_L t) \cdot \left[V_{CDC} + \hat{V}_{CAC} \sin(2\omega_L t - \phi) \right] \tag{4}$$

An instantaneous input power $p_s(\omega_L t)$ can be written $p_s(\omega_L t) = i_s(\omega_L t) \cdot v_s(\omega_L t)$, substituting input voltage $v_s(\omega_L t)$ and input current $i_s(\omega_L t)$ from (1) into it, then instantaneous input power can be rearranged

$$p_s(\omega_L t) = V_{CDC} K_1 \hat{V}_S^2 \cdot \sin^2(\omega_L t) \cdot \left[1 + k \sin(2\omega_L t - \phi) \right] \tag{5}$$

$$\text{By } k = \frac{\hat{V}_{CAC}}{V_{CDC}} \tag{6}$$

Where k is the ratio between peak of controlled signal and DC component of controlled signal, ϕ is a phase lag angle defined from Figure 1(b), K_1 is per-unit scaling gain for voltage value (K_1=1/V_B) and V_B is base voltage value scaled for K_1. An average input power (P_{SAVG}) can be derived from the averaging value in period of the instantaneous input power in (5), and then it can be obtain

$$P_{SAVG} = \frac{\omega}{2\pi} \int_0^{2\pi/\omega} p_s(\omega_L t) dt = \frac{V_{CDC} K_1 \hat{V}_S^2}{4} \cdot \left[2 + k \sin(\phi) \right] \tag{7}$$

An average output power (P_{OAVG}) is the power appearing at the output resistive load and can be expressed as

$$p_{OAVG} = \frac{V_{ODC}^2}{R_{Load}} \tag{8}$$

From the power balanced technique, the average output power (P_{OAVG}) as (8) is equal to the average input power (P_{SAVG}) as (7) then the DC component of controlled voltage (V_{CDC}) can be expressed as

$$V_{CDC} = \frac{4 \cdot V_{ODC}^2}{K_1 R_{Load} \hat{V}_S^2 \left[2 + k \sin(\phi) \right]} \tag{9}$$

Where V_{ODC} is the average output voltage. From this expression, replace V_{ODC} in (4) and rearrange by using trigonometric identities, then the input current can be expressed as

$$i_s(\omega_L t) = \frac{4 V_{ODC}^2}{R_{Load} \hat{V}_S (2 + k \sin\phi)} \cdot \left[\underbrace{\sin(\omega_L t) + \frac{k}{2} \cos(\omega_L t - \phi)}_{\text{1st harmonic}} - \underbrace{\frac{k}{2} \cos(3\omega_L t - \phi)}_{\text{3rd harmonic}} \right] \tag{10}$$

Where

$$i_s(\omega_L t) = i_{s1}(\omega_L t) + i_{s3}(\omega_L t) \tag{11}$$

$$i_{s1}(\omega_L t) = \frac{4 V_{ODC}^2}{R_{Load} \hat{V}_S (2 + k \sin\phi)} \cdot \left[\sin(\omega_L t) + \frac{k}{2} \cos(\omega_L t - \phi) \right] \tag{12}$$

$$i_{s3}(\omega_L t) = \frac{2 V_{ODC}^2}{R_{Load} \hat{V}_S (2 + k \sin\phi)} \cdot \left[k \cos(3\omega_L t - \phi) \right] \tag{13}$$

Where $i_s(\omega_L t)$ is the input current, $i_{s1}(\omega_L t)$ is the 1st harmonic content of input current, $i_{s3}(\omega_L t)$ is the 3rd harmonic content of input current and R_{Load} is resistive load at output.

As the 2nd harmonic content of $v_c(\omega_L t)$ in (3) is transformed into the 3rd harmonic of the input current in (11) and (11). The input current $i_s(\omega_L t)$ consists of two terms, fundamental current $i_{s1}(\omega_L t)$ and the 3rd harmonics current $i_{s3}(\omega_L t)$ which is the main cause of the distortion of input current. If the term $i_{s3}(\omega_L t)$ can be eliminated from $i_s(\omega_L t)$, then the input current will remain only the fundamental component. Therefore, the input current will be sinusoidal.

2.2. The Output Current

An instantaneous output power (p_o) at the output voltage can be obtain

$$p_o(\omega_L t) = i_o(\omega_L t) \cdot v_o(\omega_L t) \tag{14}$$

From the power balanced technique, the instantaneous output power (p_o) as equation reference goes here is equal to the instantaneous input power (p_s) in (5), then assume the output capacitor is bulk. Therefore, the output voltage ($v_o(\omega_L t)$) will only be DC component (V_{ODC}) then the input current ($i_o(\omega_L t)$) will expresses as

$$i_o(\omega_L t) \cdot = \frac{V_{CDC} K_1 \hat{V}_S^{\,2}}{V_{ODC}} \cdot \sin^2(\omega_L t) \cdot \left[1 + k \sin(2\omega_L t - \phi)\right] \tag{15}$$

From this expression, replace V_{CDC} by (9) and rearrange by using trigonometric identities, then the output current can be expressed as

$$i_o(\omega_L t) \cdot = \frac{4V_{ODC}}{R_{Load}(2 + k\sin\phi)} \cdot \left[\underbrace{\frac{1}{2} - \frac{k}{4}\sin\phi}_{DC} - \underbrace{\frac{1}{2}\cos(2\omega_L t) + \frac{k}{2}\sin(2\omega_L t - \phi)}_{2\text{nd harmonic}} - \underbrace{\frac{k}{4}\sin(4\omega_L t - \phi)}_{4\text{th harmonic}} \right] \tag{16}$$

Where

$$i_o(\omega_L t) = I_{ODC} + i_{o2}(\omega_L t) + i_{o4}(\omega_L t) \tag{17}$$

And

$$I_{ODC} = \frac{V_{ODC}}{R_{Load}} \tag{18}$$

$$i_{o2}(\omega_L t) = \frac{2V_{ODC}}{R_{Load}(2 + k\sin\phi)} \cdot \left[k\sin(2\omega_L t - \phi) - \cos(2\omega_L t) \right] \tag{19}$$

$$i_{o4}(\omega_L t) \cdot = \frac{-V_{ODC}}{R_{Load}(2 + k\sin\phi)} \cdot \left[k\sin(4\omega_L t - \phi) \right] \tag{20}$$

Where I_{ODC} is DC component of output current, $i_{o2}(\omega_L t)$ is 2nd harmonics content of output current and $i_{o4}(\omega_L t)$ is 4th harmonics content of output current.

2.3. The Output Voltage

The output voltage is obtained from the multiplication of the output current (16) by the output impedance that is capacitive reactance is parallelled with resistance load. The capacitive reactance will mainly involve the AC component due to lower impedance than the resisitive load; therefore, the components $i_{o2}(\omega_L t)$ and $i_{o4}(\omega_L t)$ are considered to flow through the output capacitor. At the same time, The DC component I_{ODC} is considered to flow through the resistive load. Thus, the 2nd and 4th harmonics content of output voltage ($v_{o2,4}(\omega_L t)$) can be written as

$$v_{o2,4}(\omega_L t) = i_{o2,4}(\omega_L t) \cdot x_{c2,4\omega L} \tag{21}$$

From this expression, substituting the output current $i_{o2}(\omega_L t)$ and $i_{o4}(\omega_L t)$ from (19) and (20) respectively, then the output voltage $v_{o2}(\omega_L t)$ and $v_{o4}(\omega_L t)$ can be expressed as

$$v_{o2}(\omega_L t) = \frac{2V_{ODC}}{2\omega_L CR_{Load}(2+k\sin\phi)} \cdot \left[-k\cos(2\omega_L t-\phi) - \sin\left(2\omega_L t\right)\right] \tag{22}$$

$$v_{o4}(\omega_L t) = \frac{2V_{ODC}}{2\omega_L CR_{Load}(2+k\sin\phi)} \cdot \left[\frac{k}{4}\cos(4\omega_L t-\phi)\right] \tag{23}$$

Thus, the output voltage ($v_o(\omega_L t)$) will be written as

$$v_o(\omega_L t) = V_{ODC} + \underbrace{v_{o2}(\omega_L t) + v_{o4}(\omega_L t)}_{v_{oAC}(\omega_L t)} \tag{24}$$

Where V_{ODC} is average output voltage, $v_{o2}(\omega_L t)$ is 2nd harmonics content of output voltage and $v_{o4}(\omega_L t)$ is 4th harmonics content of output voltage.

$$v_o(\omega_L t) = V_{ODC} + \frac{2V_{ODC}}{2\omega_L CR_{Load}(2+k\sin\phi)} \cdot \left[-k\cos(2\omega_L t-\phi) - \sin\left(2\omega_L t\right) + \frac{k}{4}\cos(4\omega_L t-\phi)\right] \tag{25}$$

The output voltage is described by (25) is composed of DC component (V_{ODC}) and AC component ($v_{oAC}(\omega_L t)$) which is the output ripple voltage. This ripple is sensed into voltage loop and cause the input current distortion. In the case of the k equal to zero (k=0), the Equation (25) will be written as

$$v_o(\omega_L t)\big|_{k=0} = V_{ODC} + \underbrace{\frac{V_{ODC}}{2\omega_L CR_{Load}} \cdot \sin 2\omega_L t}_{v_{o2}(\omega_L t)} \tag{26}$$

If k is controlled to be zero, then the AC component disappears in the outer loop.

3. THE REDUCTION OF RIPPLE VOLTAGE IN THE VOLTAGE LOOP

To get rid of the harmonic content of the input current, the ripple voltage in voltage loop must be eliminated. In this section, a simplifly technique to reduce those ripples is presented. The proposed technique is to generate the estimated-ripple voltage from the ripple voltage estimator (RVE) in order to cancel the sensed-ripple voltage.

The v_{oAC} ($\omega_L t$) from (24) use for estimating the estimated-ripple voltage, but in practical, there are three parameters can neglect. Firstly, the AC component v_{o4} ($\omega_L t$) is not appeared into voltage loop, because there is a LPF at the output voltage loop. The others, there are scanty value of the phase lag angle (ϕ) and the k. As a result, the ripple output voltage which is sensed into voltage loop only remain the v_{o2} ($\omega_L t$). Therefore, the estimated-ripple voltage (v_{RVE}) can be written as

$$v_{RVE} = K_1 v_{o2}(\omega_L t)\big|_{\phi=0} = -\frac{K_1}{2\omega_L C} \cdot \frac{V_{ODC}}{R_{Load}} \cdot \sin 2\omega_L t = G_{RVE} I_{ODC} \sin 2\omega_L t \tag{27}$$

Where v_{RVE} is the estimated-ripple voltage and G_{RVE} is the Ripple Voltage Estimator transfer function

4. TRANSFER FUNCTION OF THE SYSTEM AND CONTROLLER DESIGNED

An analysis of the Single-phase AC-DC converter transfer function is presented under the continous conductiontion mode of operation. The transfer function is used for designing voltage controller. As the analysis for transfer function model, there are no AC component $v_{o2}(\omega_L t)$ and $v_{o4}(\omega_L t)$ at the output voltage. Thus from (16), select only DC component and let k=0, the output current is (28).

$$I_{ODC}\big|_{k=0} = \frac{V_{CDC} K_1 \hat{V}_S^{\,2}}{2V_{ODC}} \tag{28}$$

Applying perturbation in it to perform the small-signal approximation. Therefore, the output current can be expressed as

$$\tilde{I}_{ODC} = \frac{\partial I_{ODC}}{\partial V_{CDC}} \tilde{V}_{CDC} + \frac{\partial I_{ODC}}{\partial V_{ODC}} \tilde{V}_{ODC} \tag{29}$$

Since the voltage source converter transfer function (G_{VSC}) and Disturbance transfer function (G_D) can be define as

$$\frac{\partial I_{ODC}}{\partial V_{CDC}} = \frac{\hat{V}_S^{\,2} K_1}{2V_{ODC}} = G_{VSC} \text{ and } \frac{\partial I_{ODC}}{\partial V_{ODC}} = \frac{-\hat{V}_S^{\,2} V_{CDC} K_1}{2(V_{ODC})^2} = \frac{-1}{R_{Load}} = G_D \tag{30}$$

The notation used in this section to describe the quantities. From (29), the variables with the sign '~' are the small signal values.The output impedance (G_Z) can be define as

$$G_Z(s) = \frac{\tilde{V}_{ODC}}{\tilde{I}_{ODC}} = \frac{R_{Load}}{1 + R_{Load} Cs} \tag{31}$$

Since the controller in the current loop, hysteresis controller, is selected, the dynamic response of input current is fast enough to track the reference value of the input current. Thus, the transfer function of closed current loop can be approximated as $\hat{I}_S$. In order to design voltage controller for the next issue, then the closed-loop system block diagram is obtained from (29), (30) and (31) shown in Figure 3(a). To avoid line current distortion in the VSC, the system crossover frequency in the voltage loop should be between 10-20 Hz (50 Hz line frequency) [4]. According to the low crossover frequency, the transient response of the PFC circuit is limited especially under the step-load condition. In the case of voltage and current are been the per-unit system, the plant transfer function (the voltage controller is not included) can be written

$$G_P(s) = \underbrace{K_1}_{\substack{P.U \\ Gain}} \cdot \underbrace{G_{LPF}(s)}_{\substack{Low \\ Pass \\ Filter}} \cdot \underbrace{\hat{I}_S}_{\substack{Current \\ Control \\ Loop}} \cdot G_{VSC} \cdot G_Z(s) \tag{32}$$

Where $\hat{I}_S$ is peak input current and $\hat{V}_S$ is peak input voltage. The Open-Loop Transfer Function (OLTF) can be written as

$$OLTF(s) = G_{CV}(s) \cdot G_P(s) \tag{33}$$

Where the GCV(s) is voltage controller, PI controller, can be obtained as

$$G_{CV}(s) = K_P + \frac{K_I}{s} \tag{34}$$

Where K_P is proportional gain and K_I is integral gain. The procedure for designing $G_{CV}(s)$, first, select the phase margin ϕ_m and crossover frequency f_c by $\omega_c = 2\pi f_c$. Then calculate the θ by substituting them into Equation (35). Finally, K_P and K_I will be obtained by (36).

$$\theta = -180° + \frac{\pi}{180°}\phi_m - \angle G_P(j\omega_c) \tag{35}$$

$$K_P = \frac{\cos\theta}{|OLTF(j\omega_c)|} \text{ and } K_I = \frac{(\sin\theta)\cdot 2\pi f_c}{|OLTF(j\omega_c)|} \tag{36}$$

The stability of proposed system is described by the frequency response analysis. The output voltage control loop designed must guarantee the stability and provide enough bandwidth in all possible operation conditions of the system. The bode plots in Figure 3(b) used as the tool for the frequency response analysis composing of amplitude and phase of the system. After the analog PI controller design is finished, the parameters are used to calculate the control signal of the eZdspLF2407 DSP by (37)

$$u(n) = K_P \cdot e(n) + K_I \cdot T_s \sum_{k=1}^{n} e(n) \tag{37}$$

Where u(n) is the output control signal of the digital controller, e(n) is an error signal and Ts is a sampling time period.

5. FEED-FORWARD COMPENSATION OF VSC

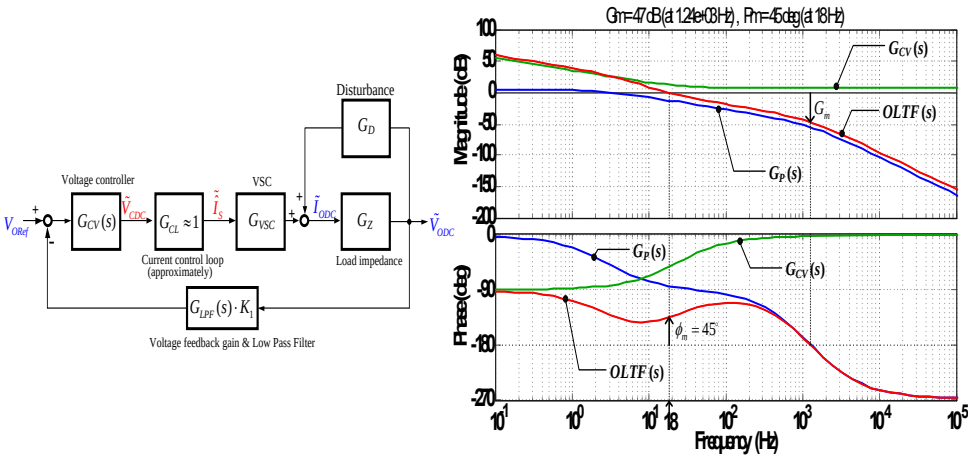
In order to more increase the responsibility of the output voltage, the disturbance rejection technique applied in the VSC is presented. The concept of it, the disturbance which is the load current is measured and fed before it has time to affect the converter. This known as the feed-forward compensation, since Feed-Forward Current (I_{FFC}) which is related disturbance ($D(s)$) and Feed-Forward Gain ($G_{FFC}(s)$) can be written as :

$$I_{FFC}(s) = D(s)G_{FFC}(s) \tag{38}$$

and Feed-Forward Gain ($G_{FFC}(s)$) can be written as

$$G_{FFC} = \frac{G_D}{G_{VSC}} = -\frac{2V_{ODC}}{R_{Load}\hat{V}_S^{\,2}K_1} \text{ and } D(s) = \tilde{V}_{ODC} \tag{39}$$

Therefore, bring (38) and (39) obtain the block diagram for FFC as shown in Figure 4



(a) (b)

Figure 3. (a) Transfer function of system. (b) Frequency response of system

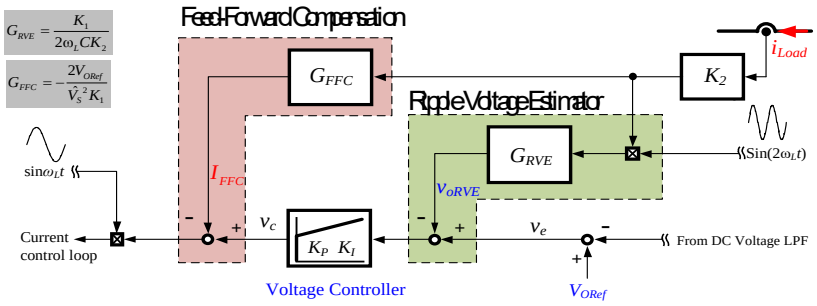
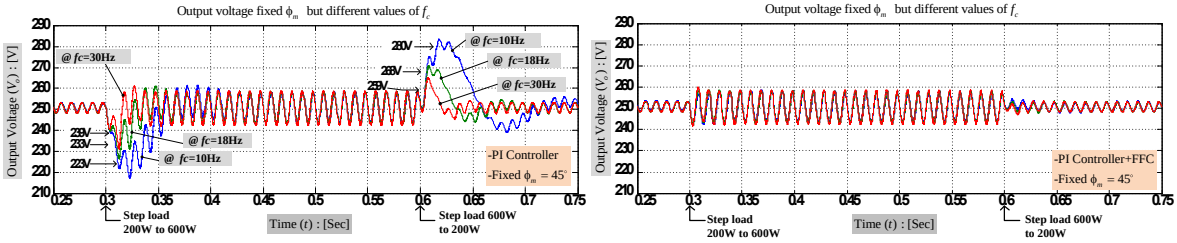


Figure 4. The proposed technique consists of the RVE and FFC

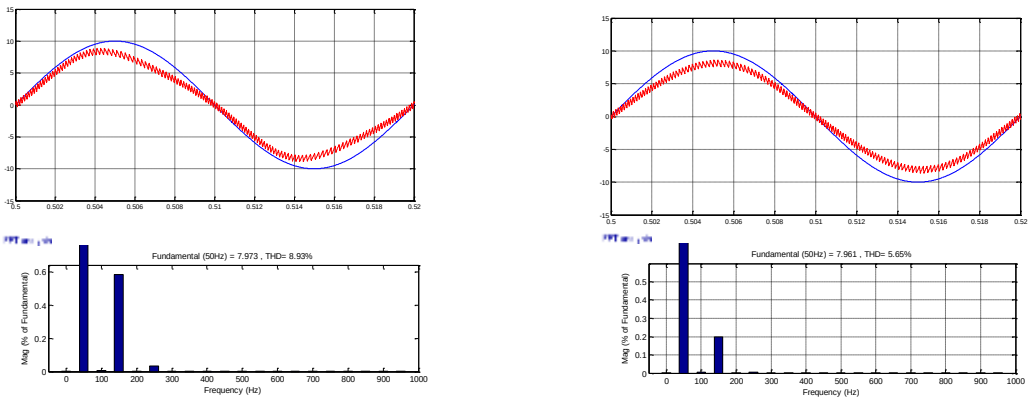
Table 1. Parameters of the proposed system

Parameters	Values
V_S, f_{Line}	110 Vrms, 50 Hz
V_{ORef}	250 Vdc
L,C	15 mH, 560 µF
P_{oMax}	600 W



(a) (b)

Figure 5. The dynamic-interval simulation results of v_o when the f_c is changed by 10Hz, 18Hz and 30Hz: (a) The conventional control. (b) The conventional control with proposed technique.



(a) (b)

Figure 6. The input current and its total harmonic distortion (THDi) at 600W of the static-simulation results: (a) The conventional control. (b) the conventional control with proposed technique

6. CIRCUIT SIMULATIONS

In this section, the simulation of the VSC is discussed. The configuration of which is simulated by SIMULINK program. The purpose of this simulation is to test the parameter of controllers, verify the control algorithms, and study the static and the dynamic of the proposed system. The simulation methods are the conventional control (PI controller) and the conventional control with proposed techniques (PI controller

with the RVE and FFC technique).The important parameters of which are shown in Table 1. The parameters of PI controller, K_P and K_I, is set by fixed ϕ_m at 45° and selected f_c at 10Hz, 18Hz and 30Hz.

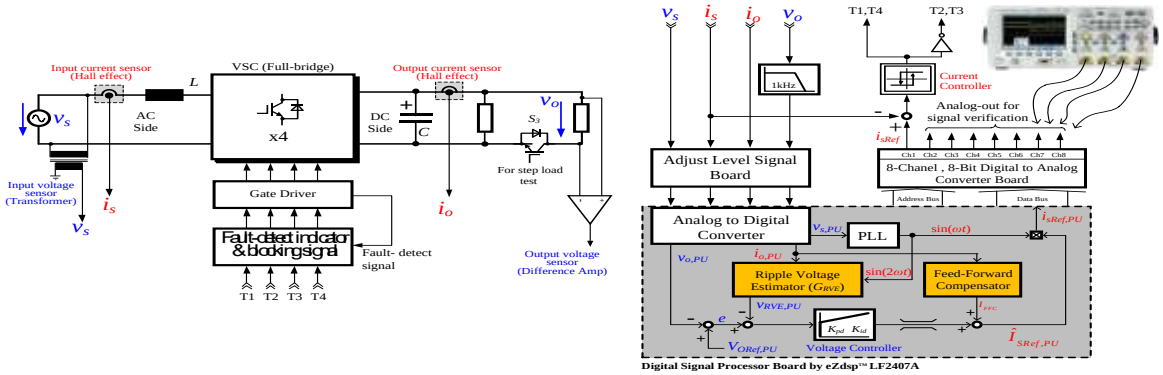
In Figure , the dynamic-interval simulation results of v_o when the f_c is changed by 10Hz, 18Hz and 30Hz will be compared between conventional control in Figure (a) and conventional control with proposed techniques in Figure (b). In Figure (a) shows the capability of responsibility when the load is immediately changed from 200W to 600W at 0.3s and stepped back to 200W at 0.6s. The value f_c at 18Hz provides the responsibility of v_o is faster than f_c at 10Hz while the value f_c at 30Hz is faster than f_c at 18Hz. As Figure (b), when the load is immediately changed the responsibility of v_o is hardly changed. It is shown that the feed-forward gain of proposed technique is capable of offering the fastest dynamical response.

In Figure (a) and Figure (b) show static-interval simulation results, the main aims of this simulation are to show the i_s waveform and its THDi at rated power 600W. For the conventional control, the i_s waveform and its THDi=8.93% shown in Figure (a). For the conventional control with proposed technique, the i_s waveform and its THDi=5.65% Figure (b). This indicated that the i_s waveform of the conventional control with RVE technique is improved to nearby sinusoidal waveform. Obviously, the FFC technique can improves the speed of dynamic response and the voltage loop and the RVE technique can improves static to almost sinusoidal better than conventional control.

EXPERIMENTAL PROTOTYPE.Error! Reference source not found. In Figure 7, an experimental prototype based on the design parameters mentioned in the above section is built and tested. The structure of prototype composes of a power section and a control section. In Figure 7(a), the VSC built from 4 IGBTs is driven by gate-drive circuit having fault-protection option. In order to isolate between power and control section, the transducer device using magnetic effect have been used as sensors. The input current and DC output current use hall-effect current sensor; the input voltage uses step-down transformer, and the output voltage is sensed by a differential amplifier built from OPAMPs.

In Figure 7(b), two control strategies were implemented on a eZdspLF2407 to control the VSC for performance comparison purposes. The implemented control methods in the experiment are the conventional control (PI controller) and the conventional control with proposed techniques (PI controller with the RVE and FFC technique). The PI controller parameters of these control methods were designed so that the phase margin (ϕ_m) of the compensated system was 45◦ with the 8Hz-18Hz crossover frequency. For every control algorithms in the experiment, the sampling time period was set at 200 µs.

The testing of dynamic interval will be compared between the conventional control in Figure (a) and the proposed technique in Figure 8(b). The configurations of PI controller are set by the same parameter as the dynamic simulation that is select ϕ_m at 45° and f_c at 18Hz. Figure 8 show the test dynamic results monitored from oscilloscope. There are the value of peak reference input current $\hat{I}_{sRef}$ or controlled-signal v_c (CH3), the input current i_s (CH4), the output voltage v_o (CH2), and the load current i_o (CH1). When the load is stepped from 200W to 600W, the i_o will be step from 0.8A to 2.4A. The v_o of the conventional control in Figure 8(a) is drooped 16V and settling time 60ms, while the v_o of the proposed technique in Figure 8(b) is drooped 10V and settling time 50ms. It is shown that, although f_c at 18Hz gives good dynamical response, the proposed technique can offer the better dynamical response of output voltage than the conventional control.



(a) (b)

Figure 7. The experimental prototype: (a) power section. (b) Control section

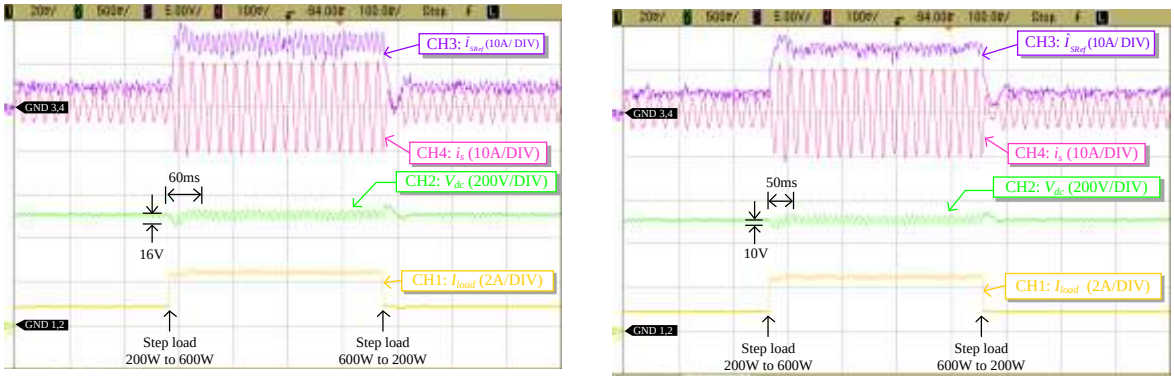


Figure 8. The dynamic-interval testing results for: (a) the conventional control. (b) The conventional control with proposed technique

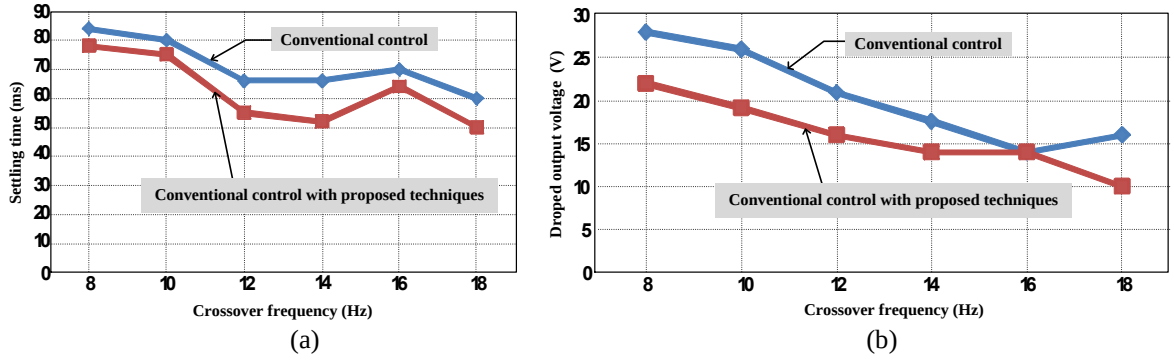


Figure 9. The dynamic-interval testing results: (a) the settling time versus crossover frequency. (b) The dropped voltage of output voltage versus crossover frequency

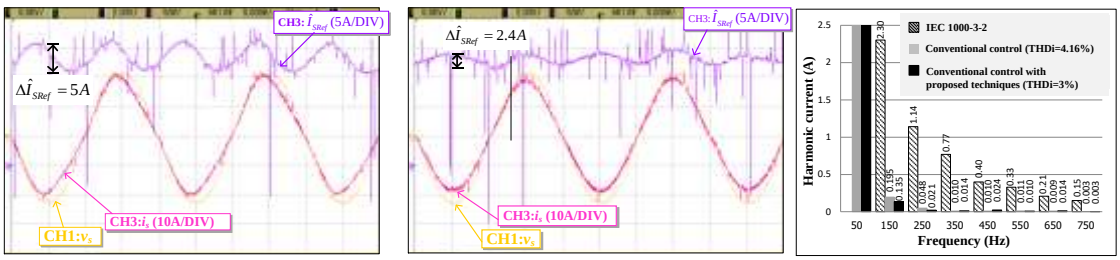


Figure 10. The static-interval testing results for: (a) the conventional control (b) The conventional control with the proposed technique (c) The THDi

In Figure 9 will be continued testing from early, but the testing of difference crossover frequency from 8Hz to 18Hz are added. Figure 9(a) shows the settling time and Figure 9(b) shows the dropped voltage. Both of the results compare the conventional control with the proposed technique. It is shown that the FFC gain of proposed technique is capable of offering better dynamical response than the conventional control in almost every f_c.

In Figure 10 present the static-interval testing results. The output power was carried out by connecting a DC load which is set at rated power 600W. The results are focus on the waveforms of the i_s indicated with THDi value as shown in what is similar to the sinusoidal waveform. In addition, the waveform of the $\hat{I}_{sRef}$ will be presented in order to show the effective reducing the ripple voltage in voltage loop. For the conventional control without RVE technique, Figure 10(a) presents the $\hat{I}_{sRef}$ waveform of which $\Delta\hat{I}_{sRef}$

=5A and the i_s waveform of which the THDi=4.16% as shown in Figure 10(c). For the proposed technique, Figure 10(b) presents the $\hat{I}_{sRef}$ waveform of which $\Delta\hat{I}_{sRef}$ is improved to 2.4A. As the result, the i_s waveform of which the THDi as shown in Figure 10(c) is improved to 3% and remain under the IEC 1000-3-2.

In Figure presents the key performance in case of relation of THDi versus difference the output power by varying difference the crossover frequency, in Figure 11(a) is the result of the conventional control, in Figure 11(b) is the result of the proposed technique. Though the high-crossover frequency will give good dynamic response, high THDi is occurred. Moreover, the THDi is quite constant every f_c when the output power is increased. The main point of difference, The THDi of proposed technique in Figure 11(b) is lower than 5% every f_c.

In Figure 12(a) presents the performance of system which is presented in case of input power factor versus difference output power. It achieves a high-power factor considerated nearly unity. The efficiency versus difference output power in Figure 12(b) indicates the overall efficiency over 85%.

7. CONCLUSION

The analysis of the ripple in voltage loop and control design of the VSC converter built from full-bridge circuit is presented. The ripple causes the 3rd harmonic in the input current, and then the input current is distorted. The proposed control composes of two algorithm techniques, The RVE technique which is the simple method can reduce the 3rd harmonic of the input current and hence the THDi is improved. Moreover, the crossover frequency high value can offer the good dynamical response; however, the FFC technique can achieve the better than. The sensed-load current is used in the FFC technique and the RVE technique. The control algorithm was implemented on the eZdspLF2407DSP and was tested. As a result, the proposed control is achieved quite well for the THDi is <5%. The output voltage regulation is the better both the transient response and the steady state. The overall performances of the system are obtained as follows: the power factor at a full load is >0.98, the harmonic distortion at AC input power source of the converter is under control in IEC61000-3-2 class A limit, and the overall efficiency >85%.

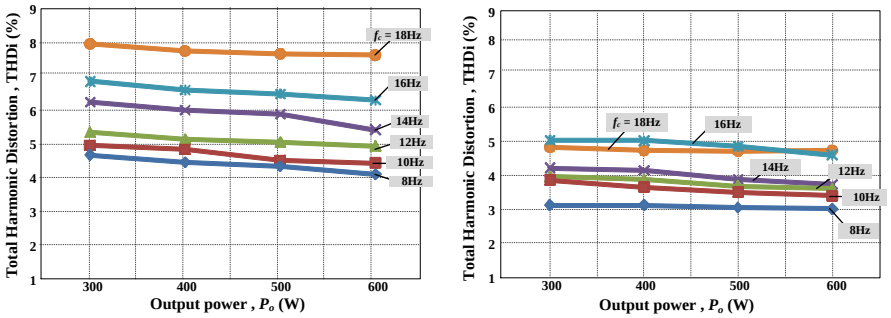


Figure 11. The relation of THDi versus difference output power by varying difference crossover frequency of: (a) the conventional control. (b) the conventional control with proposed technique.

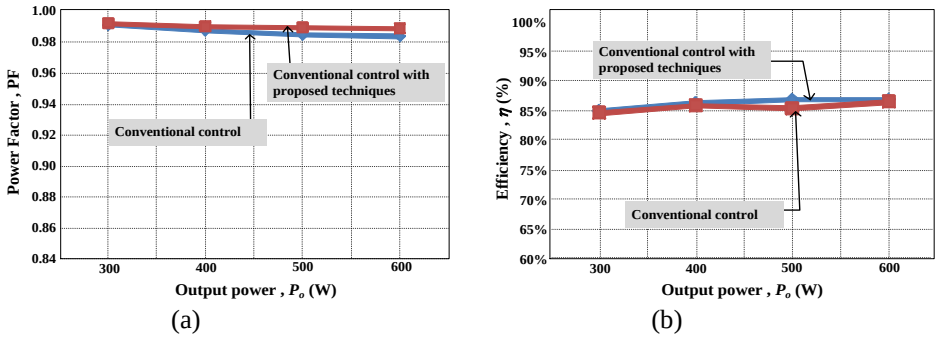


Figure 12. Test result of: (a) the output power versus the power factor. (b) the output power versus efficiency

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