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Effects of Switching Frequency Modulation on Input Power Quality of Boost Power Factor Correction Converter

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ABSTRACT

Switching frequency modulation (SFM) as spread-spectrum technique has been used for electromagnetic interference reduction in switching power converters. In this paper, a switching-frequency-modulated boost power factor correction (PFC) converter operating in continuous conduction mode is analysed in detail in terms of its input power quality. Initially, the effect of SFM on the input current total harmonic distortion, power factor and low-frequency harmonics of the PFC converter are studied by using computer simulations. Some advices on choosing parameters of SFM are given. Then the theoretical results are verified experimentally. It is shown that, from a power quality point of view, SFM can be harmful (it can significantly worsen the power quality of the PFC converter) or almost harmless. The results depend on how properly the modulation parameters are selected.

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1. INTRODUCTION

Nowadays, switched-mode power supplies (SMPS) are very popular for efficient electric power conversion in electronic equipment. A conventional AC-mains-connected SMPS usually has a full-wave diode rectifier with a large capacitive output filter. This results in significant AC line current (which in an ideal case should be sinusoidal) distortion and, consequently, noticeable degradation of the input power quality (PQ) of the SMPS [1]-[2]. Poor power quality can lead not only to ineffective utilisation of the electrical grid but can also cause damage to electronic equipment [1]-[4]. The main parameters characterizing power quality are the power factor (PF) and total harmonic distortion (THD) of the input current [5]. PF, by definition, is the real power P_{real} ratio to apparent power P_{app}

$$PF = P_{real}/P_{app} = P_{real}/(V_{inrms} \cdot I_{inrms}), \quad (1)$$

where V_{inrms} and I_{inrms} are the input voltage and current RMS values, respectively. The PF is the function of phase angle φ between input voltage and current fundamental harmonics as well as the THD of the input current [5]

$$PF = \frac{\cos(\varphi)}{\sqrt{1+THD^2}} \quad . \quad (2)$$

As the THD of the SMPS input current increases, PF decreases, leading to degradation of input PQ. In an ideal case, input voltage is in phase with input current and is purely sinusoidal, so it has only one spectrum component at the mains frequency (f_{mains}). In a real case, the input AC current is distorted and the harmonics of f_{mains} appear in its spectrum. By definition, the THD of the SMPS input current is as follows

$$\mathrm{THD}=\sqrt{\sum_{m=2}^{M}\frac{I_m^2}{I_1^2}} \quad , \tag{3}$$

where I_m is the amplitude of the input current m-th harmonic; I_1 is the input current fundamental harmonic amplitude (at f_{mains}); M is an integer whose value depends on PQ international standards requirements. For example, according to IEC 1000-3-2, the low-frequency harmonics should be measured up to M = 40. Thus, if f_{mains} = 50 Hz, then the PQ analyser measures harmonics up to f_{max} = 2 kHz.

It is interesting to note that international PQ standards are usually more concerned not with THD and PF but with the low-frequency content of the input current. When performing compliance measurements in order to meet standard requirements, SMPS input current harmonics must be lower than the maximally permissible values set by the standard. For example, per IEC 1000-3-2 for class-D equipment, low-frequency harmonics (the RMS values of odd harmonics) must be lower than 3.4 mA/W for the 3rd harmonic, 1.9 mA/W for the 5th harmonic, 1 mA/W for the 7th harmonic, 0.5 mA/W for the 9th harmonic, and 3.85/m mA/W for $11 \le m \le 39$ [6].

To reduce the THD of the SMPS input current and improve the PF, usually active power factor correction (PFC) converters are used [7] – [10]. Although active PFC converters are very useful for improving the PQ, the PFC converters are switched-mode in nature and are therefore major sources of electromagnetic interference (EMI). Reduction of conducted EMI can be achieved by using EMI suppression filters, snubbers, proper design of printed circuit boards, soft-switching techniques, interleaving, spread-spectrum technique, etc. [10] – [15]. In fact, the spread-spectrum technique has become very popular technique for SMPS EMI reduction in the scientific community owing to its good EMI reduction potential along with easiness of implementation and adding little or no additional cost to SMPS [12], [14], [16] – [19]. Spreading the spectrum of SMPS voltages and currents and EMI noise reduction (Figure 1) can be achieved by modulating one of the pulse-width-modulated (PWM) control signal parameters such as the pulse position [20], duty ratio [21], or frequency [22].

Periodic switching frequency modulation (SFM) is often used in practical designs because it has some important advantages over other spread-spectrum techniques [22]-[24]. Similarly to other EMI reduction techniques, SFM also has some disadvantages: it can increase output voltage and input current ripples of SMPS, as well as worsen the PQ of PFC converters and resonant inverters for induction heating appliances [16], [19], [22]-[28].

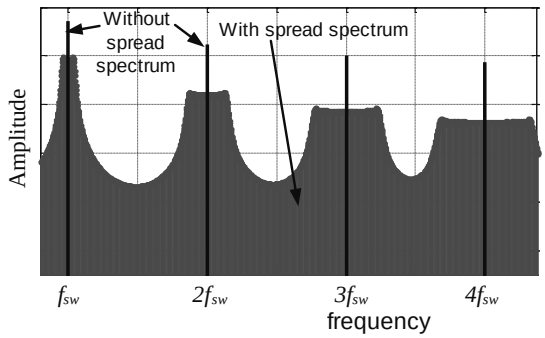


Figure 1. Spectra of SMPS input current before and after the use of spread-spectrum technique

PFC converters can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). PFC converters are designed to operate in DCM for low-power applications, but in CCM for mid- or high-power applications. A comrehensive study of the effect of SFM on the PQ of flyback PFC converters operating in DCM was presented in [16]. An improved control method to reduce the THD of input current and improve PF of DCM PFC converters with SFM was proposed in [16]. Despite the fact, that the effect of SFM on PQ of PFC converters operating in DCM is examined very well, there are only few

papers [22], [23] considering the effect of SFM on the PQ of PFC converters operating in CCM. In [22]-[23] some experimental results are presented showing that the THD of input current of boost CCM PFC converter increases owing to use of SFM. However, the study presented in the papers is purely experimentally based, has some ambiguities and is not comprehensive, nor does it explain how the choice of SFM parameters affects CCM boost PFC input current THD and low-frequency content. Moreover causes of worsening PQ owing to use of SFM are not revealed in the papers. This paper focuses on this issue. The main new research in this paper is an original analysis of the effect of SFM on boost PFC converter input current low-frequency content, THD, and the power factor. This paper also includes detailed description of SIMULINK model, thorough experimental verification of the simulation results and some advice on choosing SFM parameters.
This paper is organized as follows. In Section 2, operating principle of boost PFC converter is presented. In Section 3, SIMULINK model of the boost PFC converter is explained in details. In Section 4, a rigorous theoretical analysis of the effect of SFM parameters on input current low-frequency harmonics and THD is presented. Causes of the increase in THD are revealed. Additionally, a summary of the analysis and some practical advice for choosing effective SFM parameters are given at the end of Section 4. Section 5 presents a deep experimental study of the PQ of the SFM PFC converter and verifies the simulation results.

2. BOOST PFC CONVERTER OPERATING PRINNCIPLE

Boost converter operating in CCM is very popular for power factor correction when power levels exceed 300W [7], [8], [29]. There are two control methods of boost CCM PFC converters: peak current control and average current control methods. The latter much more often used in practical PFC converters because of higher immunity to noises [30]. Simplified schematic diagramm of the boost PFC converter with average current control is shown in Figure 2. It consists of boost power stage and two control loops: input current and output voltage control loops. In order to get high PF and low THD, averaged input current must be in phase with input voltage and it must have the same shape as input voltage. Therefore, the main purpose of the current control loop is to compare PFC input current waveform with PFC input voltage waveform in order for the input current waveform to follow the input voltage waveform [30]. Input current controller consits of current error amplifier with compensation network (R_5, R_6, C_2, C_3), multiplier and input current sense resistor R_s. Current control loop has much wider bandwidth than voltage control loop. The multiplier could be considered as programmable current source with output current proportional to the divider output voltage and scaled rectified input voltage (voltage across resistor R_2) [31]. The voltage across the current sense resistor R_s (which is proportional to the PFC converter rectified input current) is subtracted from the voltage across R_4 (which is proportional to the multiplier output current and therefore, to the scaled rectified input voltage) and then it is amplified with the current error amplifier. The pulse width modulator (PWM) then creates rectangular control signal with variable duty cycle in order to shape the input current.

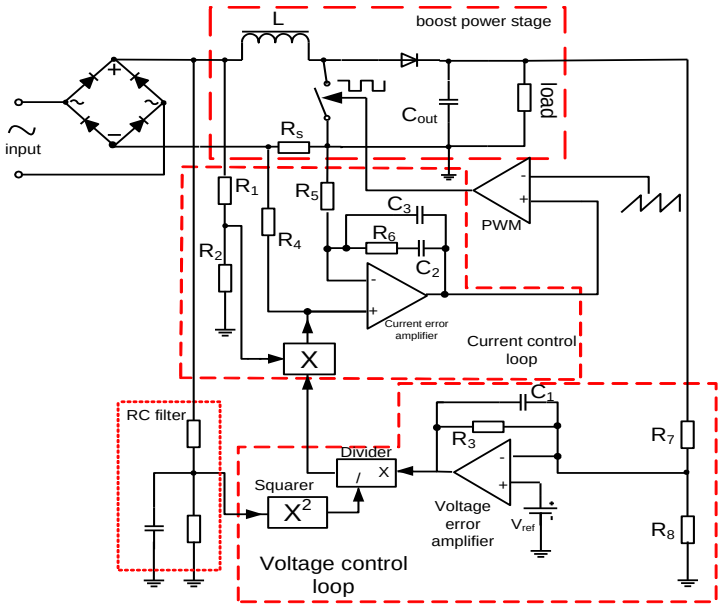


Figure 2. Simplified schematic diagramm of the boost PFC converter

Output voltage controller is neccessary in order to get regulated output voltage. It consists of voltage error amplifier with compensation network (R_3, R_7, C_1), squarer, divider, RC filter and reference voltage source. Voltage control loop usually has much narrower bandwidth than current control loop, because crossofer frequency of the loop must be much lower than twice mains frequency (f_{mains}) in order for the input current distortion to be low [31]. Usually crossover frequency of the voltage control loop is chosen to be about 10 Hz [31]. Output voltage of the RC filter (which, in fact, is DC voltage with very small AC ripples) is proportional to PFC converter input voltage amplitude V_{inm}. Squarer, divider, RC filter and multiplier are necessary in order for the voltage control loop gain to be independent on PFC boost converter input voltage amplitude.

3. DESCRIPTION OF BOOST PFC SIMULINK MODEL

For the analysis SIMULINK model of the boost PFC converter is created and explained. The model (Figure 3) can be used for simulation of boost PFC converter with and without SFM. The model is partly based on the schematic diagramm shown in Figure 2 with some simplifications. In order for simulation results to be comparable with experimental results, values of power inductors' inductance, output capacitor's capacitance as well as numerical values of coefficients of SIMULINK block transfer functions are calculated based on 360W boost PFC converter desribed in [31].

In the model parasitic equivalent series resistances of output capacitor and power inductor are taken into account. However the inductor is assumed to be linear. In order to take into account real power MOSFET and its control circuit (including PWM) turn-on switching delays (t_{don}) and turn-of switching delays (t_{doff}) (which in fact can have major influence on low-frequency content of switching-frequency modulated dc/dc power converetrs voltages [16],[19],[32]-[33]), turn-on and turn-off delay blocks consisting of two "Transport Delay" blocks, logic operators AND and OR are added to the model (Figure 3). Using that blocks we can independently enter t_{don} and t_{doff} values.

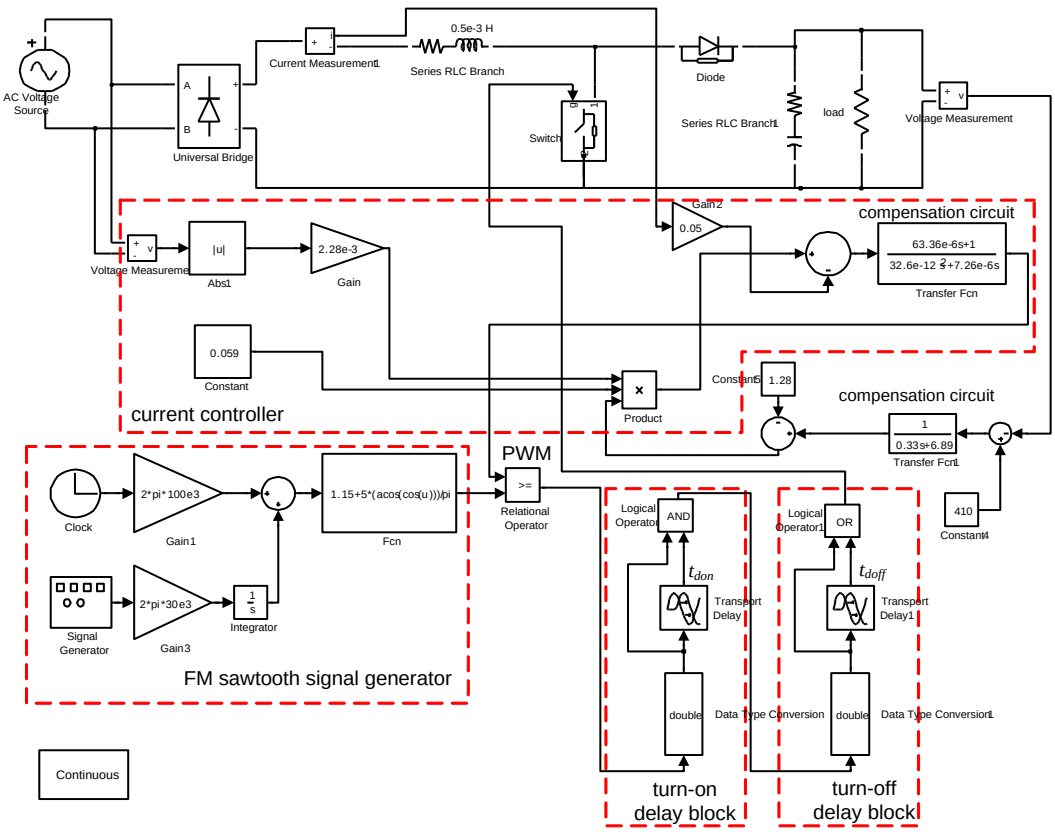


Figure 3. Boost PFC converter SIMULINK model. Note the model can be used with and without SFM

RC filter, squarer and divider (shown in Figure 2) are substituted with block „Constant" in this model in order to speed up the simulations. Actually, the block „Constant" numerical value of 0.059 is equal to $1/(4.1)^2$, where 4.1 V is DC voltage at the output of RC filter. Current sense resistor R_s is modeled using two SIMULINK blocks: „Current measurement 1" and „Gain 2". Input current control open loop gain can be described by formula [34]:

$$T(s)=H_s(s)H_{PWM}(s)H_c(s)H_{cic}(s), \quad (4)$$

where $H_s(s)$ is the current sensor gain; $H_{PWM}(s)$ is the PWM gain; $H_c(s)$ is the current loop compensation circuit gain and $H_{cic}(s)$ is the control-to-input current gain. For this model the transfer functions are:

$$H_s(s)=0.05;\ H_{PWM}(s)=0.2;\ H_{cic}(s)=V_{out}/(sL)=0.8/s;\ H_c(s)=(63.36\cdot10^{-6}s+1)/(32.6\cdot10^{-12}s^2+7.26\cdot10^{-6}s) \quad (5)$$

Based on (4) and (5) input current control open loop gain $T(s)$ versus frequency is depicted in Figure 4.

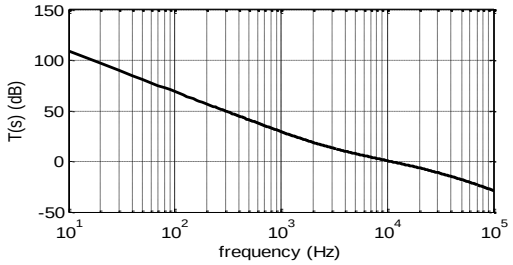


Figure 4. Input current control open loop gain of boost PFC converter model shown in Figure 3

Generator of frequency-modulated sawtooth signal is shown in Figure 5. It consists of modulating signal $m(t)$ (with unitary amplitude) generator, integrator, adder, amplifiers "Gain 1" and "Gain 3" and function block "Fcn". Output signal of "Gain 1" block is $2\pi f_{sw0}t$, but output signal of "Gain 3" block is $2\pi\Delta f_{sw}m(t)$. Where f_{sw0} is central switching frequency and Δf_{sw} is switching frequency deviation. The output voltage of FM sawtooth signal generator can be described by formula:

$$v_{\mathrm{mod}}(t) = 1.15 + 5\cdot\mathrm{acos}(\cos(2\pi f_{sw0}t + 2\pi\Delta f_{sw}\int_0^t m(\tau)d\tau))/\pi \quad (6)$$

Function "acos" is necessary in order to get sawtooth voltage from cosine. The most important waveforms of FM sawtooth signal generator are shown in Figure 6.

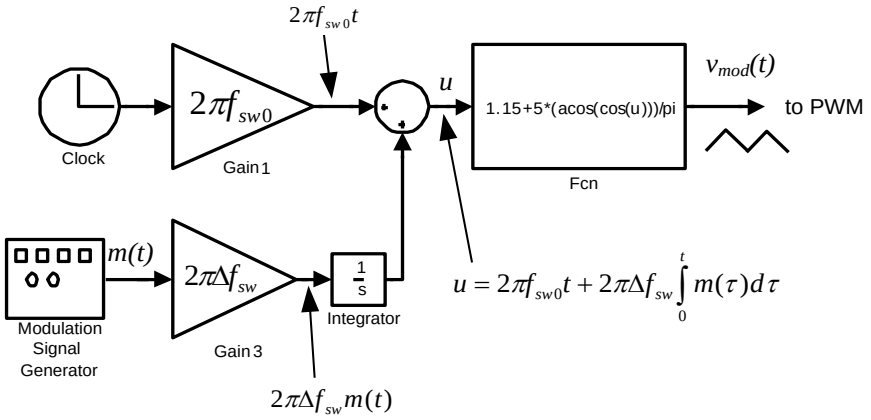


Figure 5. SIMULINK Model of FM Sawtooth Signal Generator

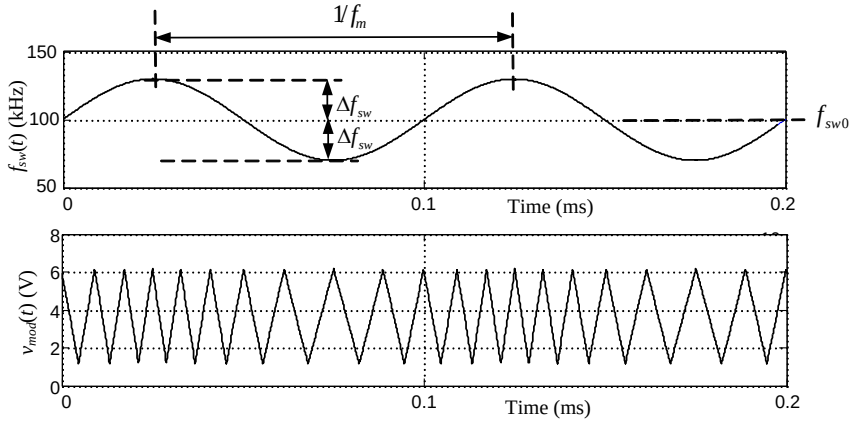


Figure 6. Simulated instantaneous switching frequency $f_{sw}(t)$ and output signal ($v_{mod}(t)$) of FM sawtooth signal generator. (Parameters: switching frequency deviation Δf_{sw}=30kHz; modulation frequency f_m=10kHz; central switching frequency f_{sw0}=100kHz)

4. THEORETICAL ANALYSIS OF INPUT CURRENT

This section presents a comprehensive theoretical analysis of the effects of SFM on boost PFC converter input current low-frequency content and THD. For the analysis SIMULINK model (Fig.3) is used.

4.1. Without SFM

If SFM is not used, then the PFC converter input AC current i_{acin} spectrum is made of f_{mains} harmonics with frequencies mf_{mains} (where m = 1, 2, 3…) as well as high-frequency components with frequencies $nf_{sw0} \pm kf_{mains}$ (where n = 1, 2, 3…, k = 1, 2, 3). This is depicted in Figure 7(c).

4.2. With SFM

To study the effect of SFM on boost PFC converter input PQ, difference between the switch turn-on and turn-off swiching delays ($|\Delta t_d|=|t_{doff}-t_{don}|$) is taken into account. As it can be deduced from Figure 7(c) and Figure 8(c), SFM, from one hand, has an advantage in terms of conducted EMI reduction, because high-frequency side-bands with noticeably lower amplitudes than for unmodulated PFC converter appear around f_{sw0} and its harmonics, but from other hand, it has disadvantage, because modulation frequency f_m subharmonics (with frequencies f_m-$(2y-1)\cdot f_{mains}$, where y=1, 2, 3, ...) and interharmonics (with frequencies $f_m+(2y-1)f_{mains}$ and $zf_m\pm(2y-1)f_{mains}$, where z=2, 3, 4, ...) appear in i_{acin} spectrum [Figure 8(c)]. First order subharmonic $A_{1,1}$ and interharmonic $A_{1,2}$ are the highest and they are most responsible for the input current i_{acin} distortion. Obviously the subharmonics and interharmonics can significantly increase THD of PFC input current and reduce PF. Moreover since PQ standards are more concerned with low-frequency content of SMPS input current, these low-frequency components can exceed maximally permissible values set by the PQ standards and as a result PFC converter under test will fail the harmonics test (of course, if frequencies of these undesirable low-frequency components are below power analyzer maximum analysis frequency f_{max}, e.g 2kHz). Effect of SFM on conducted EMI reduction (in terms of reduction of the amplitudes of the high-frequency components) in boost PFC converter has been addressed in [5]. In this paper we will study the effect of SFM on the THD of i_{acin} and f_m subharmonics and interharmonics in details.

As it is depicted in Figure 8(a), i_{acin} becomes highly distorted in time domain. Filtered versions of i_{acin} show distinct low-frequency ripples with modulation frequency f_m (Figure 8(b)). Amplitudes of the subharmonics and interharmonics are approximately linearly dependant on Δf_{sw}, as shown in Figure 9(b). As Δf_{sw} increases, the THD of i_{acin} also increases (Figure 9(a)). Higher values of $|\Delta t_d|$ lead to higher THD of i_{acin} and the amplitudes of the f_m subharmonics and interharmonics (they increase approximately linearly with $|\Delta t_d|$) as it is shown in Figure 10. The amplitudes of the undesirable componnets depend also on f_m: as f_m increases the amplitudes also increase as it can be deduced from Figure 11. The THD and PF of i_{acin} for different f_m are shown in Table 1. Note the THD of i_{acin} in this table is calculated using (3) when M=40 (as it is required by the international standards). As shown in Table 1, when f_m=10 kHz negative effect of SFM on the low-frequency content and the THD is completely neutralized (they are the same as in unmodulated case). This is because frequencies of f_m subharmonics are higher than $40f_{mains}$ (so they are out of the scope of the PQ analyzer, because M=40). However, if we calculate the THD using (3) when M=210 (Table 2), then THD for f_m=10 kHz is even worse than for lower f_m. Important conclusion appears here: if we want to

neutralize the negative effect of SFM on the low-frequency content from normative point of view, then we should choose f_m sligthtly higher than $40f_{mains}$.

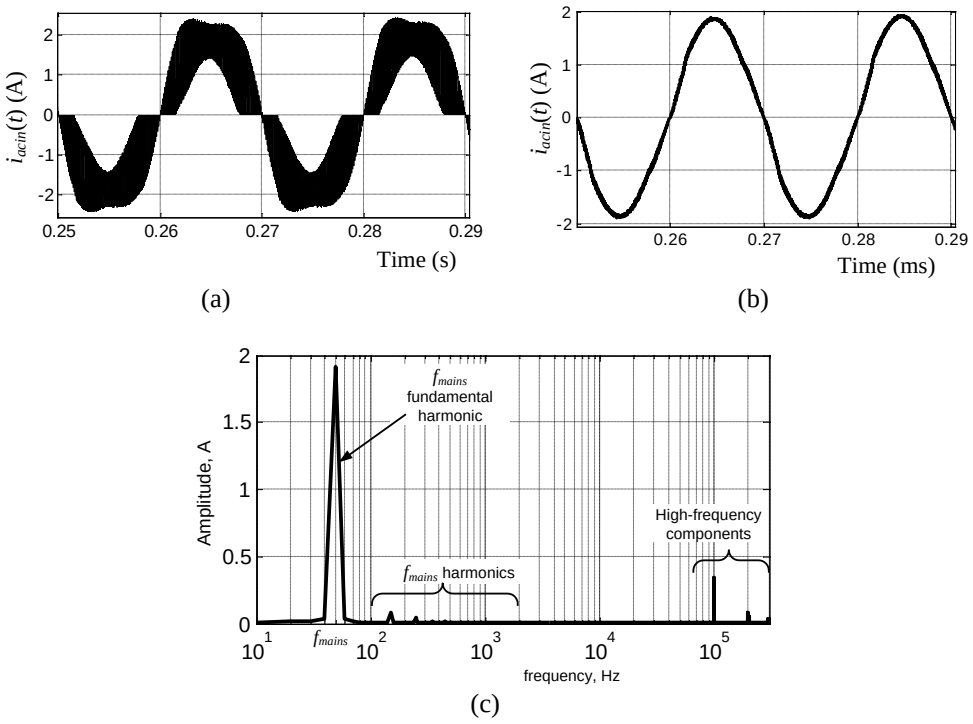


Figure 7. Simulated i_{acin} of CCM boost PFC converter: (a) in time domain without SFM; (b) in time domain without SFM (filtered); (c) in frequency domain without SFM. (Parameters: f_{mains} = 50 Hz, V_{inrms} = 240 V, L= 500 µH, V_{out} = 400 V, R_{out} = 485 Ω, P_{out}=330W; $|\Delta t_d|$=600 ns. Note: filtered version of i_{acin} [in Fig. 7(b)] is obtained using 2nd-order low-frequency filter with cutoff frequency of 2 kHz)

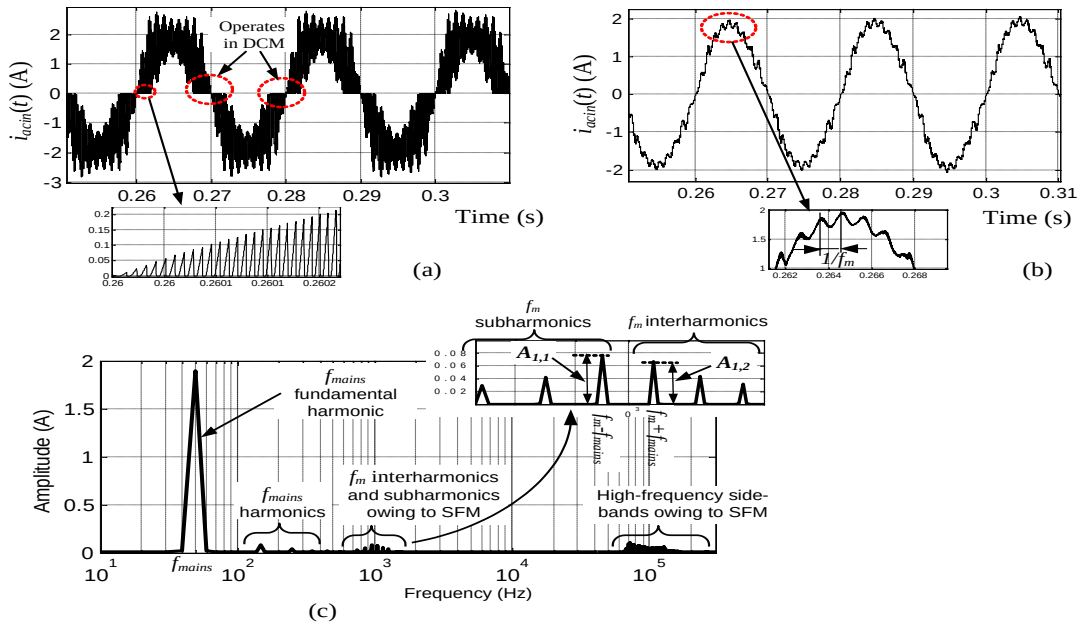
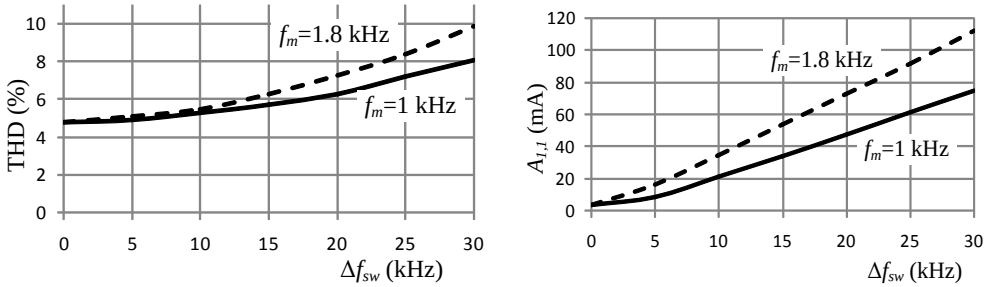
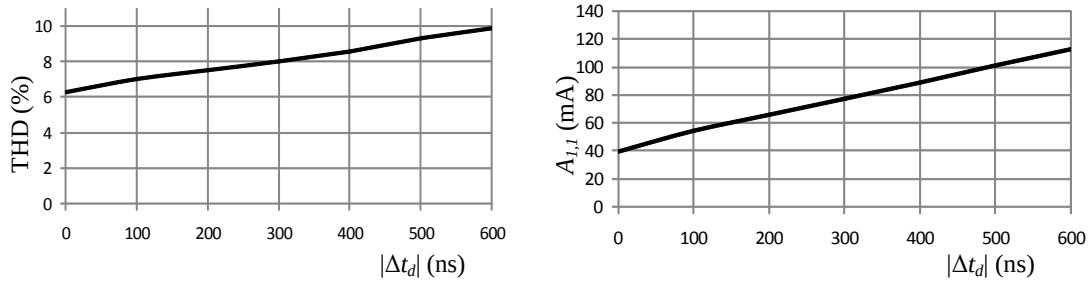


Figure 8. Simulated i_{acin} of SFM boost PFC converter: (a) in time domain; (b) in time domain (filtered); (c) in frequency domain. (Modulation parameters: $m(t)$ is sine, f_m = 1 kHz, Δf_{sw} = 30 kHz, f_{sw0} = 100 kHz. Other parameters the same as in Figure 7).



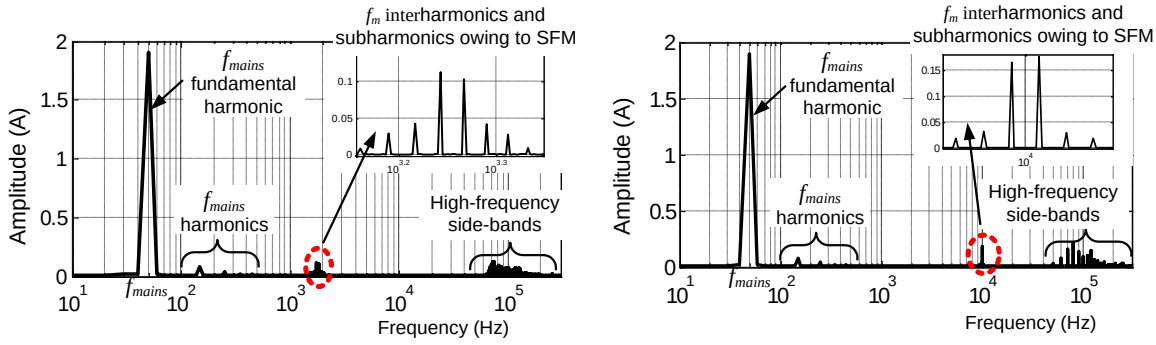
(a) (b)

Figure 9. Simulated THD of the PFC input current i_{acin} and $A_{1,1}$ versus Δf_{sw} for different f_m. (Modulation parameters: *m(t)* is sine; other parameters of the PFC converter the same as in Fig.7). Note THD of i_{acin} is obtained using (3) when M=40



(a) (b)

Figure 10. Simulated THD of the PFC input current i_{acin} and $A_{1,1}$ versus $|\Delta t_d|$. (Modulation parameters: *m(t)* is sine; f_m=1.8kHz; Δf_{sw}=30kHz; other parameters of the PFC converter the same as in Fig.7). Note THD of i_{acin} is obtained using (3) when M=40



(a) (b)

Figure 11. Simulated spectra of i_{acin} for different modulation frequencies: (a) f_m=1.8 kHz; (b) f_m=10 kHz. (Modulation parameters: *m(t)* is sine; Δf_{sw}=30kHz; other parameters of the PFC converter the same as in Figure 7).

The THD of i_{acin} and amplitudes of the f_m subharmonics and interharmonics caused by SFM depend also on modulation waveform *m(t)* [Figure 12(c), Table 3 and Table 4]. Sawtooth *m(t)* is more beneficial than sine because it gives a lower THD and amplitudes of the undesirable low-frequency components.

Table 1. Simulated THD and PF versus f_m (Δf_{sw} = 30 kHz, f_{sw0} = 100 kHz, *m(t)* is sine)

f_m (kHz)	THD (%)	PF
0.25	5.6	0.997
0.5	7	0.996
1	8.1	0.995
1.5	9.1	0.995
1.8	9.9	0.995
2	8.3	0.995
10	4.8	0.997

Table 2. Simulated THD and $A_{1,1}$ versus Δf_{sw} (f_m = 10 kHz, f_{sw0} = 100 kHz, *m(t)* is sine)

Δf_{sw} (kHz)	THD* (%)	THD** (%)	$A_{1,1}$ (mA)
0	4.8	4.9	3.7
10	4.8	6.4	53
20	4.7	9.8	108
30	4.7	13.9	165

* THD of i_{acin} is calculated using (3) when M=40; ** THD of i_{acin} is calculated using (3) when M=210.

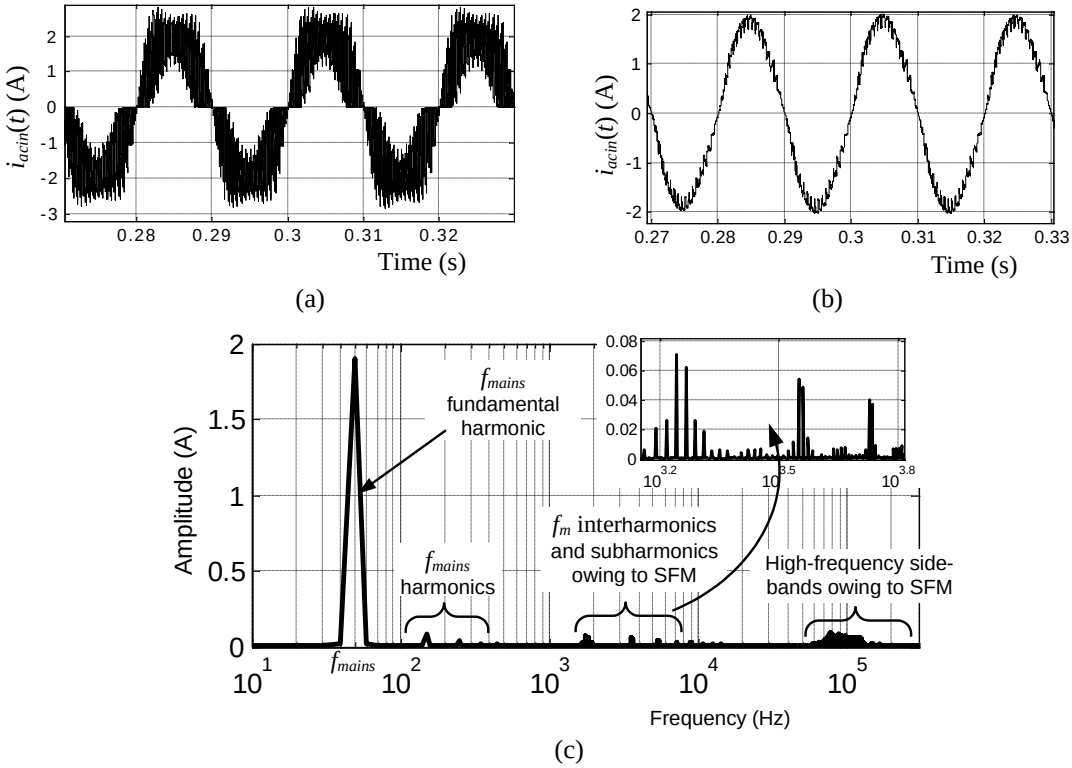


Figure 12. Simulated i_{acin} of SFM boost PFC converter: (a) in time domain; (b) in time domain (filtered); (c) in frequency domain. (Modulation parameters: *m(t)* is sawtooth, f_m = 1.8 kHz, Δf_{sw} = 30 kHz, f_{sw0} = 100 kHz. Other parameters the same as in Figure 7).

Table 3. Simulated THD and $A_{1,1}$ for different *m(t)* (f_m = 1 kHz, Δf_{sw}=30kHz, f_{sw0} = 100 kHz)

m(t)	THD (%)	$A_{1,1}$ (mA)
sine	8.1	76.2
triangular	6.8	62
sawtooth	6.6	46

Table 4. Simulated THD and $A_{1,1}$ for different $m(t)$ (f_m = 1.8 kHz, Δf_{sw}=30kHz, f_{sw0} = 100 kHz)

Δf_{sw} (kHz)	THD (%)	$A_{1,1}$ (mA)
sine	10.2	112.6
triangular	8.3	90
sawtooth	7.1	70.3

4.3. Summary of the Theoretical Analysis

An analysis of the effects of SFM parameters on the input PQ of the PFC converter reveals many interesting facts. Let us summarise the most important facts:

1. From normative point of view, the effect of SFM on input PQ of the PFC converter can be either harmful or almost harmless. This depends on the value of f_m:
   a. If f_m-f_{mains}>Mf_{mains} (where M is the harmonic number up to which the f_{mains} harmonics should be measured), then the SFM is harmless from the normative point of view. (Table 1 and Table 2 show that if f_m=10kHz, then the THD is almost the same as for PFC converter without SFM.)
   b. If $f_m + f_{mains} < Mf_{mains}$, then the SFM is harmful from the PQ point of view because the THD and the amplitudes of f_m interharmonics and subharmonics increase (Table 1 and Figure 9). In this case, THD and the amplitudes of f_m interharmonics and subharmonics increase approximately linearly as Δf_{sw} and $|\Delta t_d|$ increase.
2. Practical advices:
   a. In order to get low THD and the amplitudes of f_m interharmonics and subharmonics, the power MOSFET turn-on and turn-off switching delays should be as close as possible. So careful attention should be paid on designing power MOSFET control circuit.
   b. If f_m is chosen to be lower than Mf_{mains}, then Δf_{sw} should be chosen so that f_m interharmonics and subharmonics amplitudes do not exceed the maximally permissible levels according to the PQ standard. In order to estimate the correct value of Δf_{sw}, proposed SIMULINK model can be used.
3. The choice of modulation waveform $m(t)$ is also very important. A sawtooth $m(t)$ gives a lower THD, $A_{1,1}$ and $A_{1,2}$ but a sine $m(t)$ gives a higher THD, $A_{1,1}$ and $A_{1,2}$ (Table 3 and Table 4). It is interesting to note that a sawtooth also exhibits better EMI reduction than the sine and triangular $m(t)$ [28]. This is why the sawtooth $m(t)$ is the best choice from both points of view.
4. If f_m is chosen to be lower than Mf_{mains}, then there is a trade-off between the EMI attenuation and input PQ of the PFC converter because a higher Δf_{sw} gives a higher EMI attenuation, but the THD also increases. However, when f_m is chosen to be slightly higher than Mf_{mains}, then other SFM parameters should be chosen only from the EMI attenuation point of view, because in this case SFM does not worsen the PQ from normative point of view.

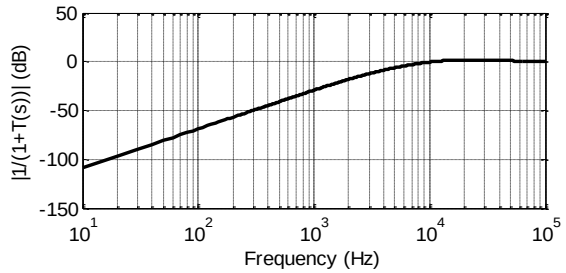


Figure 13. The boost PFC converter model (Figure 3) transfer function 1/(1+$T(s)$) magnitude versus frequency

5. EXPERIMENTS

5.1. Experimental Setup

In the experiments a 360W boost PFC converter demo board from STMicroelectronics™ is used [31]. The PFC converter produced by the STMicroelectronics is based on PWM controller L4981A and it does not have SFM. To perform the SFM, the modulating signal from a signal generator is fed into pin 17 of the controller via RC circuit as described in [5]. To measure Δf_{sw} a spectrum analyzer (Agilent E4402B)

with frequency demodulator and zero span capabilities is used. A picture and block diagramm of the experimental setup are shown in Figure 14. For input PQ (THD, PF, and input current low-frequency content) measurements, a low-distortion AC power source (TTI AC1000A) and power analyser (TTI HA1600A) are used. For input AC voltage and current measurements in the time domain, a digital storage oscilloscope (Agilent DSO3202A) connected to the waveform monitor outputs of a power analyser (TTI HA1600A) is used.

The nominal output power of the PFC is 330 W, the output DC voltage is 400 V, and the nominal switching frequency is 100 kHz. The open-loop gain crossover frequency of the current control loop is approximately 10 kHz. In order to compare experimental results with the simulated ones $|\Delta t_d|=|t_{doff}-t_{don}|$ was measured using the oscilloscope (when drain current amplitude was 2 A). It was 500 ns approximately. t_{doff} was measured between time instant at which both input voltages of PWM are equal and time instant at which drain-to-source voltage of the power MOSFET is equal to 10% of drain-to-source voltage amplitude. t_{don} was measured between time instant at which both input voltages of PWM are equal and time instant at which drain-to-source voltage of the power MOSFET is equal to 90% of drain-to-source voltage amplitude.

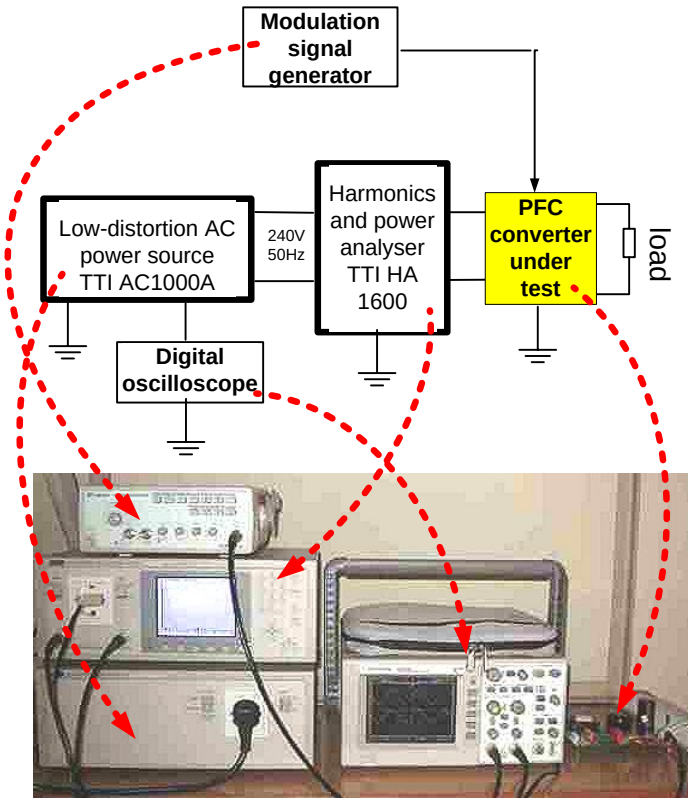


Figure 14. A picture and block diagramm of the experimental setup

5.2 Experimental Results

The experimental results are shown in Figure 15-Figure 17. A comparison of the simulation results with the experimental results is shown in Figure 18, Table 5 and Table 6. Note: in making the comparison it is assumed that $|\Delta t_d|$=500 ns. Figure 15 shows the input AC voltage and current waveforms obtained using the oscilloscope connected to the power analyser. Figure 16 shows the THD and power analysis from the power analyser screen for different cases. Figure 17 presents low-frequency harmonics analysis (up to the 40th harmonic) according to the IEC 1000-3-2 standard. Please note that the experimental waveforms shown in Figure 15 are obtained by connecting the oscilloscope to the waveform monitor outputs of the power analyser, which ignores all frequencies above 2 kHz. In order for the experimental waveforms to be comparable with the simulated ones, a simulated i_{acin} should be postprocessed with a low-frequency 2nd-order filter with a cutoff frequency of 2 kHz.

5.3. Discussion

As can be seen, the experiments confirm the simulations:

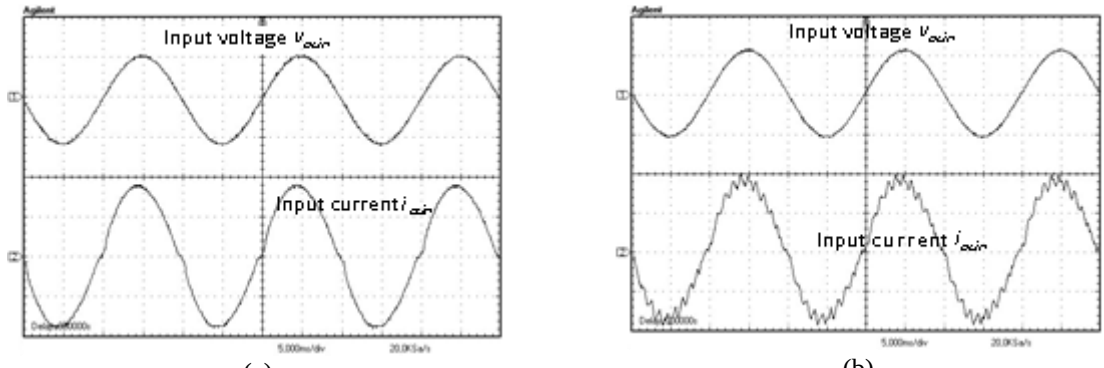
1. If $f_m + f_{mains} < Mf_{mains}$ (in our case, M =40), then SFM leads to a worsening PQ of the PFC converter [Figure 16(b,c,e)]. As Δf_{sw} increases, the THD, $A_{1,1}$ and $A_{1,2}$ also increase (Figure 18), but the PF decreases. The cause of this problem is related to low-frequency components (f_m interharmonics and subharmonics) owing to SFM in the i_{acin} spectrum. For higher Δf_{sw}, harmonic levels exceed the maximally permissible values set by the IEC standard. As a result, the PFC converter does not meet IEC requirements, as shown in Figure 16(c, e) and Figure 17(c, e).
2. If $f_m - f_{mains} > Mf_{mains}$, then PQ is not worsened: THD almost the same as for the unmodulated PFC converter [Figure 16(a) and Figure 16(d)].
3. When $f_m + f_{mains} < Mf_{mains}$ then lower f_m gives a lower THD and amplitudes of the subharmonics and interharmonics (Table 6) because open curren control loop gain is higher for lower frequencies (Figure 4).
4. A sawtooth *m(t)* gives a lower THD, $A_{1,1}$ and $A_{1,2}$ [Figure 16(e), Figure 17(e), Table 5].
5. The simulation results are in a quite good agreement with the experimental results. The differences between them are mainly a result of measurement errors and the fact that the nonlinearities of the power inductor are not taken into account in the simulations. Moreover in the SIMULINK model numerical values of the coefficients of the transfer functions are calculated based on the nominal (not actual) values of resistors and capacitors of the PFC converter under test. It should also be noted that the Simulink model (Figure 3) uses fixed Δt_d, but in reality it is variable.

Table 5. Experimental and simulated THD and PF for different *m(t)*

m(t)	Simulated THD (%)	Simulated PF	Experimental THD (%)	Experimental PF
sine	7.9	0.996	7.8	0.99
triangular	6.8	0.996	7	0.991
sawtooth	6.6	0.996	6.5	0.991

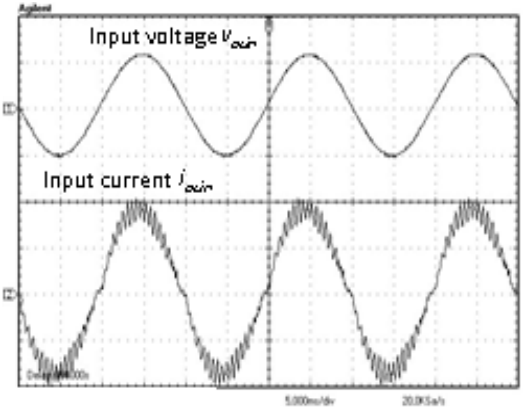
Table 6. Experimental and simulated THD and PF versus f_m

f_m *(kHz)*	Simulated THD (%)	Simulated PF	Experimental THD (%)	Experimental PF
0.25	5.6	0.997	5	0.993
1	7.9	0.996	7.8	0.99
1.5	9.1	0.995	9.4	0.989
1.8	9.9	0.995	10.7	0.987
2	8.3	0.995	8.7	0.986
10	4.8	0.997	4.6	0.993

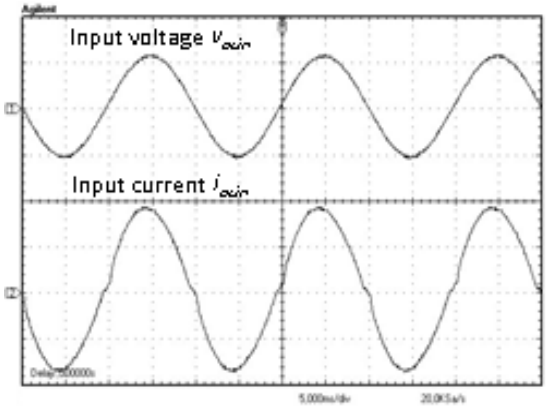


(a) (b)

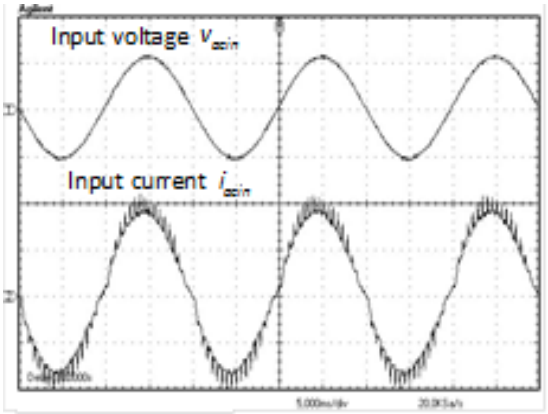
Figure 15. Input AC voltage and current (filtered) waveforms of PFC converter under test for different cases: (a) without SFM; (b) with sinusoidal SFM, f_m = 1 kHz, Δf_{sw} = 30 kHz.



(c)



(d)



(e)

Figure 15. Input AC voltage and current (filtered) waveforms of PFC converter under test for different cases:(c) with sinusoidal SFM, f_m = 1.8 kHz, Δf_{sw} = 30 kHz; (d) with sinusoidal SFM, f_m = 10 kHz, Δf_{sw} = 30 kHz; (e) with sawtooth SFM, f_m = 1.8 kHz, Δf_{sw} = 30 kHz. (Scale: time 5 ms/div; input voltage 310 V/div; current 1 A/div)

(a)

(b)

Figure 16. THD and power analysis of PFC converter under test for different cases: (a) without SFM; (b) with sinusoidal SFM, f_m = 1 kHz, Δf_{sw} = 30 kHz;

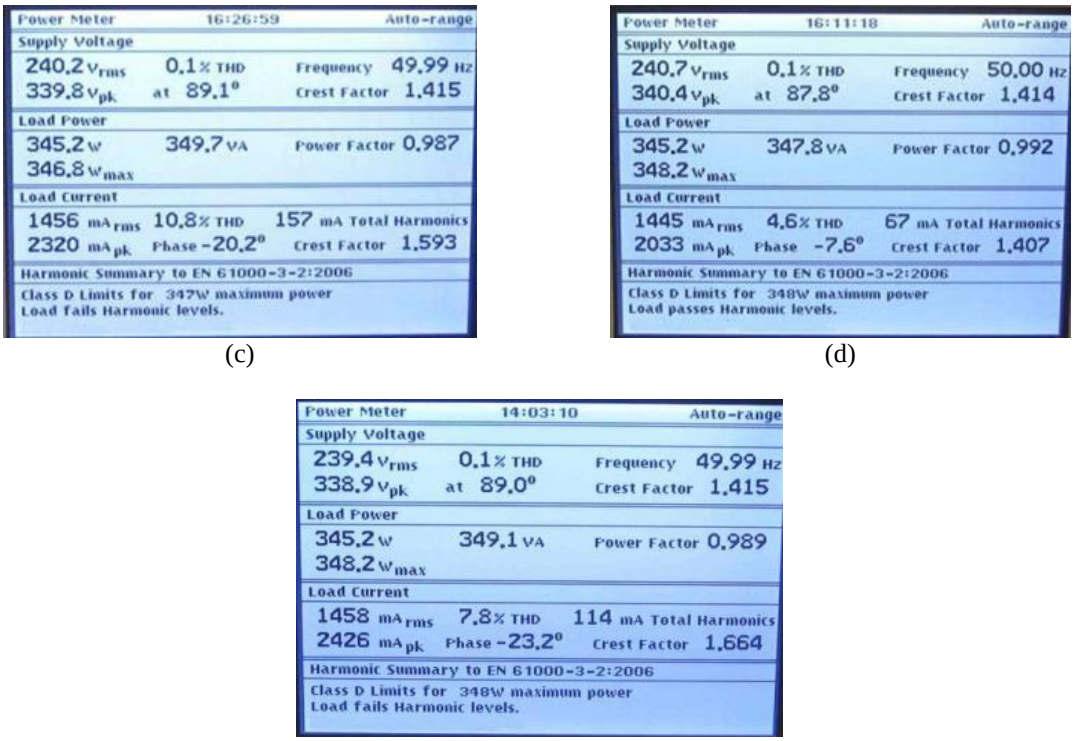


Figure 16. THD and power analysis of PFC converter under test for different cases: (c) with sinusoidal SFM, f_m = 1.8 kHz, Δf_{sw} = 30 kHz; (d) with sinusoidal SFM, f_m = 10 kHz, Δf_{sw} = 30 kHz; (e) with sawtooth SFM, f_m = 1.8 kHz, Δf_{sw} = 30 kHz

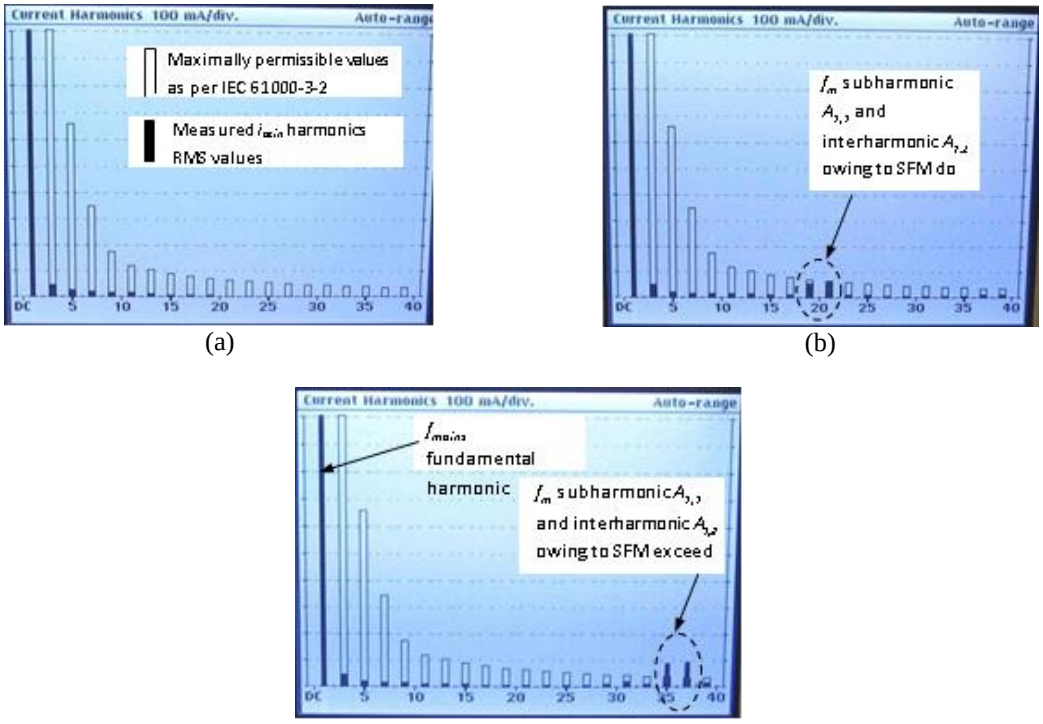
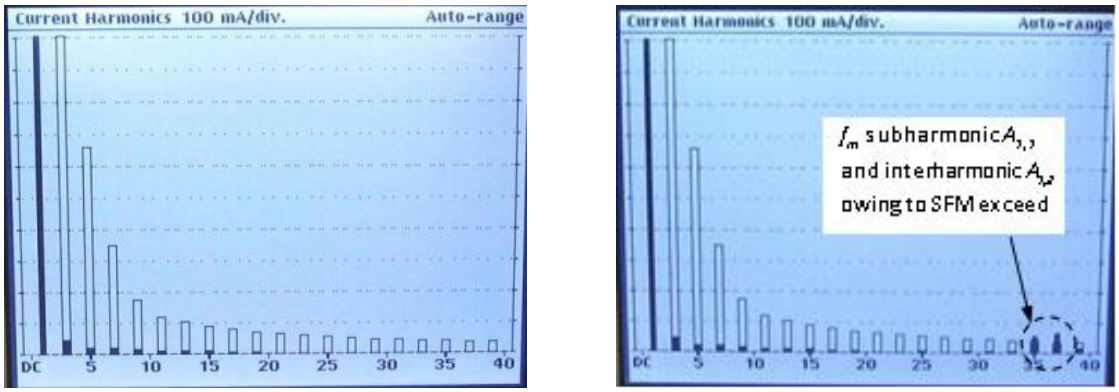


Figure 17. Harmonics analysis of PFC converter input current (up to the 40th harmonic) for different cases: (a) without SFM; (b) with sinusoidal SFM, fm = 1 kHz, Δfsw = 30 kHz; (c) with sinusoidal SFM, fm = 1.8 kHz, Δfsw = 30 kHz;



(d) (e)

Figure 17. Harmonics analysis of PFC converter input current (up to the 40th harmonic) for different cases: (c) with sinusoidal SFM, f_m = 1.8 kHz, Δf_{sw} = 30 kHz; (d) with sinusoidal SFM, f_m = 10 kHz, Δf_{sw} = 30 kHz; (e) with sawtooth SFM, f_m = 1.8 kHz, Δf_{sw} = 30 kHz

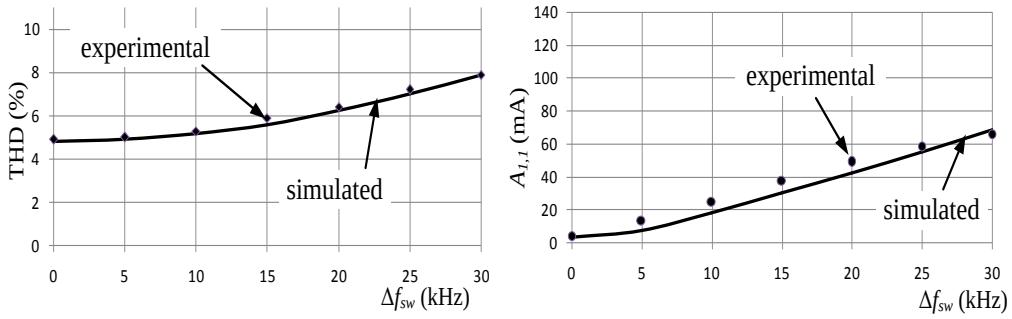


Figure 18. Comparison of the simulation and experimental results for different f_m when $|\Delta t_d|$=500 ns

6. COMPARISON OF THE ANALYSES PERFORMANCES

This section presents comparison of the performance of our analysis of the effect of SFM on the PQ of boost PFC converter to the performance of the analysis presented in [22]-[23]. As it was said in introduction, papers [22] and [23] show some experimental results demonstrating that THD of boost PFC input current increases owing to the use of triangular SFM. However the analysis presented in the above mentioned papers have many disadvantages:

1. The analysis is very short, is not comprehensive and is based only on some experimental results.
2. The analysis does not give any clear answers on how the choice of SFM parameters affects the THD, the power factor and the input current low-frequency content.
3. The analysis has some ambiguities:
   a. It is stated in [22] and [23] that the main cause of increase in the THD is appearance of f_m harmonics in the PFC input current spectrum. However as it is proved in our paper, SFM does not generate f_m harmonics, instead it generates f_m subharmonics and interharmonics with frequencies $zf_m \pm (2y\text{-}1)f_{mains}$. These subharmonics and interharmonics are responsible for the increase in the THD.
   b. It is stated in [22] and [23] that the main cause of f_m harmonics in the PFC input current spectrum is owing to some interactions between the PFC converter wide-bandwidth current control loop and SFM. However as it is proved in our paper, the main causes of the f_m interharmonics and subharmmonics in the input current spectrum are DCM operation of the PFC converter in the vicinity of the input current zero-crossings and unequal power MOSFET switching delays. Moreover as it is shown in our paper wide-bandwidth current control loop reduces the undesirable low-frequency components owing to SFM if f_m is lower than the current control open loop gain crossover frequency, because lower f_m gives lower amplitudes of the interharmonics and subharmonics (Table 6).

4. The analysis is based on the measurements using a digital storage oscilloscope without taking into account the IEC requirements for the THD and harmonics measurements.
5. Genuine causes of worsening the PQ of the PFC converter are not revealed.
6. Some advice for choosing correct SFM parameters are not given in [22] and [23].

When making comparison of the performance of our analysis with the performance of the analysis presented in [22] and [23] we can mention many advantages:

1. Our analysis of the effect of SFM on the boost PFC converter input power quality is detailed, comprehensive and is based not only on experimental results but also on simulation results (for this purpose boost PFC converter SIMULINK model is proposed in this paper).
2. The PQ measurements are done as required by the IEC using high-quality power and harmonics analyser.
3. Our analysis gives a clear answer what causes decrease in the power factor, inscerase in the THD and appearance of the undesirable low-frequency content of the PFC converter owing to use of SFM and gives some advice for the choice of the SFM parameters.
4. Detailed explanation of the effect of SFM parameters on the PQ of the PFC converter is also presented.

7. CONCLUSION

The analysis presented in the paper shows that SFM used for EMI suppression in PFC converters can appreciably increase the THD of the input AC current of the PFC converter and consequently degrade the input PQ. The main cause of the problem is that SFM causes noticeable modulation frequency subharmonics and interharmonics in the PFC converter AC input current spectrum. Since power quality standards are very concerned with the low-frequency content of input current, these modulation-frequency interharmonics and subharmonics can exceed the maximally permissible values set by the PQ standard. As a result, a PFC converter under test will fail the harmonics test. The low-frequency components are a result of two causes: DCM operation of the PFC converter in the vicinity of the input current zero-crossings and unequal power MOSFET switching delays. Higher Δf_{sw} gives higher THD of the input AC current and higher amplitudes of the subharmonics and interharmonics. The choice of modulation waveform also affects the THD. A sawtooth modulation waveform results in lower distortion of the PFC converter input current.

Even though SFM results in input current distortion for all modulation frequencies (lower f_m gives lower THD), from normative point of view the negative effects of SFM on input PQ can be completely neutralized when a modulation frequency is chosen to be slightly higher than Mf_{mains} (where M is harmonic number up to which the harmonics should be analyzed) because power analysers measure harmonics up to a certain frequency (e.g. 40·50=2 kHz).

In order to simplify the design of a SFM boost PFC converter operating in CCM, proposed SIMULINK model as well as some advice for choosing correct SFM parameters, can be used. Overall, we conclude that, from the power quality point of view, SFM can be either harmful or harmless. The result depends on how properly the modulation parameters (especially the modulation frequency) are chosen.

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