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A comparative Analysis of Symmetrical and Asymmetrical Cascaded Multilevel Inverter Having Reduced Number of Switches and DC Sources

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ABSTRACT

As multilevel inverters are gaining increasing importance .New topologies are being proposed in order to achieve large number of levels in output voltage. A simplified MLI topology has been presented with both symmetrical and asymmetrical configurations. This paper represents a comprehensive analysis of above mentioned topology with FFT analysis,switching and conduction losses of the inverter.Hence efficiency at different carrier frequencies has been calculated successfully.Results are verified with simulation studies.Multilevel inverters are currently considered as a better industrial solution for high dynamic performance and power-quality demanding applications, covering a wide power range.

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1. INTRODUCTION

The two level inverters however have many limitaions in operating at high frequency mainly due to constraints of device ratings and switching losses. The multilevel inverters have got tremendous interest in the power indusry.Increasing the number of voltage levels in the inverter without requiring higher ratings on indivisual devices can increase the power rating [1]. Without the use of transformers the unique structure of MLI allows them to reach high voltages with low harmonics or series connected snchronised switching devices.MLIs are divided into three categories, they are neutral point clamped , flying capacitor and cascaded H-bridge [2]. For high voltage applications Cascaded H-bridge multilevel inverter has been researched and preferable [3]-[4]. As the number of level increases, the number of H-bridges also increases [5]. TO avoid the large number of Dc sources, cascaded MLIs are again designed for reduced number of Dc sources and switches [6]. They are catagorised as symmetrical and asymmetrical Cascaded MLIs [7] depending upon the voltage source used. A different topology of MLI designed from several bidirectional switches is proposed in [8]. .Due to bidirectional switches voltage stress across the switches is higher.As the number of switches are less compared to conventional topologies each switch undergoes high voltage stress and switching loss thus increased [9].

2. RESEARCH METHOD

2.1. Proposed Topology

It has two voltage sources V_1 and V_2 along with two capacitors C_1 and C_2 which act like voltage divider circuit. If $V_1=V_2$ it is treated as symmetrical otherwise asymmetrical. Proposed Topology produces 7/9/11 levels with certain voltage combinations.

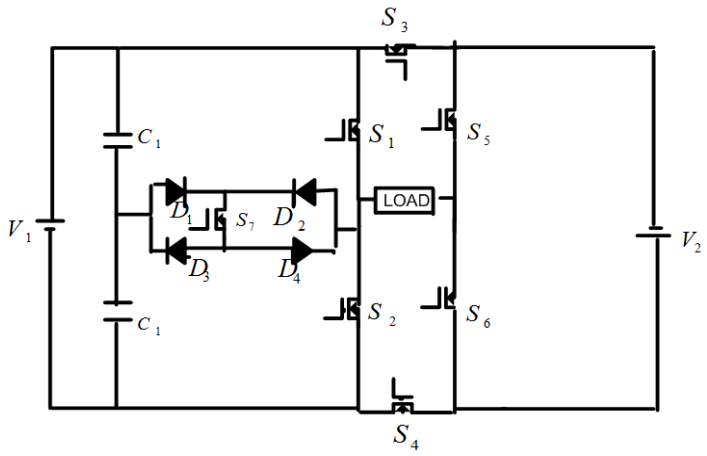

Figure 1. Proposed Topology

2.2 Different Switching States Of Topology

Topology with different levels have been represented in this section. Both symmetrical and asymmetrical configurationshave been simulated at different carrier frequencies and results are compared.

Table 1. Different Switching Strategies

7 level		9 Level		11 Level	
Out put	Conducting Switches	Output	Conducting Switches	Output	Conducting switches
Vdc	S_4 , S_2 , S_5	Vdc	S_7 , S_6 , S_4	Vdc	S_4 , S_2 , S_5
2Vdc	S_4 , S_7 , S_5	2Vdc	S_4 , S_2 , S_5	2Vdc	S_7 , S_6 , S_4
3Vdc	S_4 , S_1 , S_5	3Vdc	S_4 , S_7 , S_5	3Vdc	S_4 , S_7 , S_5
0	S_1 , S_3 , S_5	4Vdc	S_4 , S_1 , S_5	4Vdc	S_6 , S_4 , S_1
-Vdc	S_6 , S_1 , S_3	0	S_1 , S_3 , S_5	5Vdc	S_4 , S_1 , S_5
-2Vdc	S_3 , S_6 , S_7	-Vdc	S_3 , S_5 , S_7	0	S_1 , S_3 , S_5
-3Vdc	S_6 , S_2 , S_3	-2Vdc	S_6 , S_1 , S_3	-Vdc	S_6 , S_1 , S_3
x	x	-3Vdc	S_3 , S_6 , S_7	-2Vdc	S_3 , S_5 , S_7
x	x	-4Vdc	S_6 , S_2 , S_3	-3Vdc	S_6 , S_7 , S_3
x	x	x	x	-4Vdc	S_3 , S_5 , S_2
x	x	x	x	-5Vdc	S_3 , S_6 , S_2

For 7 level asymmetrical V_1=2V, V_2=V and V_{dc}=V. For 9 level symmetrical V_1=V_2=V.For 11 level asymmetrical V_1=4V, V_2=V.

3. MODULATION SCHEME

Both for symmetrical and asymmetrical topologies to generate gating signal, Phase Disposition Pulse Width Modulation (PDPWM) technique is preferable.

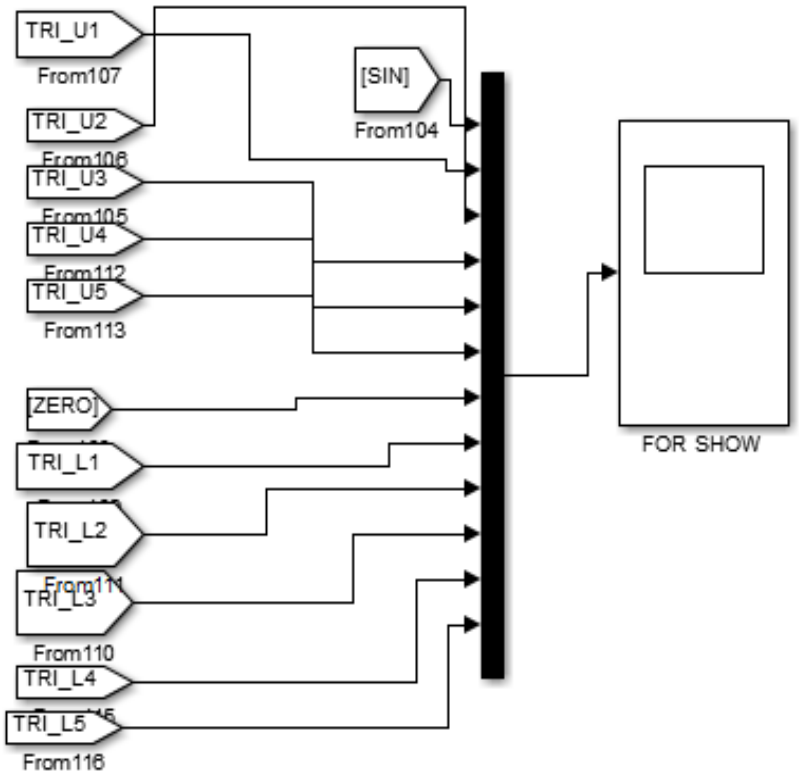

Figure 2(a). PWM signals Generaion for Proposed Topology

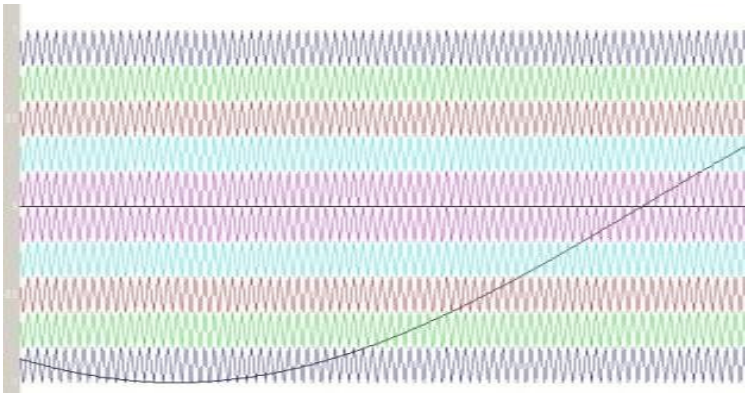

Figure 2 (b). PWM signals for Proposed Topology

4. SIMULATION RESULTS

For proposed topology the simulations are carried out in MATLAB environment and results are compared. Following Figure 4 represents output voltage and current wave form at Carrier Frequency=10KHz,R=10Ω,L=25mH in 11 level asymmetric configuration.

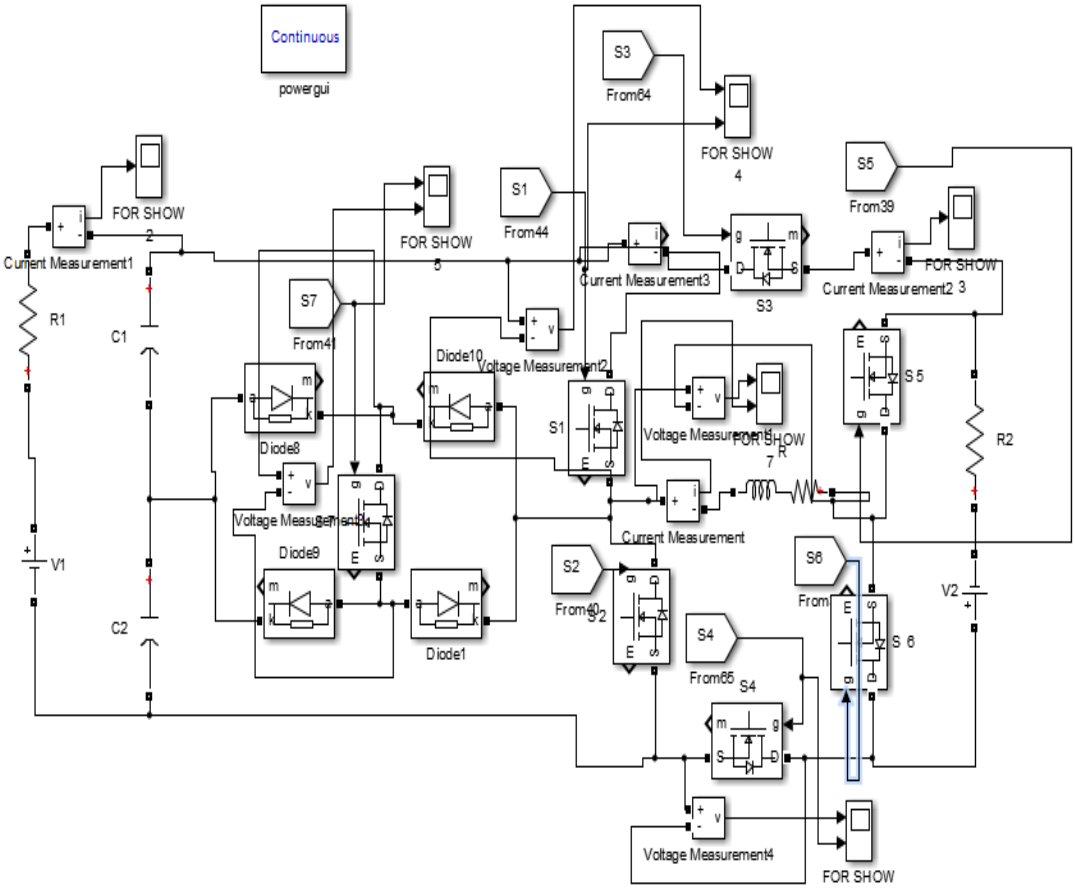

Figure 3. Simulaion in MATLAB for Proposed Topology

Each voltage source is connected with a current measuring device to measure input current.Similarly load current can be measured by the current measurement device in RL load.Hence input power and ouput power has been calculated.

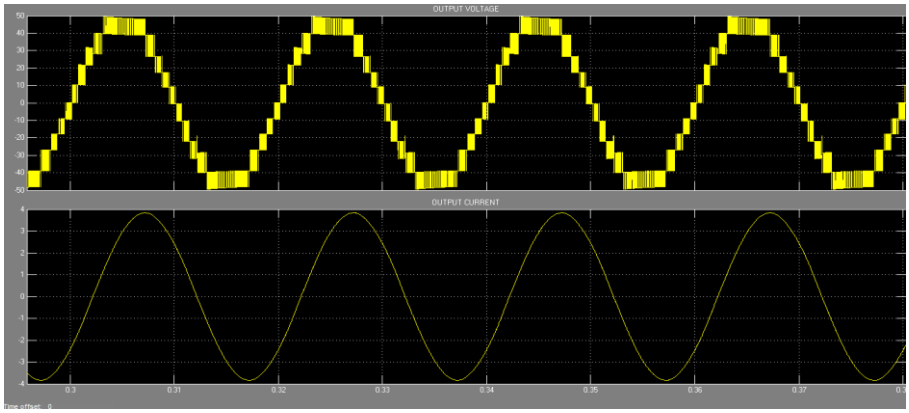

Figure 4. Simulaion in MATLAB for Proposed Topology boh voltage and current

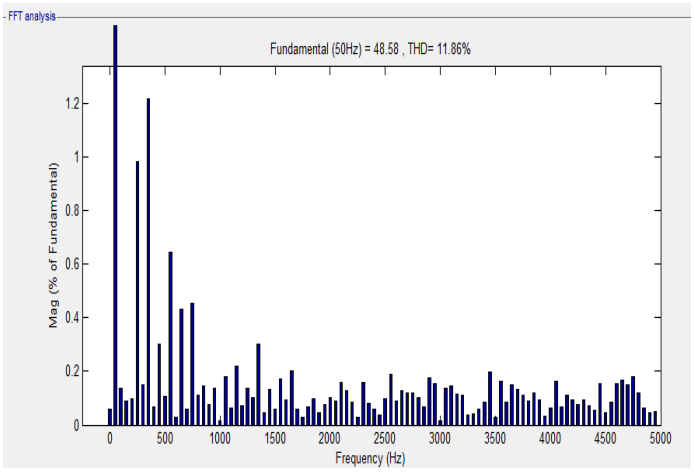

Figure 5. FFT analysis in MATLAB for Proposed Topology

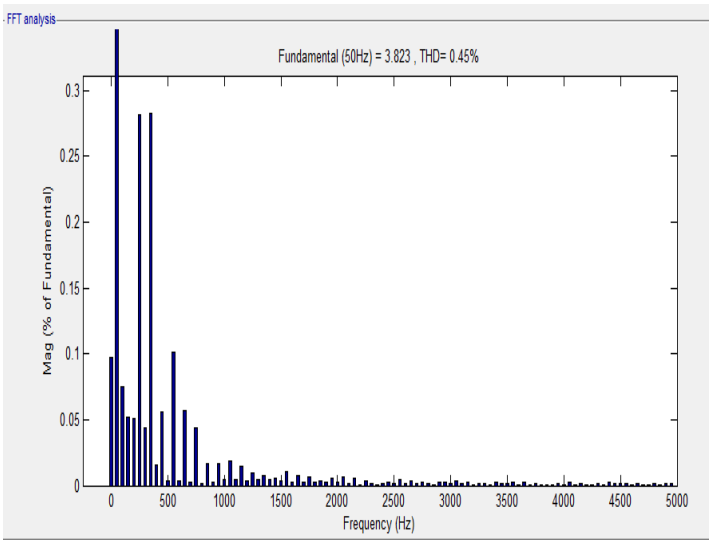

Figure 6. FFT Analysis of load current in MATLAB for Proposed Topology

5. RESULT ANALYSIS

At Modulation index(MI) 1,for Asymmetrical 7 level at V_1= 30V and V_2= 15V , symmetrical 9 level at V_1= 30Vand V_2= 30V, Asymmetrical 11 level at V_1= 40V, V_2= 10V the input power,output power and losses are calculated at different carrier frequencies . FFTanalysis for both voltage and current have been presented for the load RL type.

Table 3. Inverter losses, THDs and efficiencies at different carrier frequencies at MI=1

7 Levels						
Carrier frequencies(in KHz)	Input Power	Output Power	Losses	V_{thd}	I_{thd}	Efficiency(η)
1	61.36	50.32	11.04	17.53	20.5	0.82
3	63.16	51.73	11.43	21.17	18.79	0.819
5	63.72	51.3	12.42	22.4	17.36	0.805
7	69.54	55.29	14.25	22.16	15.98	0.795
10	74.06	57.77	16.29	19.78	14.06	0.78
15	77.6	58.2	19.4	16.56	12.5	0.75
9 Levels						
Carrier frequencies(in KHz)	Input Power	Output Power	Losses	V_{thd}	I_{thd}	Efficiency(η)
1	106.3	95.4	10.9	18.07	4.3	0.84
3	110.06	98.16	11.9	18.81	3.68	0.83
5	112.74	100.02	12.72	18.98	2.88	0.85
7	115.62	101.64	13.98	18.67	2.10	0.80
10	116.55	102.05	14.5	17.53	1.9	0.78
15	118.42	103.4	15.02	16.4	1.4	0.76
11 Levels						
Carrier frequencies(in KHz)	Input Power	Output Power	Losses	V_{thd}	I_{thd}	Efficiency(η)
1	79.48	68.69	10.79	10.21	1.74	0.867
3	80.82	69.22	11.6	12.7	1.31	0.856
5	82.79	70.33	12.46	13.09	1.0	0.849
7	85.34	71.43	13.91	13.06	0.71	0.837
10	87.13	72.91	14.22	11.86	0.45	0.836
15	88.02	73.22	14.8	9.89	0.2	0.831

In all the levels it has been observed that with increase in inverter levels the inverter losses reduced at same carrier frequency but in same level with increase in carrier frequencies the inverter losses increases. The inverter efficiency and THD in current reduces as the carrier frequency increases. The results of 11 level asymmetrical CHB has been taken into consideration to obtain Switching and Conduction losses of the inverter.

Table 4. Switching and Conduction losses for Proposed Topology (11level)

Carrier Frequency (in KHz)	Inverter Loss(in W)	Conduction Loss(in W)	Switching Loss(in W)
1	10.79	9.99	0.8
3	11.6	10.58	1.02
5	12.46	10.62	1.84
7	13.91	10.44	3.47
10	14.22	10.69	3.53
15	14.8	10.89	3.91

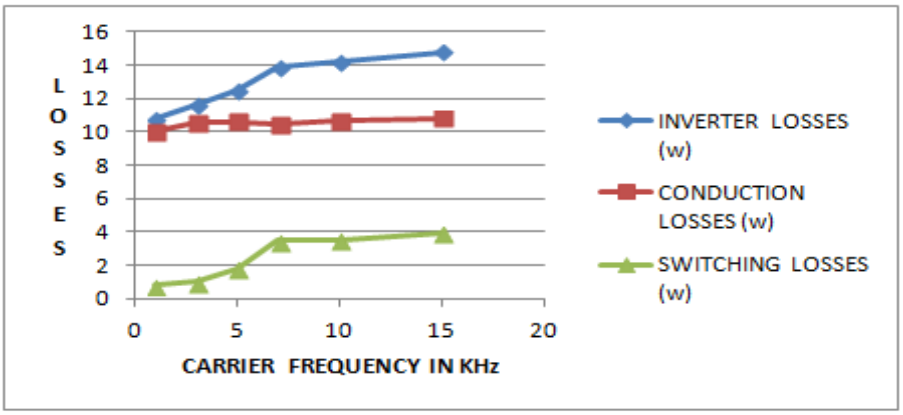

Figure 7.Carrier frequencies vs inverter losses

It has been observed that with increase in carrier frequency the switching loss is increasing whereas the conduction losses are independent on carrier frequencies.Hence inverter losses increases with increase in carrier frequencies.

Table 5. THD at different carrier frequencies

Carrier Frequencies	7 Levels		9 Levels		11 levels	
	THD	Efficiency	THD	Efficiency	THD	Efficiency
1	7.84	0.82	4.31	0.84	1.74	0.867
3	7.61	0.819	3.68	0.83	1.31	0.856
5	5.61	0.805	2.88	0.85	1.0	0.845
7	3.98	0.795	2.10	0.80	0.71	0.837
10	2.71	0.78	1.9	0.78	0.45	0.836
15	2.2	0.75	1.4	0.76	0.26	0.831

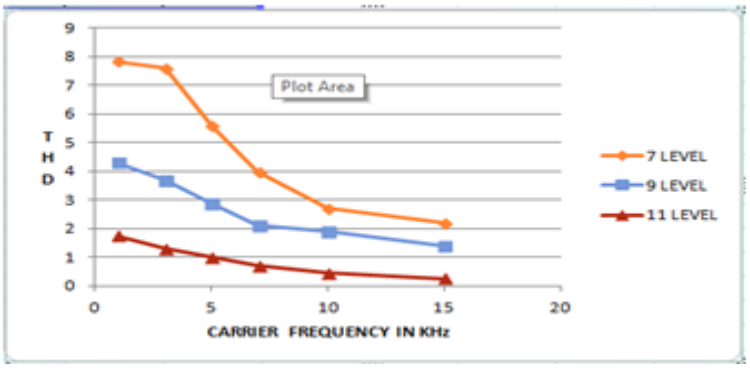

Figure 8. THD at different levels of topology l

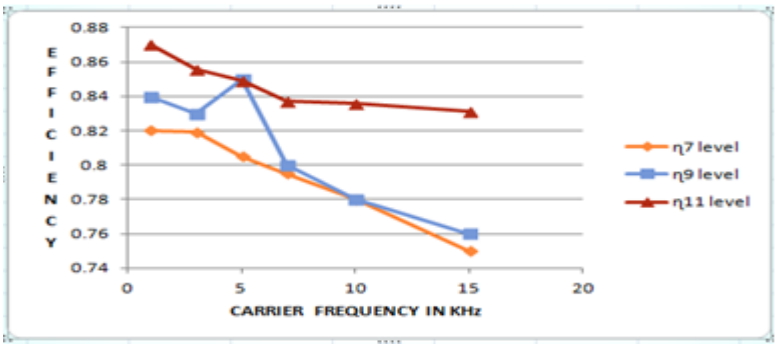

Figure 9. Carrier frequencies vs efficiencies of Topology1

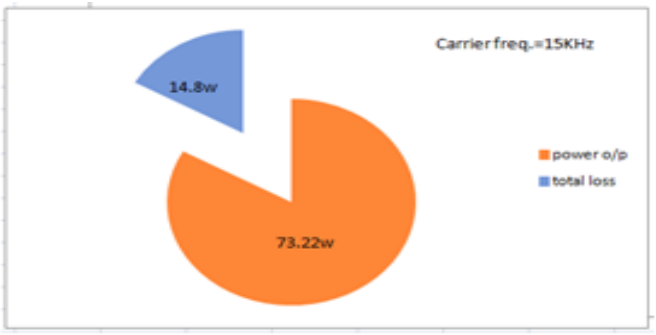

Figure10. Percentage o f output power and Inverter losses

6. CONCLUSION

In this paper, compared to conventional symmetrical and asymmetrical topologies the proposed topologies have less number of switches and DC sources .From simulation it has been observed that with increase in carrier frequencies THD in load current and the inverter efficiency reduces. At the same carrier frequency ,the inverter efficiency is more in higher levels . With increase in MI volage THD reduced significantly.

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