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Bidirectional Resonant DC-DC Converter for Microgrid Application

Jaisudha S., Sowmiya Srinivasan, Kanimozhi G.
School of Electrical Engineering, VIT University, Chennai, India

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ABSTRACT

This paper proposes a non-isolated soft-switching bidirectional DC/DC converter for interfacing energy storage in DC microgrid. The proposed converter employs a half-bridge boost converter at input port followed by a LCC resonant tank to assist in soft-switching of switches and diodes, and finally a voltage doubler circuit at the output port to enhance the voltage gain by two times. The LCC resonant circuit also adds a suitable voltage gain to the converter. Therefore, overall high voltage gain of the converter is obtained without a transformer or large number of multiplier circuit. For operation in buck mode, the high side voltage is divided by half with capacitive divider to gain higher step-down ratio. The converter is operated at high frequency to obtain low output voltage ripple, reduced magnetics and filters. Zero voltage turn-on is achieved for all switches and zero current turn-on and turn-off is achieved for all diodes in both modes i.e., buck/boost operation. Voltage stress across switches and diode is clamped naturally without external snubber circuit. An experimental prototype has been designed, built and tested in the laboratory to verify the performance of the proposed converter.

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Corresponding Author:

Kanimozhi.G,
School of Electrical Engineering,
VIT University, Vandalur –kelambakkam Road, Chennai, India.
Email: kanimozhi.g@vit.ac.in

1. INTRODUCTION

Micro-grids are smaller grids confined to a limited area that can be disconnected from the traditional grid to operate autonomously and they able to operate while the main grid is down. Micro-grids can build up grid flexibility and help alleviate grid disturbances as well as function as a grid resource for faster system response and recovery [1-6]. Micro-grids support a flexible and efficient electric grid by enabling the integration of growing deployments of distributed energy resources such as renewable like solar as shown in Figure1. In addition, the use of local sources of energy to serve local loads helps reduce energy losses in transmission and distribution, further increasing the efficiency of the electric delivery system [7]-[8]. Solar photovoltaic, fuel cells and battery output are available as source in dc form [9]-[10] and therefore, another stage of conversion is required before its interconnection with an ac system or regulated dc system. To improve the conversion efficiency, dc grid is an alternative [11]-[14].

Figure 1 shows a typical design of a dc micro-grid with a low-voltage battery bus of 48 V and a high-voltage dc-bus of 380 V fed by numerous sources as well as energy storage elements. The battery acts as a backup device owing to its high energy density [15], providing energy under the steady-state condition when the other sources are not capable. Thus a bidirectional converter [16] is required for voltage conversion and power flow control. Conventionally, the bidirectional converter have been categorized into two, namely, isolated [17] and non-isolated [18]. An isolated bidirectional DC/DC converter attains high voltage gain by changing isolated transformer turn ratios, such as flyback‑type, forward‑flyback‑type [19-20]. Non isolated converters operating at extreme duty cycle in either direction to achieve high step up/step down ratio leads to extreme stress on devices, resulting in large reverse recovery loss and high EMI issues. High-frequency operation is vital to realize high power density, improve dynamic characteristics and reduce aural noise. The switching frequency of the hard switching bidirectional converter is restricted due to switching losses and EMI problem.

The bidirectional power flow using switched-capacitor converter cells have modular structure and higher power handling capability, but the number of switches required becomes high [21]. Their major drawbacks are hard-switched devices and high current pulse arises since two capacitors with dissimilar voltages are connected in parallel at every switching instant. A major shortcoming of the switched capacitor-based converter is ESR drop of the active and passive devices, which are significant due to large number of series connected devices in the current path causing reduced output voltage. This limits the power level to which the switched capacitor converter can be functional.

To overcome the above drawbacks, a non-isolated bidirectional converter with high-voltage gain that can be applied to high power level has seldom been suggested. In order to increase the switching frequency of the bidirectional converters with soft switching techniques, an auxiliary circuit in both forward and reverse modes of operation to realize Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) of the switches [22-24] is used. The high-efficiency bidirectional dc–dc converter for a power storage system topology is developed in [25], which can boost the voltage of an energy-storage module to a high-voltage side dc bus for a given load demand. When there is excess energy in high-voltage-side dc bus, this energy-storage module can be charged by the dc bus. However one major disadvantage of this module is that the analysis is difficult, also it makes the converter bulky.

The proposed topology employs a half-bridge boost converter followed by an LCC resonant circuit and a voltage doubler circuit. It is operated at high frequency for the advantage of low output voltage ripple and reduced magnetics. Zero voltage turn-on and Zero current turn-on / turn-off is achieved for all switches and diodes. Voltage stress across switches is less and clamped naturally without external snubber circuit. Moreover, it supplements the output from the half bridge boost giving a high voltage gain and soft switching of the power switches within the operating range.

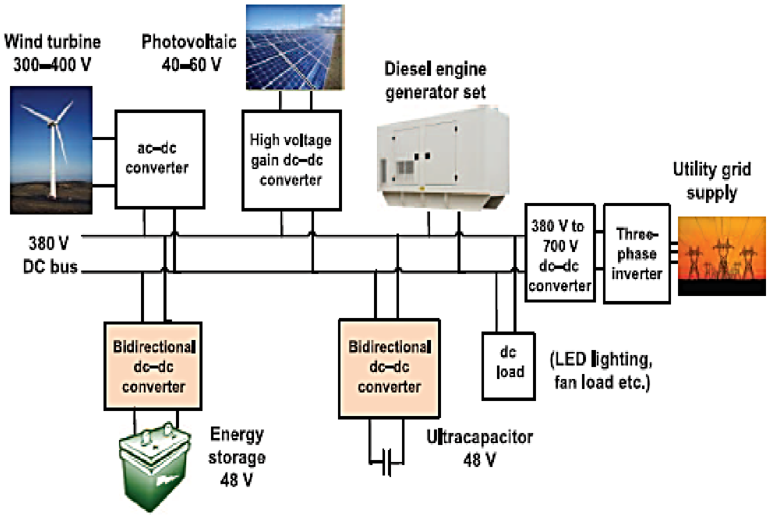


Figure 1. A typical Micro-grid system

The paper is structured as follows: Section 1 explores conventional bidirectional converter with its merits and demerits. Section 2 gives an overview of the theoretical evaluations to design the proposed converter and describes its working in detail. Section 3 provides an insight into the prototype developed, its simulation results and Section 4 elucidates the prototype hardware implementation followed by conclusion in Section 5.

2. BIDIRECTIONAL DC/DC CONVERTER

The proposed converter as shown in Figure 2 has boost converter (half- bridge) followed by a LCC resonant circuit. This LCC combination increases the voltage gain from half-bridge boost and achieves resonance when operated at high frequency. Consequently, high gain is obtained without the use of transformer. In boost mode of operation switches S_1, S_2 conducts and the body diode of S_3, S_4 operates. The dc voltage at low side is converted to pulsed ac at AB. This pulsed voltage output at AB is converted to sinusoidal ac at PQ by the LCC resonant tank. This is fed to the voltage doubler cum rectifier which gives a DC output voltage at high side. In buck mode of operation switches S_3, S_4 and the body diodes of $S_{1,}$ S_2 operates.

The dc voltage at high side is converted to sinusoidal ac at PQ. This sinusoidal voltage output at PQ is converted to pulsed ac at AB by the LCC resonant tank which further gives a gain of 0.39. This is again fed to the rectifier which gives a DC output voltage at the low side. The switches S_1 and S_2 realize ZVS and devices D_{S3} and D_{S4} achieves ZCS. LCC combination is followed by voltage doubler to provide gain of two times in buck operation, the higher voltage is divided to half and further stepped down by the switches S_3 and S_4. Further LCC combination provides ZCS for diodes D_{S1} and D_{S2} and ZVS for switches S_3 and S_4

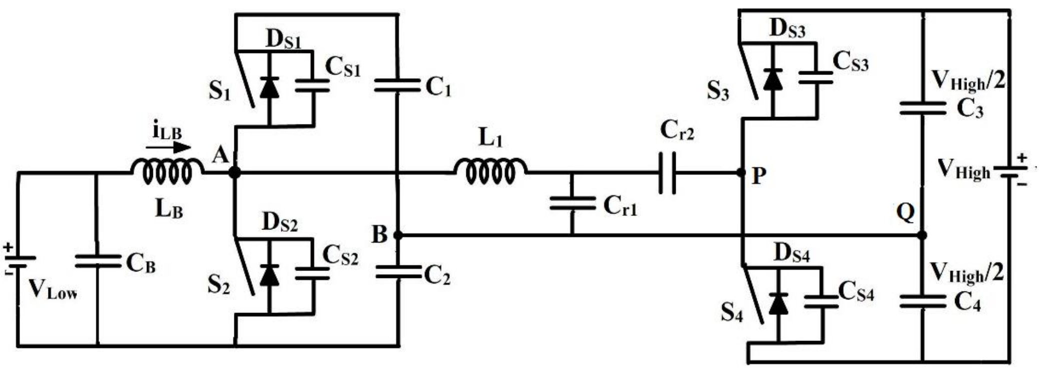


Figure 2. Proposed Bidirectional dc/dc converter

2.1. Boost Mode Operation

The switches S_1 and S_2 are ON and S_3 and S_4 are OFF .Interval-1 as in Figure 4a ($\boldsymbol{t_0 < t < t_1}$**):** At time $t = t_0$,switches S_1 and S_2 are OFF. The difference between the inductor current and the resonant current starts discharging the parasitic capacitor C_{S1} and charges $C_{S2.}$ Power is transferred through the output capacitors C_3 and C_4. At t_1 the parasitic capacitor C_{S1} is discharged and C_{S2} is charged immediately. The current through the switches,

$$i_{S1}(t_1) = 0\,,\; V_{S1}(t_1) = 0 \text{ and } V_{M2}(t_1) = \frac{V_{Low}}{1-d} \tag{1}$$

Where $d = \frac{T_{ON}}{T_S}$; T_{ON} = conduction time of the main switch and T_S = switching time period. The current flowing through the boost inductor i_{LB} and the switch S_1 current i_{S1} are same.

$$\text{i.e. } V_{Low} = L_B \Delta i_1 + C_B \Delta V_{CB} \tag{2}$$

$$L_1 \Delta i_{L1} + C_r \Delta V_{Cr} + C_{P2} \Delta V_{C_{P2}} = 0 \tag{3}$$

Where C_{P2} is the combination of all the other capacitors.

$$V_{Cr} - V_{C4} - C_{r2}\left(\Delta V_{DS4} - \Delta V_{Cr2}\right) + R_4 i_{DS4} = 0 \tag{4}$$

Interval-2 as shown in Figure 4b **(t_1 < t <t_2):** At $t = t_1$, the parasitic capacitor C_{S1} gets discharged completely and C_{S2} gets charged completely as shown in Figure 3a. The difference between the inductor current and the resonant current discharges through anti parallel diode D_{S1} causing zero voltage across S_1. At $t = t_1$, D_{S4} is forward biased. L_1 and C_{r1} start to charge simultaneously,while C_3 and C_4 supply power to the load. Final values are $i_{S1}(t_2) = 0,\ i_{S2}(t_2) = 0;\ V_{S2}(t_2) = \frac{V_{Low}}{1-d};\ V_{S2}(t_2) = 0$.

$$i_{Ds1}(t_2) = i_{LB}(t_2) - i_{L1}(t_2) \tag{5}$$

$$V_{C2} - V_{Low} - L_B \Delta i_B + D_{S1} R_1 \left(i_{L1} - i_{LB}\right) - V_{C1} = 0 \tag{6}$$

Interval-3 as shown in Figure 4c **(t_2 < t < t_3):** At $t = t_2$, switch S_1 is turned on using ZVS, i_{LB} starts decreasing. The current through the resonant inductor L_B decreases linearly through the switch S_1, capacitor C_{S3}, resonant inductor L_1 and resonant capacitor C_{r1}. The diode D_{S4} still conducts to charge C_4 and D_{S3} is reversed biased. The current and voltage expressions are given as

$$i_{S1}(t) = i_{L1}(t) - i_{LB}(t) \tag{7}$$

$$V_{Low} - L_B \Delta i_{LB} - V_{Cr1} - V_{Cr2} = 0 \tag{8}$$

Interval-4 as shown in Figure 4 d **(t_3 < t < t_4):** At this interval S_1 is still in ON state. The anti-parallel diodes at the output side are reverse biased. Load receives the power from the output capacitor C_3 and C_4. At $t = t_4$ switch S_1 is turned OFF.

Here $V_{DS3} = 0,\ V_{S4} = 0,\ V_{S2} = \frac{V_{Low}}{1-d}$; $i_{S1} = i_{LB}$; $i_{LB}(t) = i_{LB}(t_3) - \frac{\left(V_{LB} - V_{Cr1} - V_{Cr2}\right)}{L_B}$ (9)

$$i_{L1}(t_3) = \frac{V_{Cr1} - V_{Cr2}}{L_1} \tag{10}$$

Interval-5 as shown in Figure 4e **(t_4 < t < t_5):** Switches S_1 and S_2 are turned OFF. Parasitic capacitor C_{S1} gets charged completely meanwhile C_{S2} gets discharged. No current flows to the load from input to load end as diodes are not conducting. So load is powered by C_3 and C_4. At this time C_{S2} gets discharged and C_{S1} gets charged to

$$\frac{V_{High}}{1-D}.\quad V_{High} = V_{High/2} + V_{High/2} \tag{11}$$

$$V_{Cr1} - L_2 \Delta i L_2 - D_{S3} V_{Cr2} - V_{High/2} = 0 \tag{12}$$

Interval-6 as shown in Figure 4f (t_5 < t <t_6): Anti parallel diode D_{S2} starts conducting by differences of i_{L1} and i_{LB} where S_2 is provided with gating pulse for ZVS turn-on. Antiparallel diodes in the output side are reverse biased. Therefore, $i_{S1}(t_6)=0,\ i_{S2}(t_6)=0$, $V_{S2}(t_6)=\frac{V_{Low}}{1-d}$, $V_{S2}(t_6)=0.$

$$i_{DS2}(t_6)=i_{LB}(t_6)-i_{L1}(t_6) \tag{13}$$

$$V_{Low}-L_B\varDelta i_B+D_{S2}R_2(i_{L1}-i_{LB})=0 \tag{14}$$

Interval-7 as shown in Figure 4g **(t_6 < t < t_7):** At $t=t_2$ switch S_2 is turned on using ZVS, L_B starts charging. Inductor L_1**,** capacitors C_{r1} and C_{S4} resonate simultaneously. The diode D_{S3} is forward biased and conducts throughout this interval. At $t=t_7$, D_{S3} turns off.

$$i_{LB}(t)=i_{LB}(t_6)+\frac{V_{LB}}{L_B}(t-t_6) \tag{15}$$

$$i_{L1}=-\frac{(V_{Cr1}(t_6)+V_{Cr2}(t_6))}{Z_r} \qquad \text{Where } Z_r=\sqrt{\frac{L_1(C_{r1}+C_{r2})}{C_{r1}C_{r2}}} \tag{16}$$

Interval-8 as shown in Figure 4h **(t_7 < t <t_8):** All output diodes are reverse biased and power is transferred to load by the capacitors C_3 and C_4. Switch S_2 is ON and inductor L_B stores energy in it. At $t=t_8$, S_2 is turned OFF.

2.2 Buck Mode Operation

S_3 /S_4 are ON and S_1 /S_2 are switched OFF for the complete buck operation. Interval 1 as shown in Figure 5a **t_0 < t <t_1):** In the beginning of this interval, switches S_3 and S_4 are turned off. Parasitic capacitor C_{S3} starts discharging and capacitor C_{S4} starts charging via resonant current i_{L2} as shown in Figure 3b. Diode D_{S2} at the output side is forward biased. Energy accumulated in inductor L_B is transmitted to output capacitor C_o via anti parallel diode D_2. There is a power transfer to the load by output capacitor C_o. By the end of this interval parasitic capacitor C_{S3} is completely discharged and parasitic capacitor C_{S4} is completely charged to V_{High}. The final values of components are i_{S3} (t_1) = 0, i_{S4} (t_1) = 0, V_{S3}=V_{High} and V_{S4}=0. Resonant inductor L_1 current is given by

$$i_{D_{S2}}=i_{L_1}-i_{L_B} \tag{17}$$

Interval 2 as shown in Figure 5b **t_1 < t <t_2):** At the beginning of this interval, parasitic capacitor C_{S3} is discharged completely and parasitic capacitor C_{S4} is charged completely. Resonant inductor (L_2) current i_{L2} flows via anti parallel diode D_{S3} resulting in zero voltage condition across switch S_3. Diode D_{S2} still conducts and diode D_{S1} is under reverse bias condition. The final values are i_{S3} (t_2)=0, $i_{S4}(t_2)$=0, $V_{S3}(t_2)$=0 and $V_{S4}(t_2)$=V_{High}. Resonant inductor current L_2 is given by

$$\Delta i_{L_2}=\frac{V_{Cr1}-0.5V_{High}}{L_2} \tag{18}$$

$$V_{Cr1}-V_{Cr2}-V_{CS4}-V_{\frac{High}{2}}=0 \tag{19}$$

$$i_{L_1} = \frac{V_{Cr1} + V_{Cr2}}{Z_r} \quad \text{where } Z_r = \sqrt{\frac{C_3 + C_{r1}}{C_{r2} C_3 C_{r1}}} \tag{20}$$

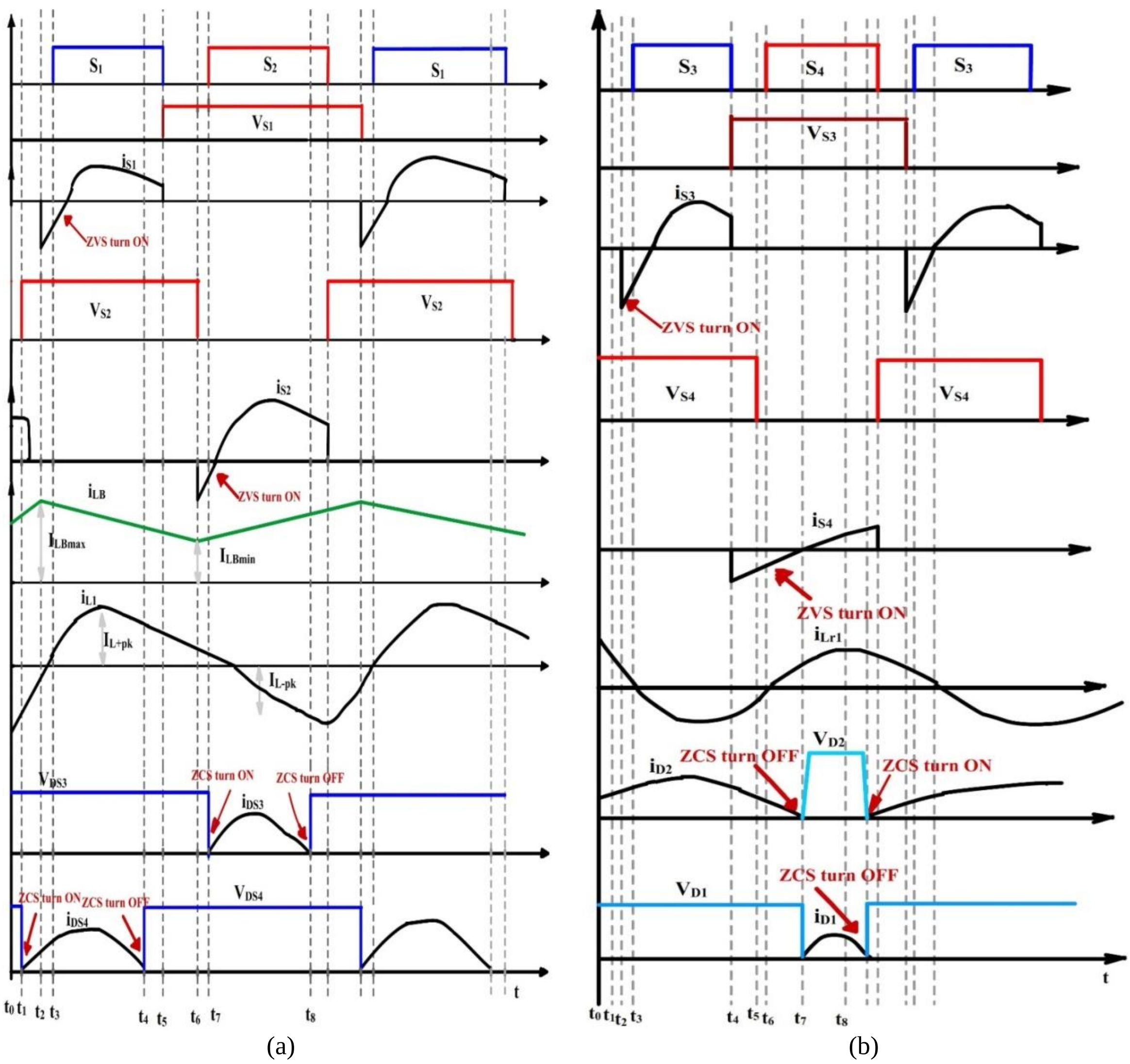


Figure 3. Theoretical waveforms (a) Boost mode operation (b) Buck mode operation

Interval 3 as shown in Figure 5c $t_2 < t < t_3$): When $t=t_2$, switch S_3 is switched on with ZVS. A voltage $V_{High/2}$ is applied on resonant circuit via switch S_3. Resonant capacitor C_{r1} resonates with capacitor C_3. At output end energy is transferred to load by output capacitor C_B. Diode D_{S2} continues to conduct freewheel energy stored in inductor L_B. Resonant inductor (L_1) current i_{L1} continues to flow through diode D_{S2}. This interval ends at $t=t_3$ when switch S_3 is turned OFF.

Interval 4 as shown in Figure 5d $t_3 < t < t_4$): Switches S_3 and S_4 in this interval are turned OFF. Parasitic capacitor C_4 starts discharging and capacitor C_3 starts charging through resonant current i_{Lr2}. Anti-parallel diode D_2 is still in forward biased condition. Power supply to load is provided by output capacitance C_B. When $t=t_4$ parasitic capacitance C_4 is completely discharged and parasitic capacitance C_3 is completely charged to V_H. The final values of these parameters are i_{S3} (t_4) = 0, i_{S4} (t_4) = 0, $V_{S3}=V_H$ and V_{S4}=0.

Interval 5 as shown in Figure 5e $t_4 < t < t_5$): During this interval, the anti-parallel diode D_4 starts to conduct through resonant inductor current i_{Lr2} so that S_4 could be gated for turn on by ZVS. The anti-parallel diode D_2 is still conducting along the output side. By this interval end the anti-parallel diode D_2 turns off by ZCS. The final values of these parameters $i_{S3}(t_5)$=0, $i_{S4}(t_5)$=0, $V_{S4}(t_5)$=0, $V_{S3}(t_5)=V_H$. Interval 6 as shown in Figure 5f $t_5 < t < _{t6}$): At $t=t_5$ switch S_4 is turned on with zero voltage across it. Therefore, resonant current i_{Lr2} is diverted through switch S_4. Anti-parallel diode D_1 is also forward at start of this interval and it start charging capacitor C_5. At $t=t_6$ anti-parallel diode D_1 turns off with zero current. Interval 7 as shown in Figure 5g $t_6 < t < t_7$): None of the anti-parallel diode D_1 and D_2 is conducting. Switch S_4 is turned ON for this complete interval. At $t=t_7$ switch S_4 is turned OFF.

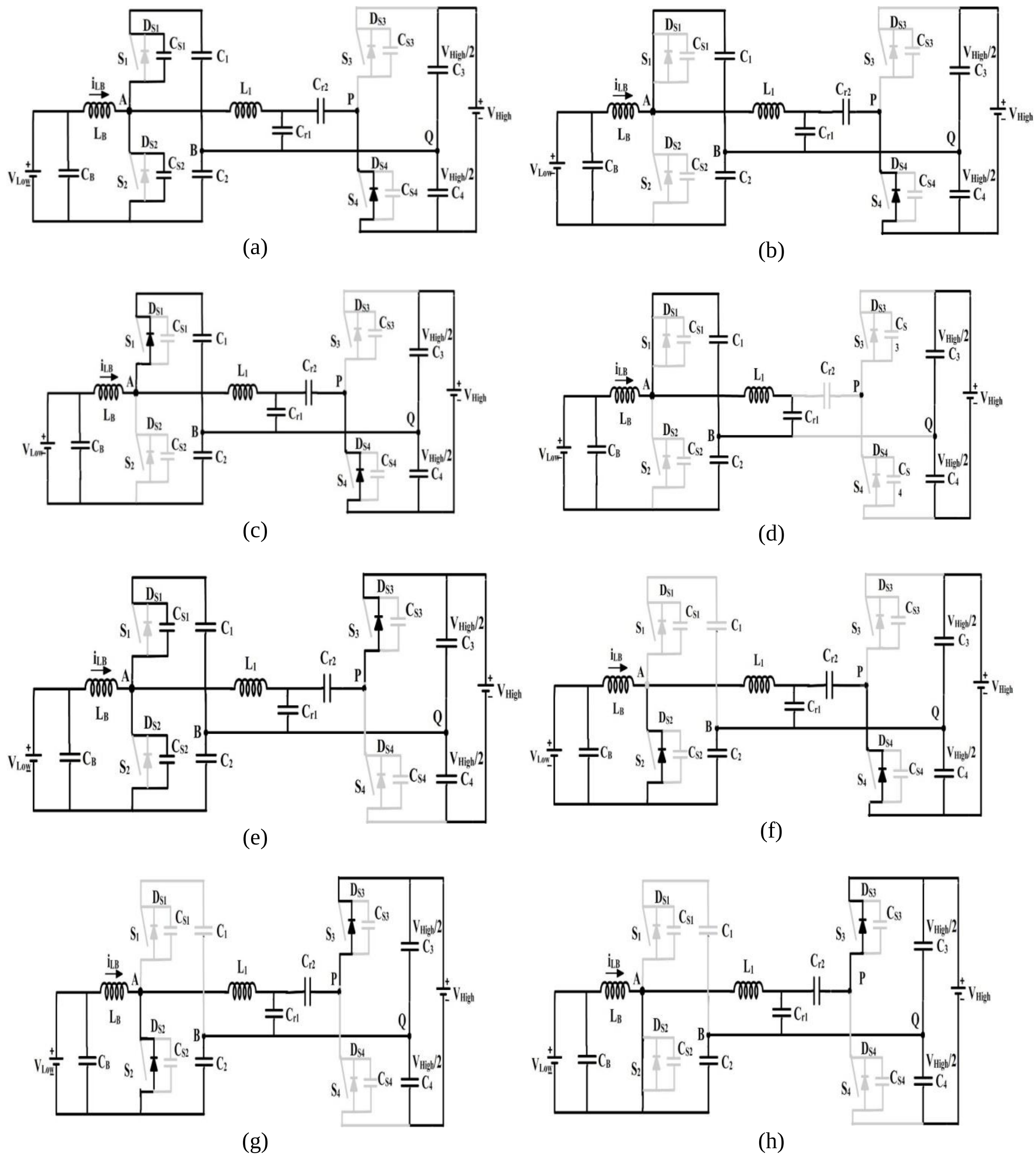


Figure 4. Equivalent circuits during different modes of boost operation

Current through inductor L_B is given by $i_{L_{B1}}(t) = i_{L_B}(t_0) - \frac{V_{L_B}}{L_B}(t - t_0)$ (21)

Current through diode D_{S_2} is given by $i_{D_{S2}}(t - t_0) = i_{L_B}(t - t_0) - i_{L_B}(t - t_0)$ (22)

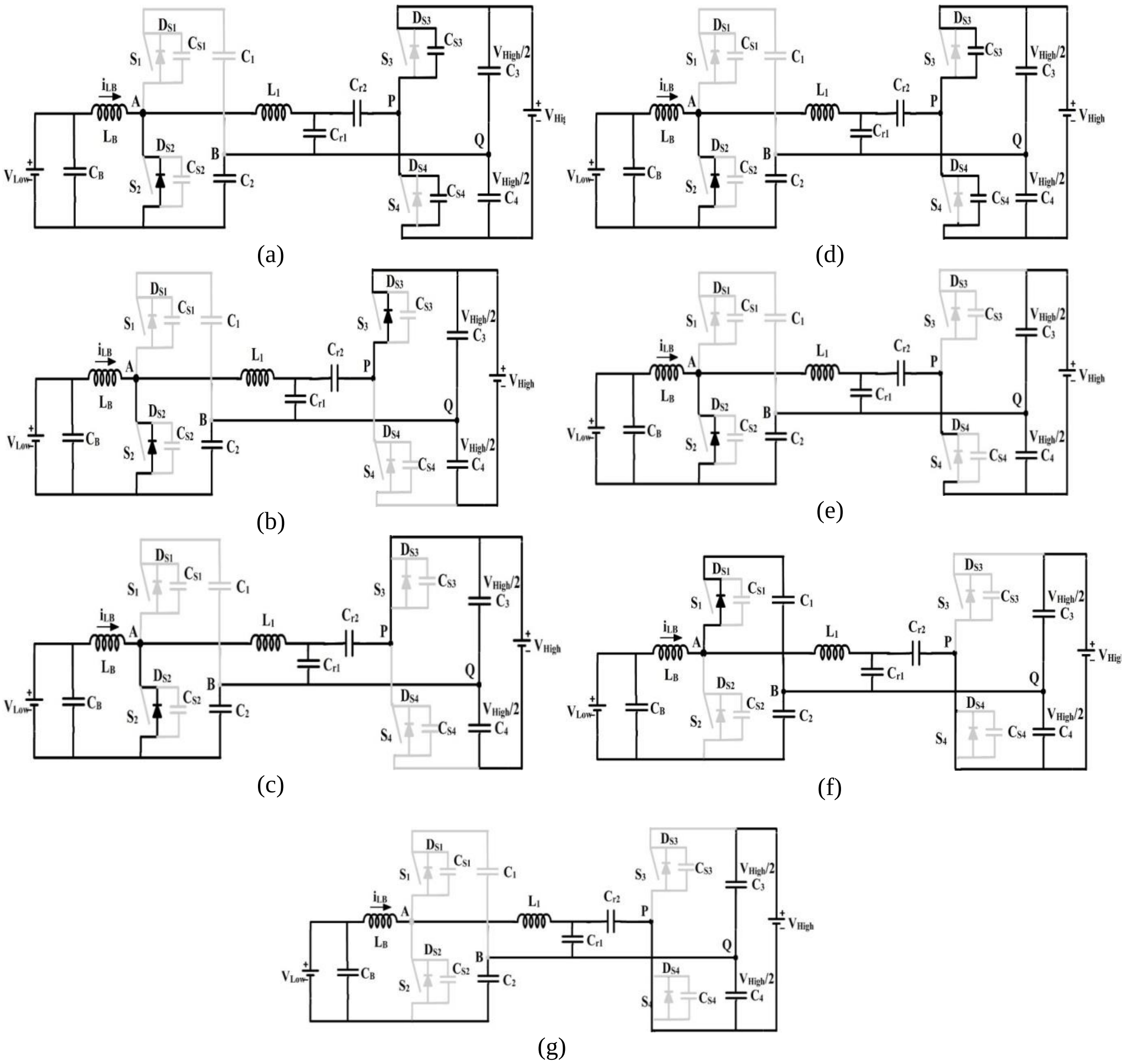


Figure 5. Equivalent circuits during different modes of buck operation

2.3. Gain of the Converter

2.3.1. Boost Mode Gain

The overall gain of the converter is contributed by three stages. The gain given by front end half bridge boost converter is $V_{Low}/_{1-d}$. This is followed by second stage LCC resonant circuit to provide a voltage gain corresponding to the operating frequency. The final stage of the circuit is the voltage doubler enhancing converter gain by two times. Thus overall gain is given by

$$V_{High} = \frac{V_{Low} \bullet G_{boost}(f) \bullet 2 \cdot}{1 - D} \quad \text{where} \quad G_{boost}(f) = \frac{(X_{L1} + R_{ac})R_{ac}}{(X_{L1} + X_{Cr1})(X_{Cr2} + R_{ac}) + R_{ac}} \tag{30}$$

R_{ac} is effective resistance of ac load which is $R_{ac} = {}^{2R_{dc}}\!/_{\pi^2}$, $X_{Cr1}, X_{Cr2}, X_{Cr2}, X_{C2}$ are reactance of C_{r1}, L_1, L_1, C_{r2} respectively. D = duty cycle, f is switching frequency.

2.3.2. Buck mode ratio

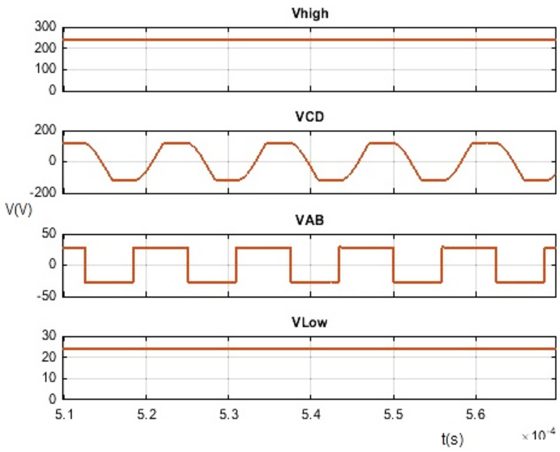
Only half the voltage V_H is applied to the resonant component on account of voltage divider circuit. The overall step down ratio can be expressed as

$$V_{Low} = 0.5 V_{High} D_{Buck} G_{Buck}(f) \tag{31}$$

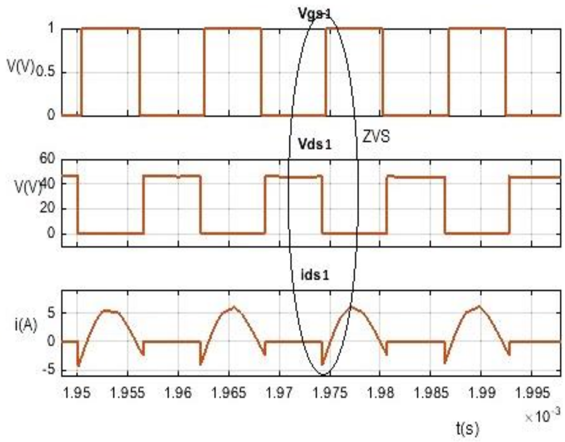
where $$G_{Buck} = \frac{sR_{ac}C_{r1}}{s^2\left(L_1C_{r1} + L_1C_{r2} + C_{r1}C_{r2}R_{L1}R_{ac}\right) + s\left(R_{L1}C_{r1} + R_{L1}C_{r2} + R_{ac}C_{r1} + R_{ac}C_{r2}\right) + 1}$$

3. SIMULATION RESULTS

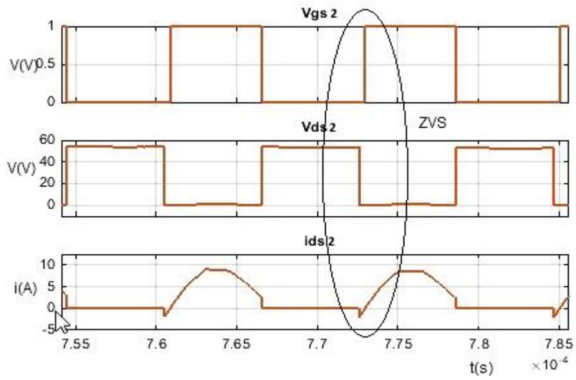
The converter is operated at 83kHz with an input voltage, V_{Low}=24V and output voltage, V_{high}=240V. Duty cycle is 47% with an appropriate dead time. The boost mode waveforms are shown in Figure 6. It is observed that the DC input voltage at low side is converted to pulsed ac voltage at AB (refer Figure 6a, then resonance along with a gain of 5 is achieved at LCC tank giving a sinusoidal ac output at PQ.This sinusoidal output at PQ is rectified to boosted DC output by the voltage doubler. ZVS for switches S_1 and S_2 are depicted in Figure 6b and diodes in Figure 6c. ZCS for the diode is shown in Figure 6d.



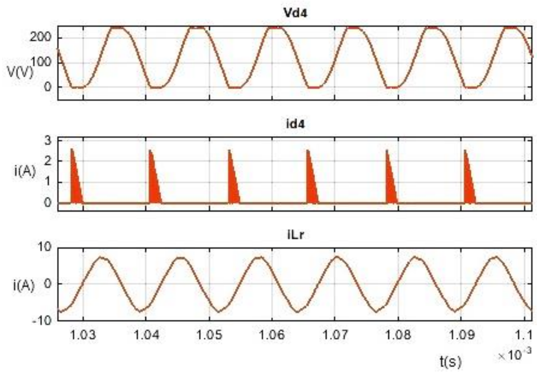
(a)



(b)



(c)



(d)

Figure 6. Simulated waveforms for boost operation (a) Stage wise voltage waveforms including high side input voltage, voltage across PQ, voltage across AB and output at low side (b) Gate source, drain source voltage and current waveforms for switch S_1 (c) Gate source, drain source voltage and current waveforms for switch S_2 (d) Current and voltage waveforms across the diode D_{S4} and resonant inductor.

For Buck mode of operation, the input voltage V_{Low}=200V is supplied and the waveforms are illustrated in Figure 7. It is observed that the DC input voltage at high side is converted to sinusoidal ac voltage at PQ by voltage divider, then resonance along with a gain of 0.39 is achieved at LCC tank gives a pulsed ac output at AB. This pulsed output at AB is converted to DC output by the rectifier.

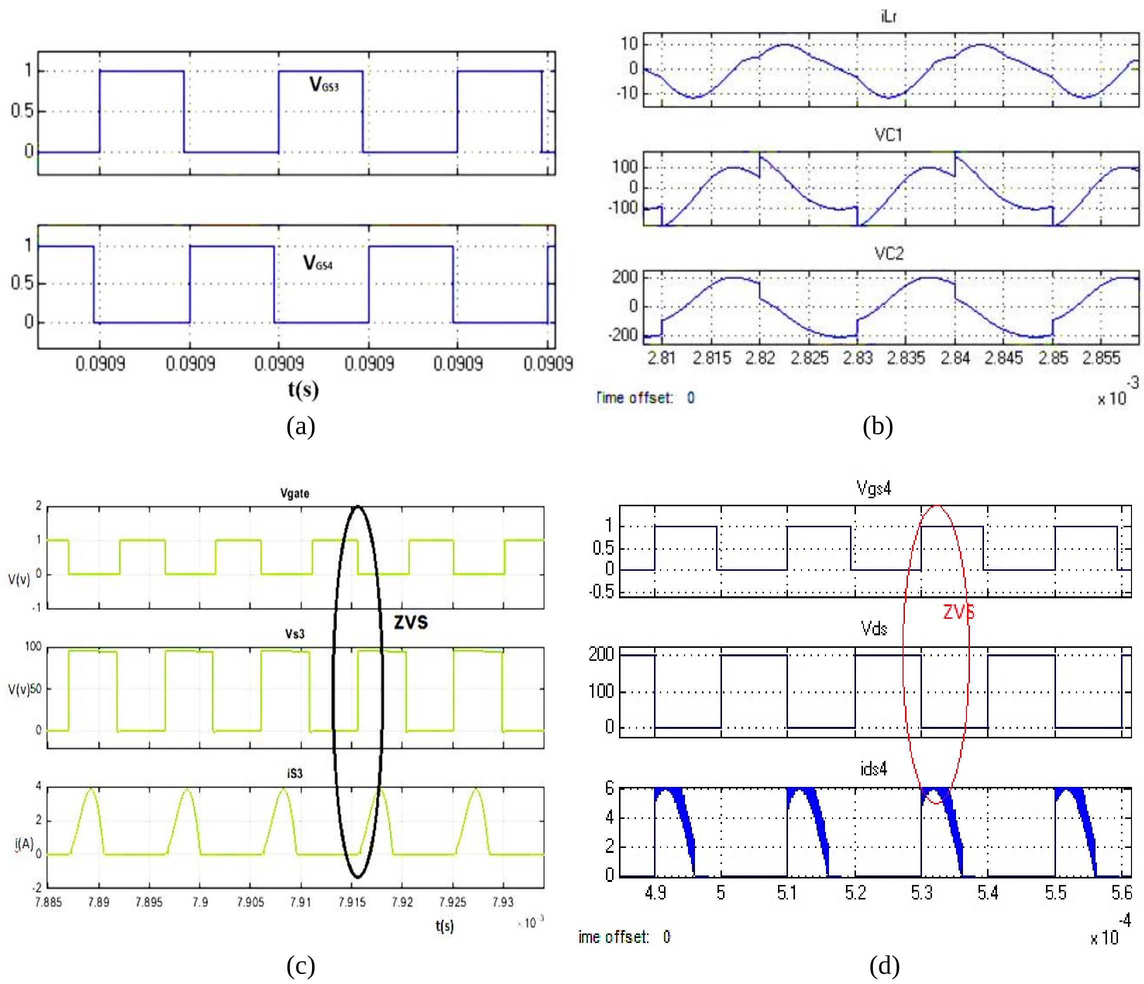


Figure 7. Simulation waveforms for buck operation (a) Gate source voltage for switches S_3 and S_4 (b) Resonant inductor current and resonant capacitor voltage waveforms (c) Gate Source voltage,Drain Source Voltage and Current across Switch S_3 (d) Gate source voltage, Drain Source Voltage and Current across Switch S_4.

4. HARDWARE RESULTS FOR THE CONVERTER

The hardware set up of the converter shown in Figure 8 and the specifications are given in Table 1. The gate pulses to the MOSFETs are provided by DSP board TMS320F2812. TMS320F2812 is chosen due to its high PWM resolution as well as its flexibility in PWM frequency setting.

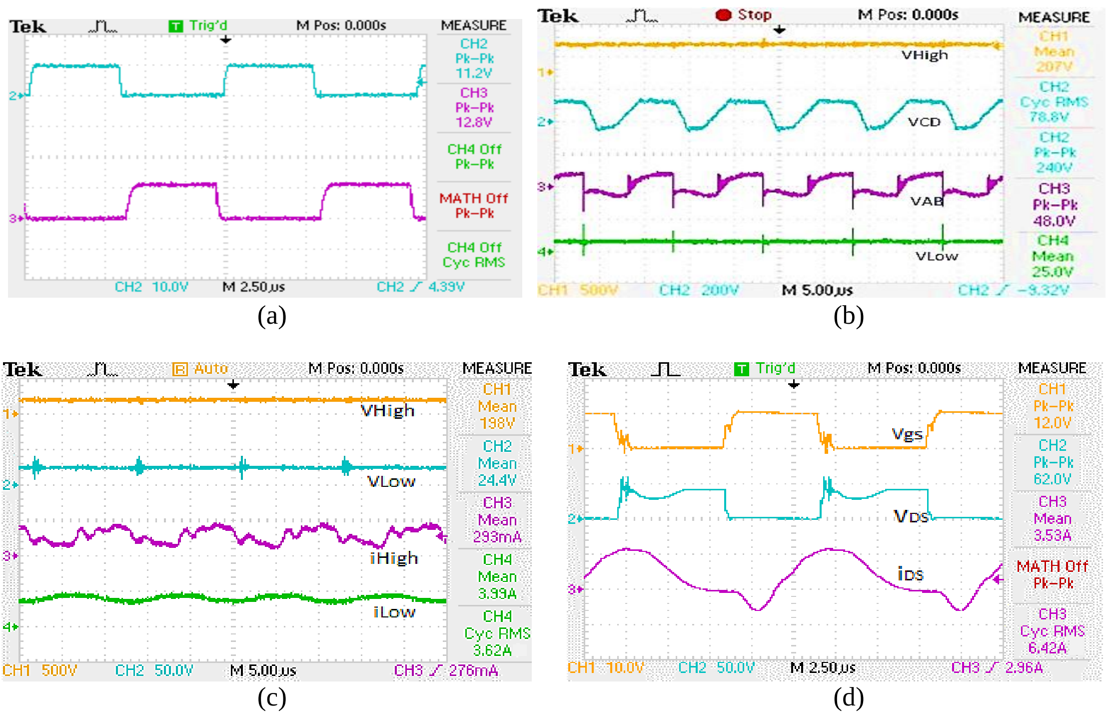


Figure 9(a) Gating pulses for switches S_1, S_2 at 83 kHz (b)Stage wise output voltages at V_{low}=25V including voltages across AB,PQ and high side output voltage(c) Input,output voltage and current waveforms V_{low}= 25V, power = 65W (d)Gate source voltage, Drain source Voltage and Current Waveforms for Switch S_1.

The above setup is operated at a frequency of 83kHz with an input voltage of 24V. It is observed in Figure 9(b) that the DC input voltage at low side is converted to pulsed ac voltage at AB, then resonance along with a gain of 5 is achieved at LCC tank giving a sinusoidal ac output at PQ. This sinusoidal output at PQ is rectified to boosted DC output by the voltage doubler. Figure 9(c) illustrates input, output voltage and current waveforms V_{low}=25V at output power of 65W and Figure 9(d) depicts the gate source, drain source voltage and current waveforms for switch S_1. ZVS for switches S_1 and S_2 are depicted in Figure 10(a) and Figure 10(b). The following are the waveforms observed: Stress across the switch is zero since the voltage across the gate becomes zero before the gate pulse is applied to the switch. Hence, the stress across the switch is made zero everytime without using an additional snubber circuit.

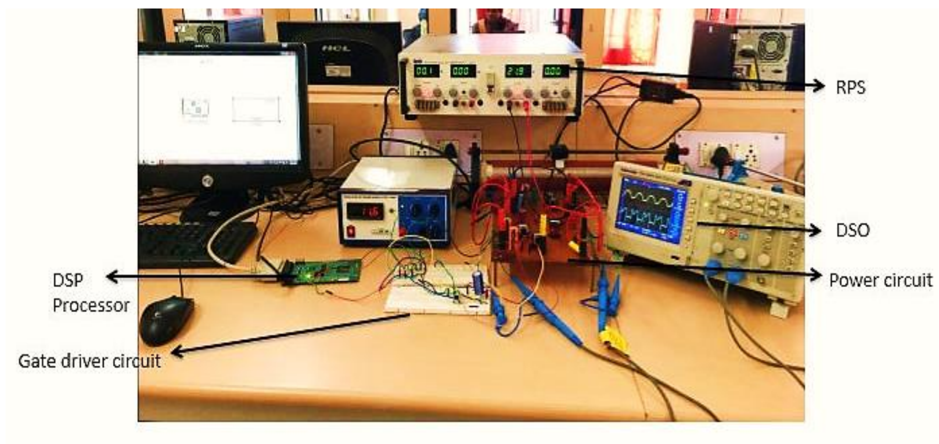
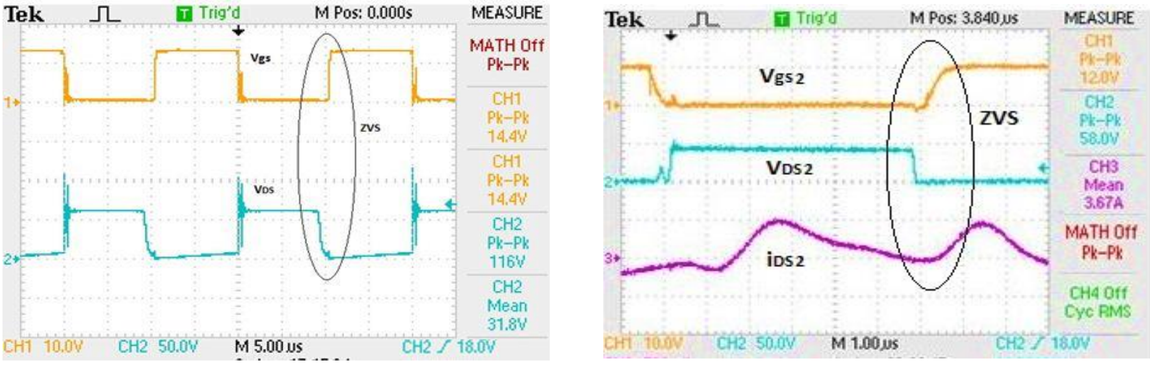


Figure 8. Hardware Setup

Table 1. Design Specifications for the proposed converter

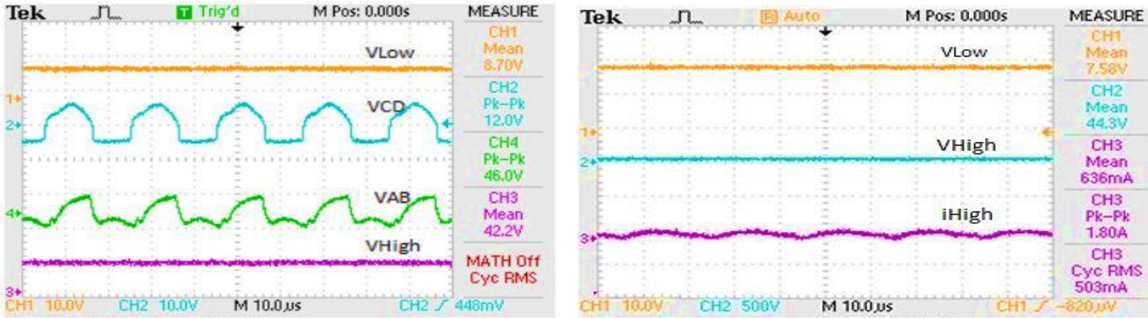
Parameters	Values in Hardware	Parameters	Values in Hardware
Boost Low side voltage V_{low}	24V	L_B	PCV-0-333-12L, Ferrite Bobbin Core, 180µH
Boost High side Voltage V_{high}	207V	L_1	L0451-AL, Ferrite core, 33µH
Buck High side Voltage V_{high}	9V	C_1 and C_2	100µF Electrolytic capacitor,250V
Buck Low side voltage V_{low}	45V	C_{r1} and C_{r2}	0.01µF Polyester capacitor, 400V
Switching frequency f_s	83kHz	C_3 and C_4	33µF Electrolytic capacitor, 450V
Switches, S_1-S_4	IRF740, 400V, 10A	C_o	470µF Electrolytic capacitor, 250V
		DSP Processor	TMS320F2812



(a) (b)

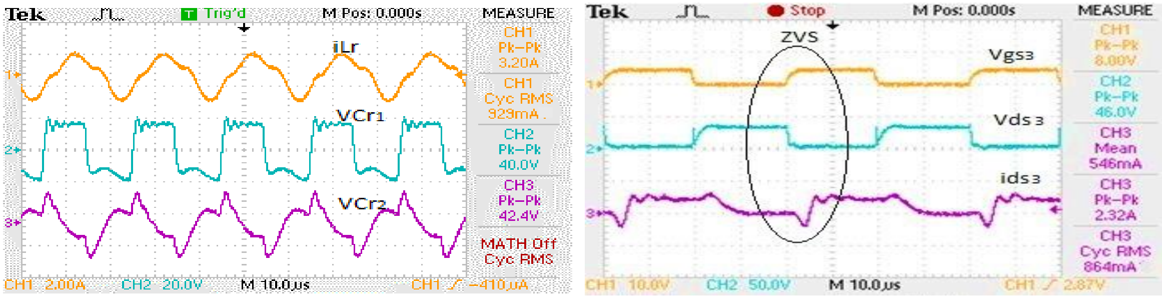
Figure 10(a) Gate source and drain source voltage waveforms for switch S_1 (b) Gate source and drain source voltage and current waveforms for switch S_2

The converter is tested for buck mode of operation as shown in Figure 11. The stagewise waveforms in Figure 11(a) depicts that the soft switching can be achieved from light load to full load condition. Figure 11(b) represents the high voltage and current waveform at light load condition.The voltage and current waveforms across LCC resonant can be observed from Figure 11(c). Zero voltage switching across switch S_3 and S_4 is shown in Figure 11(d) and Figure 12(a). From Figure 12(b), it is observed that the proposed converter operates at maximum efficiency at both boost and buck operation at variable power levels.



(a) (b)

Figure 11. Hardware waveforms in buck mode of operation (a) Stage wise voltage waveforms at V_{High}=45V and power=25W (b) Input voltage and current waveforms at V_{High}=45V

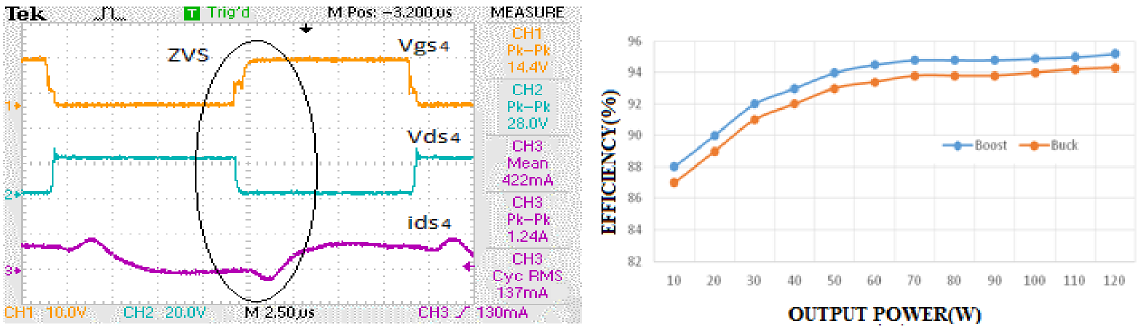


(c) (d)

Figure 11. (c) Voltage and current waveforms across the LCC resonant tank at V_{High}=45V (d) Gate-Source, Drain-Source voltage and current across switch S_3.

5. CONCLUSION

A transformer-less LCC resonant soft-switching bidirectional dc/dc converter is proposed. The key features are high step up/step down ratio, low device voltage stress, ZVS turn-on for all switches and ZCS turn-on and turn-off for all diodes in both buck/boost mode of operation. The proposed converter can achieve ZVS for switches and ZCS for diodes over a wide load range. Device voltage is also clamped without any external snubber circuit. The detailed operation, analysis and design procedure of the converter are presented.



(a) (b)

Figure 12. (a) Gate-source and drain-source voltage and current across switch S_4 (b) P_{out} vs η plot for both boost and buck modes of operation.

Simulation and experimental results have been demonstrated to validate the proposed converter analysis, design and soft-switching. The converter maintains high efficiency for both the direction of power flow. This converter can be used in battery storage applications in micro-grid and hybrid electric vehicles.

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