

Performance Analysis of FPGA based Diode Clamped Multilevel Inverter Fed Induction Motor Drive using Phase Opposition Disposition Multicarrier Based Modulation Strategy

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ABSTRACT

Multilevel inverters (MLI) are becoming more popular over the years for medium and high power applications because of its significant merits over two level inverters. This paper presents an implementation of multicarrier based sinusoidal pulse width modulation technique for three phase seven level diode clamped multilevel inverter. This topology is operated under phase opposition disposition pulse width modulation technique. The performance of three phase seven level diode clamped inverter is analyzed for induction motor (IM) load. Simulation is performed using MATLAB/SIMULINK. Experimental results are presented to validate the effectiveness of the operation of the diode clamped multilevel inverter using field programmable gate array.

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1. INTRODUCTION

Latest trend of multilevel inverters (MLI) is to use medium voltages in industrial drives to meet the power requirements going up to several megawatts. MLI technologies are receiving increased attention for high power applications in power industry. This is due to the improvement in output waveforms compared to two level inverter [1]-[5]. The bipolar junction transistor (BJT), insulated gate bipolar transistor (IGBT), metal oxide semiconductor field effect transistor (MOSFET) switches of the inverter are turned on and off as per the sequence specified by a pulse width modulation (PWM) method to produce ac output waveforms. Multilevel inverters has several advantages such as reduced voltage stress across switching devices, output voltages with less distortion, lower electromagnetic interference, output with near sine waveform, capability of achieving high voltage and high power, lower switching losses etc. The digital control techniques are greatly increased in modern power electronics. For improved performance of the power converter, the controller such as Application Specific Integrated Circuits (ASICs), micro controllers, Field Programmable Gate Arrays (FPGA), Digital Signal Processor (DSP) are responsible. A new breed of inverters called multilevel inverters has been came into existence because a single switching device cannot be directly connected for high voltages. The capacitor voltages in such inverters are switched in a manner to give stepped output waveform that is closer to sinusoidal waveform which is required in electric drive system. Different techniques are used in three types of classical multilevel inverters namely diode clamped inverter, cascaded H-bridge inverter and flying capacitor inverter to achieve such waveforms. The combination of semiconductor switches and capacitors produce output voltage waveforms with smaller steps and the power semiconductors should withstand the reduced voltages. The major advantages of MLI are

quality in waveform, output voltage and input current with less distortion, stress on device is reduced, reduced common mode voltage, switching losses are lower and higher efficiency [6]-[10]. The term multilevel starts from three levels. The concept of multilevel inverter is to perform the power conversion in small voltage steps which utilizing a higher number of active semiconductor devices. This approach has many advantages when compared with the conventional power conversion method. It leads to reduce voltage stress on the load and to produce higher power quality waveforms [11]-[13]. For operating at higher voltages the switches are wired in a series-type connection which is an essential feature of MLI. Due to lower switching losses the multilevel inverters have attracted a great deal of attention in medium and high-power applications [14]-[16]. The MLI structure is presented in Figure 1 for two levels, three levels and n-levels.

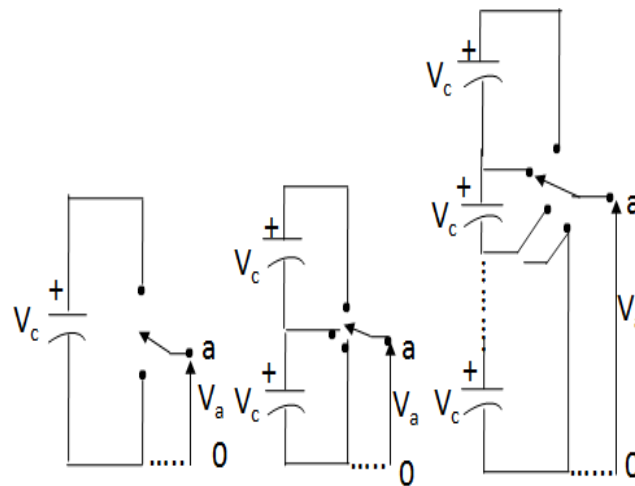


Figure 1. Multilevel inverter structure for (a) Two- levels (b) Three- levels (c) n-levels

2. DIODE CLAMPED MULTILEVEL INVERTER

The diode-clamped MLI was introduced many years ago and there has been vast research especially for medium-voltage applications. A three level diode clamped inverter is also called as “neutral clamped” inverter. It uses diodes to limit the voltage stress of power semiconductor devices. For achieving the desired steps in the output voltage waveform, diode is used as clamping device to clamp the dc bus voltage. It consists of two capacitor voltages in series and has the centre tap which is called as neutral. The three level inverter has two pairs of switching devices in series in each phase leg. Through clamping diodes the centre of each device pair is clamped to the neutral. The quasi-square output voltage waveform is obtained from a three level diode clamped inverter. It can be applied to higher levels. The synthesized output voltage waveform adds more steps as the number of levels increases that leads to sinusoidal waveform with less harmonic distortion. The output voltage waveform with zero harmonic distortion can be achieved from infinite levels. But, due to voltage unbalance problems, voltage clamping requirements, circuit layout and packaging constraints, the number of desired voltage levels is quite limited. The operation of five level diode clamped inverter is explained in this section. To achieve the desired level, four switches are triggered at any point of time.

Table 1 shows the output voltage levels of five level diode clamped multilevel inverter and its corresponding switching states. Here, ‘1’ describes switch in ON position and ‘0’ indicates OFF position. The voltage across each capacitor is $V_{dc}/4$ and voltage stress on each device is limited to $V_{dc}/4$ through clamping diodes to achieve a DC bus voltage V_{dc} . Neutral is the middle point of the four capacitors used. The steps involved for synthesis of five level output voltage are (i) $V_{an}=V_{dc}/2$ is achieved by turning ON of the switches S1 to S4. (ii) one lower switch S5 and three upper switches S2, S3, S4 are turned ON to obtain output voltage of $V_{an}=V_{dc}/4$. (iii) for $V_{an}=0$, two lower switches S5, S6 and two upper switches S3, S4 are turned ON. (iv) one upper switch S4 and three lower switches S5, S6, S7 are turned ON to get $V_{an}= -V_{dc}/4$. (v) all lower switches S5 to S8 must be turned ON for $V_{an}= -V_{dc}/2$.

Table 1. Switching states for five level diode clamped multilevel inverter

V_{an}	S1	S2	S3	S4	S5	S6	S7	S8
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

3. PHASE OPPOSITION DISPOSITION SPWM

For synthesizing the output voltage using different levels of DC inputs, the semiconductor switches must be turned ON and OFF to achieve desired fundamental with less harmonic distortion. This paper presents an implementation of multi carrier pulse width modulation technique i.e., phase opposition disposition. The carrier waveforms above zero reference are in phase as shown in Figure 2 and are 180° out of phase with those below zero for five level diode clamped multilevel inverter using phase opposition disposition (POD) sinusoidal pulse width modulation (SPWM) method. Gating pulses are generated by comparing the sinusoidal reference and four carrier waveforms.

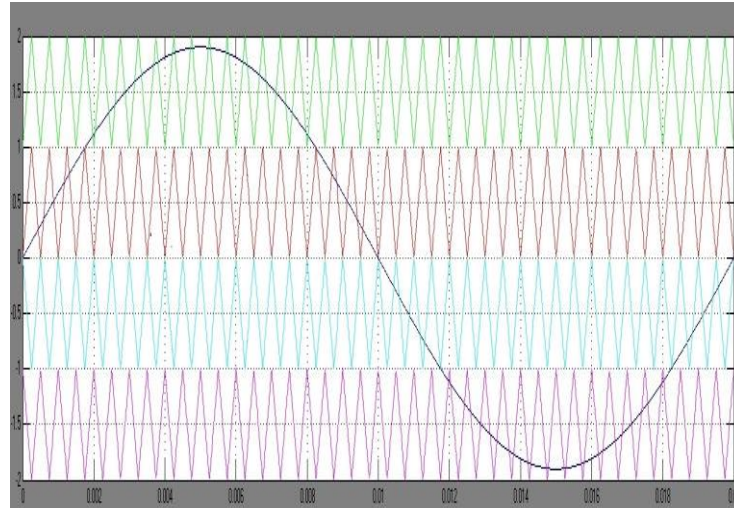


Figure 2. Carrier arrangement using phase opposition disposition for five level diode clamped inverter

In this technique, the modulation signal i.e., sinusoidal waveform is compared with the carrier waveforms. The carriers required for n level inverter are $n-1$. Figure 2 shows a modulating signal and four carriers that are required for five level diode clamped inverter. When the modulating signal is greater than both the upper carriers, we get output voltage of $+V_{dc}/2$. Whenever the modulating signal is greater than first upper carrier, $+V_{dc}/4$ can be obtained. If the modulating signal is higher than the lower carrier but lower than the upper carrier then the output voltage is zero. As the modulating signal is less than the first lower carrier, the resultant voltage obtained will be $-V_{dc}/4$. Similarly, it is switched to $-V_{dc}/2$ whenever modulating signal is less than both lower carriers. The switching pulses in this strategy are generated at every instant of time depending on the comparison of modulating signal and carrier waveforms as seen in Figure 3.

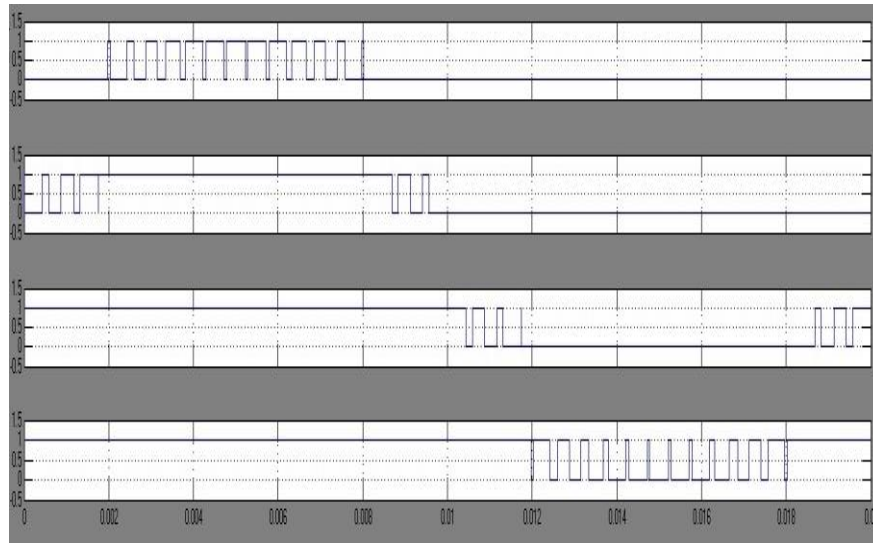


Figure 3. Switching signals generated for five level diode clamped inverter using POD technique

4. RESULTS AND DISCUSSION

The seven level diode clamped multilevel inverter is implemented using MATLAB. Figure 4 depicts the overall simulation diagram of seven level diode clamped multilevel inverter fed squirrel cage induction motor (IM) using phase opposition disposition pulsewidth modulation technique.

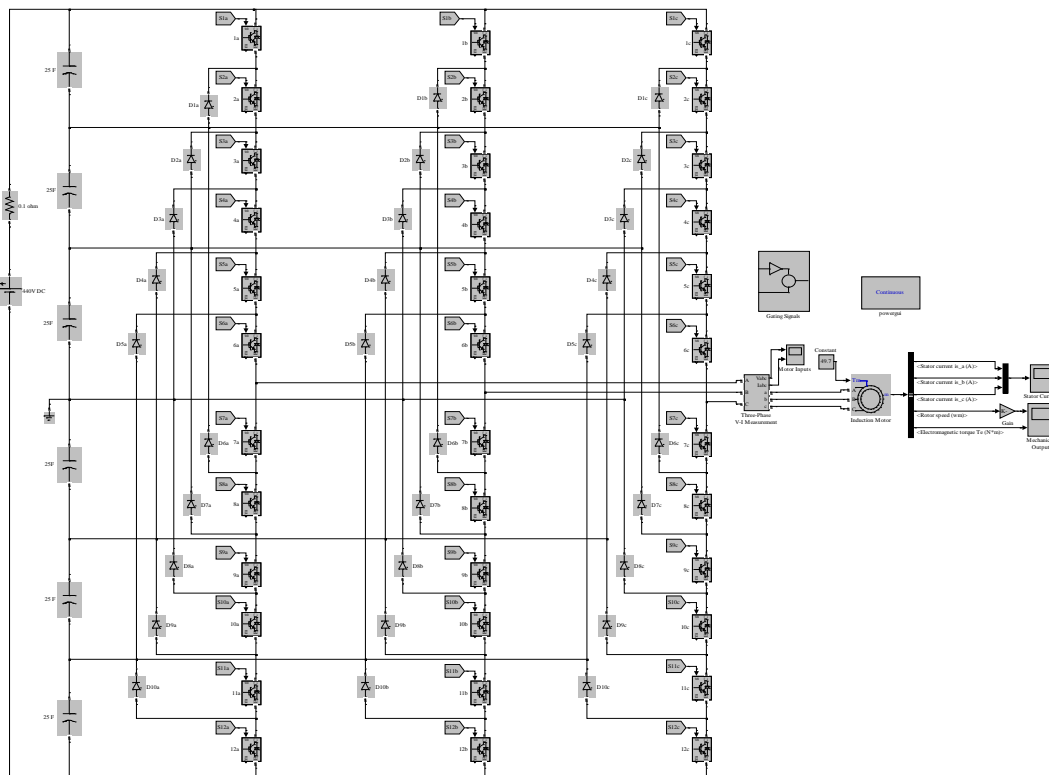


Figure 4. Simulation model of seven level diode clamped inverter fed IM drive using POD technique

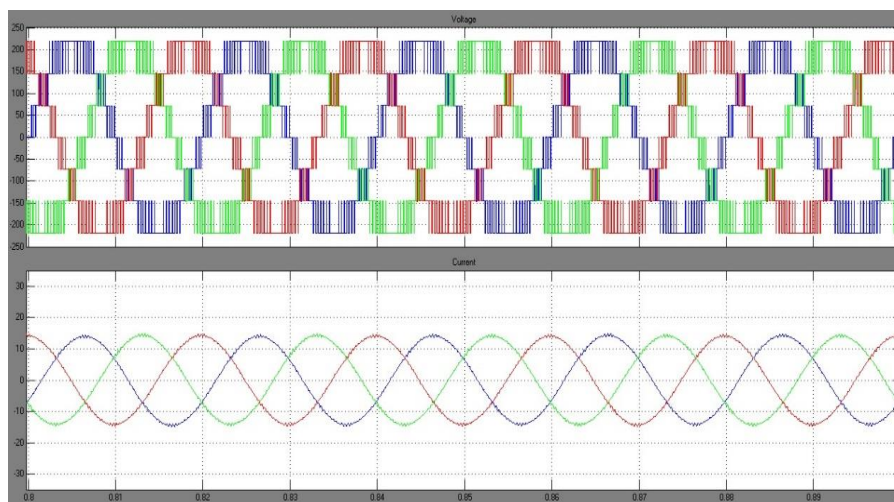


Figure 5. Voltage and current waveforms at half-load

The results of seven level diode clamped multilevel inverter fed induction motor using POD approach are represented from Figure 5 to Figure 9 considering half load torque.

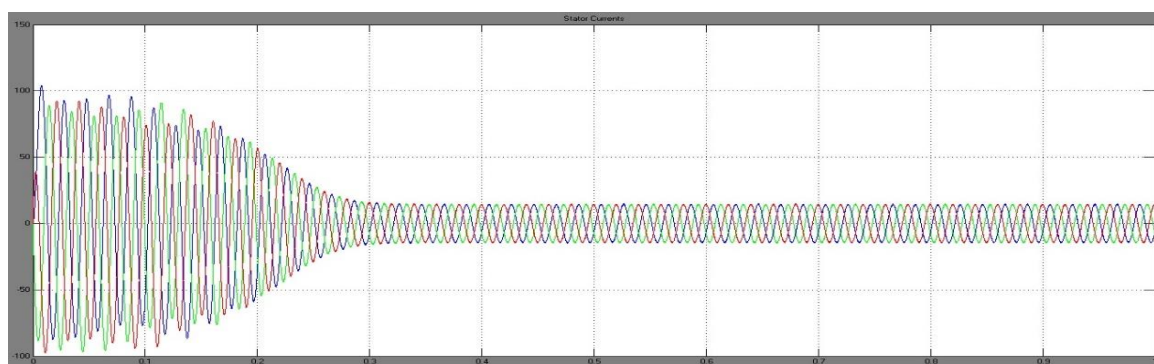


Figure 6. Stator currents at half-load

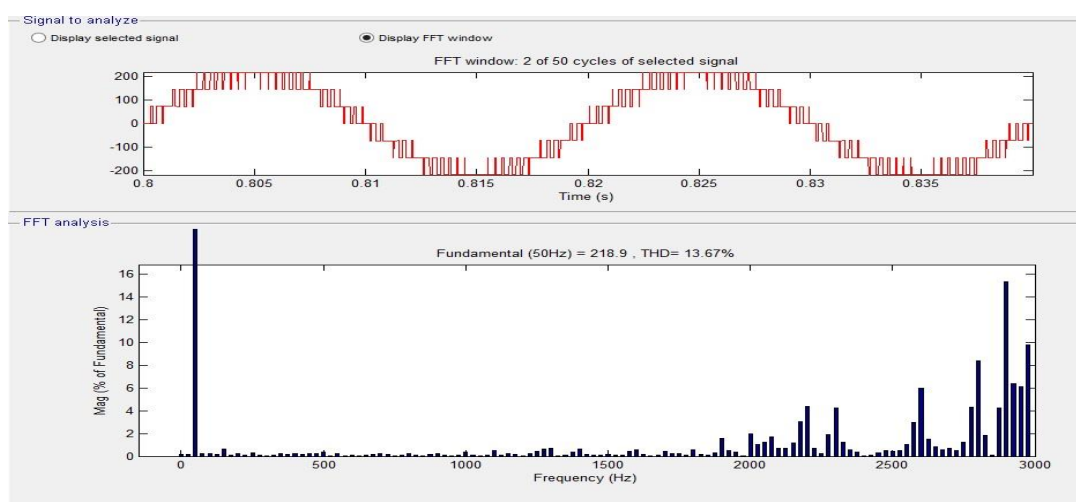


Figure 7. FFT analysis of voltage at half-load

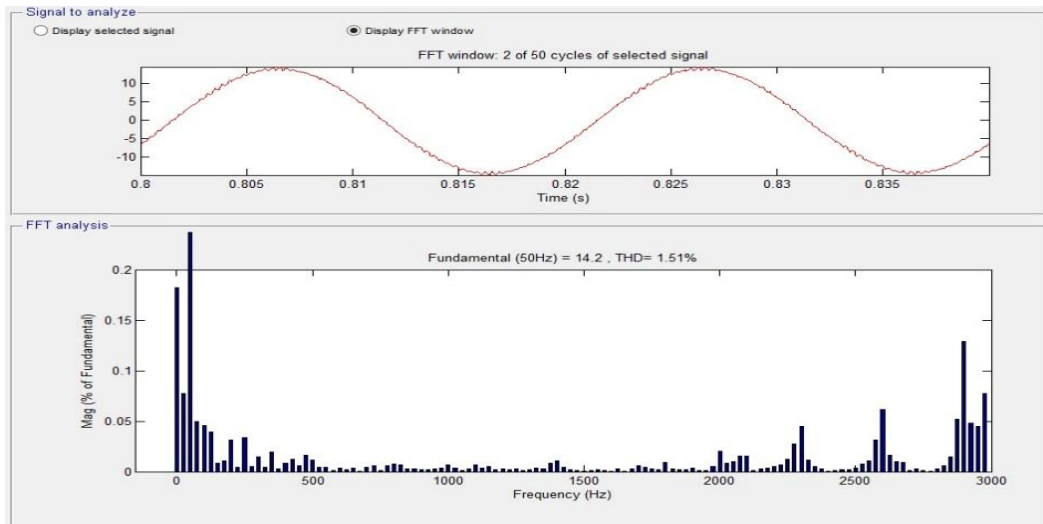


Figure 8. FFT analysis of current at half-load

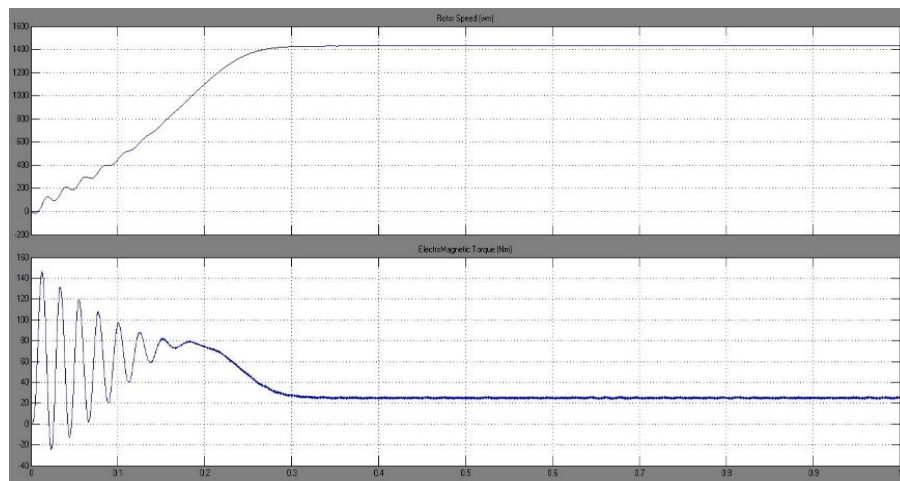


Figure 9. Speed and torque characteristics at half-load

Figure 10 to Figure 14 shows the waveforms obtained using phase opposition disposition method for seven level diode clamped multilevel inverter at full-load torque.

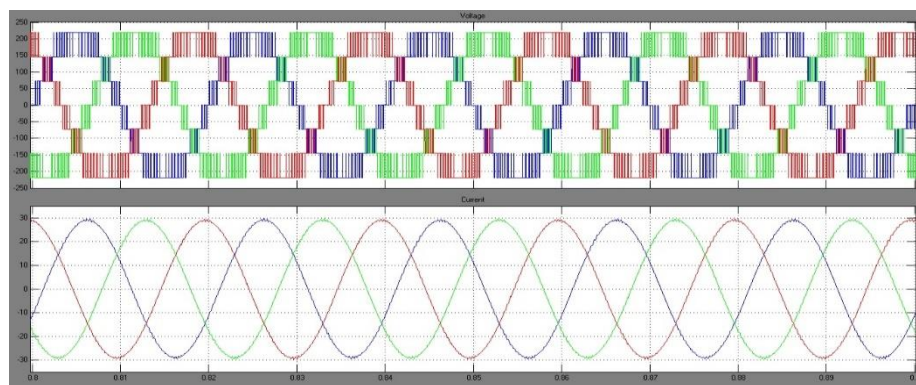


Figure 10. Voltage and current waveforms at full-load

The results of phase voltage and current can be seen in Figure 10. Where as the stator currents are presented in Figure 11.

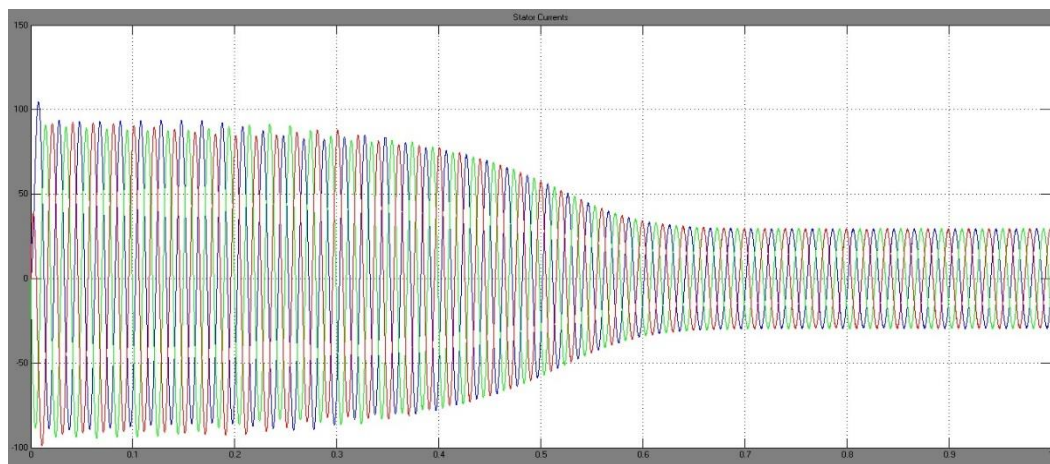


Figure 11. Stator currents at full-load

The FFT analysis is carried out for voltage and current waveforms and is presented in Figure 12 and Figure 13.

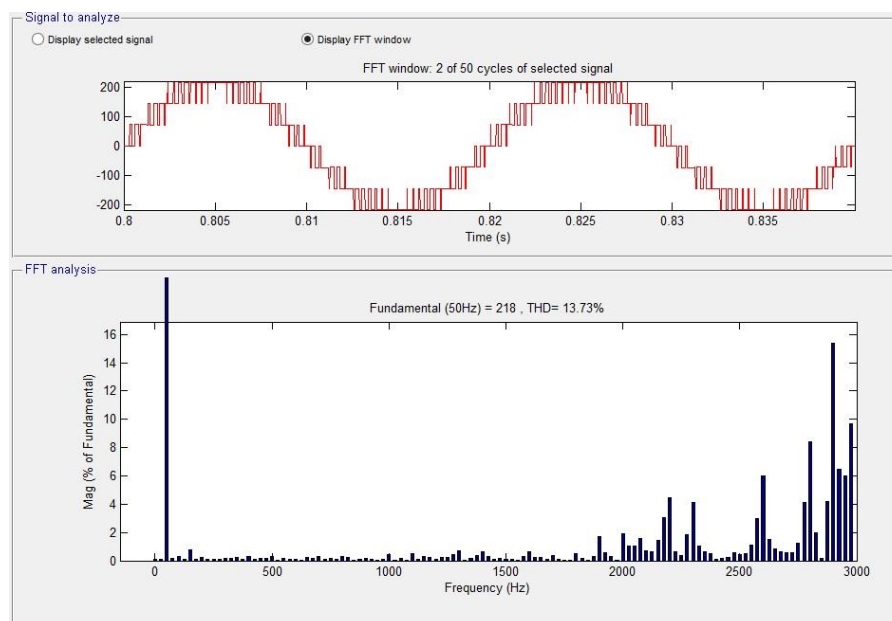


Figure 12. FFT analysis of voltage at full-load

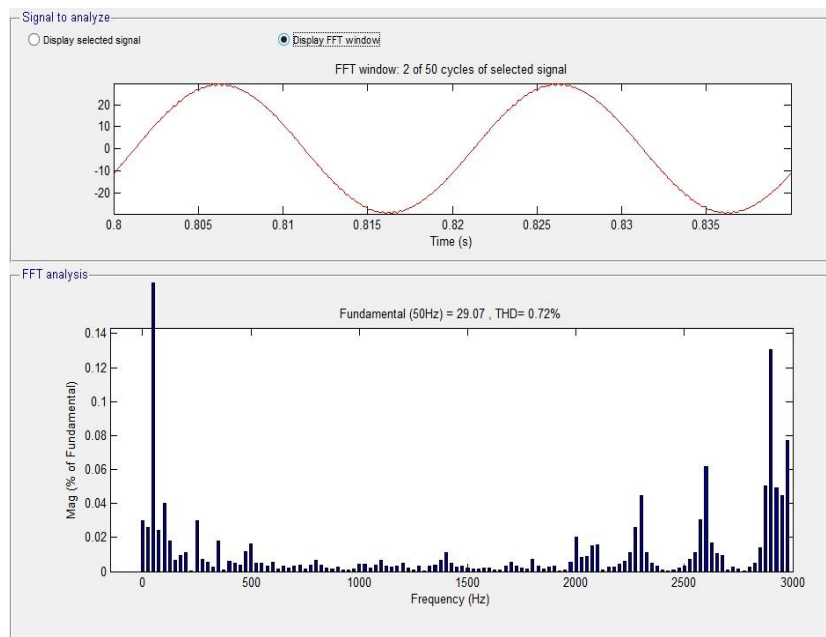


Figure 13. FFT analysis of current at full-load

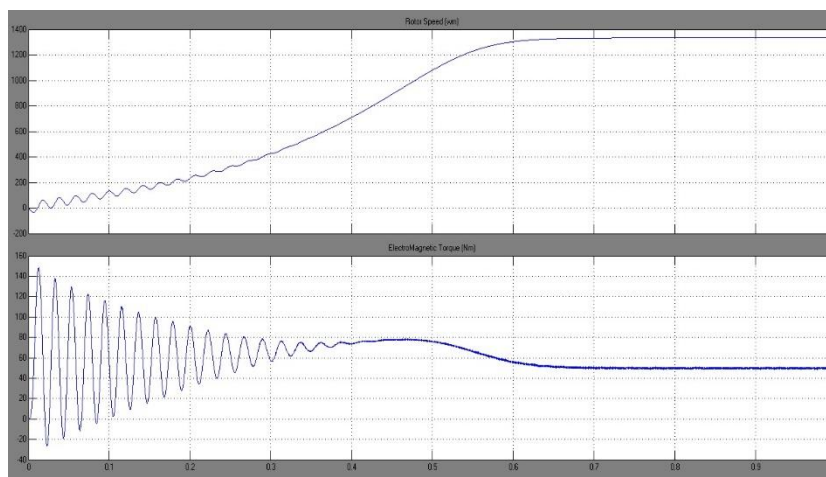


Figure 14. Speed and torque characteristics at full-load

The speed and torque characteristics of motor can be seen in Figure 14 at full load. Table 2 and Table 3 summarizes the FFT analysis carried out at various load torques.

Table 2. Voltage THD (%) of seven level diode clamped multilevel inverter using POD method

S.No	Load Torque	THD
1	No-load	13.59
2	Half-load	13.67
3	Full-load	13.73

Table 3. Current THD (%) of seven level diode clamped multilevel inverter using POD method

S.No	Load Torque	THD
1	No-load	3.9
2	Half-load	1.51
3	Full-load	0.72

5. EXPERIMENTAL RESULTS

The Phase opposition disposition method for seven level diode clamped multilevel inverter is implemented on VPE Spartan 3A DSP board using Xilinx field programmable gate array. The FPGA implements the sinusoidal pulse width modulation scheme in real time for any command reference voltage received, and the digital to analog converter outputs are applied to observe the inverter output voltages. The seven level diode clamped multilevel inverter is implemented by executing the program coding in Xilinx software, then the required gate pulses for the FPGA processor are generated for all the IGBT switches used in the seven level diode clamped multilevel inverter. The hardware setup for seven level diode clamped inverter fed induction motor drive using Xilinx Spartan FPGA Processor is depicted in Figure 15.



Figure 15. Experimental setup for seven level diode clamped MLI fed IM drive

The phase voltage and current waveforms obtained in one phase leg can be seen in Figure 16 by using phase opposition disposition method for seven level diode clamped inverter fed IM.

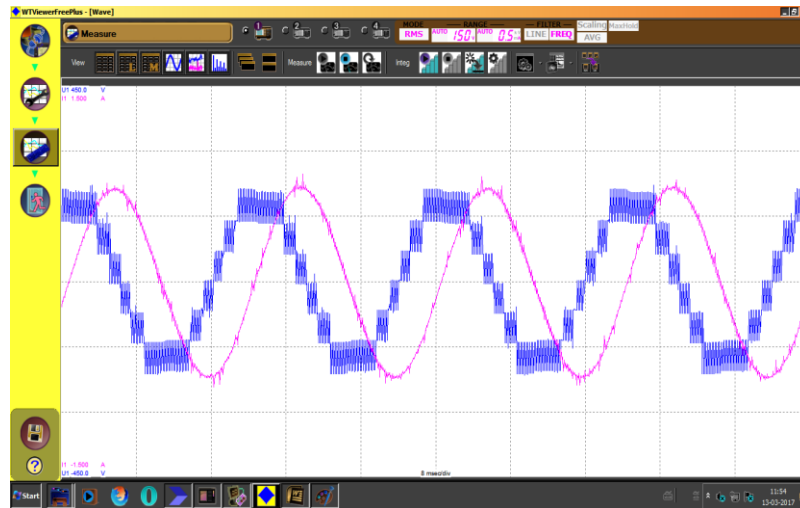


Figure 16. Hardware results of voltage and current in one phase

Similarly the results for three phase voltages and currents are shown in Figure 17.

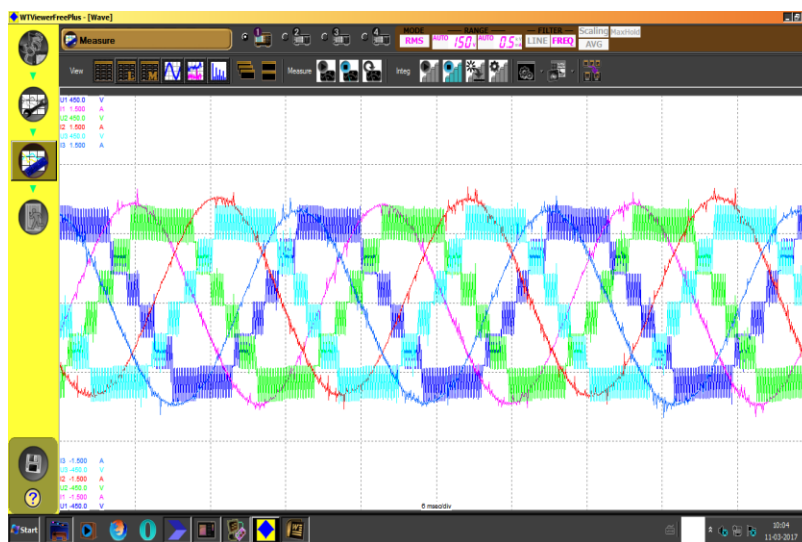


Figure 17. Experimental waveforms of three phase voltages and currents

The software named WTViewerFreePlus is used to record the results achieved for the measured numeric values, harmonic values and data regarding the waveform as shown in Figure 18.

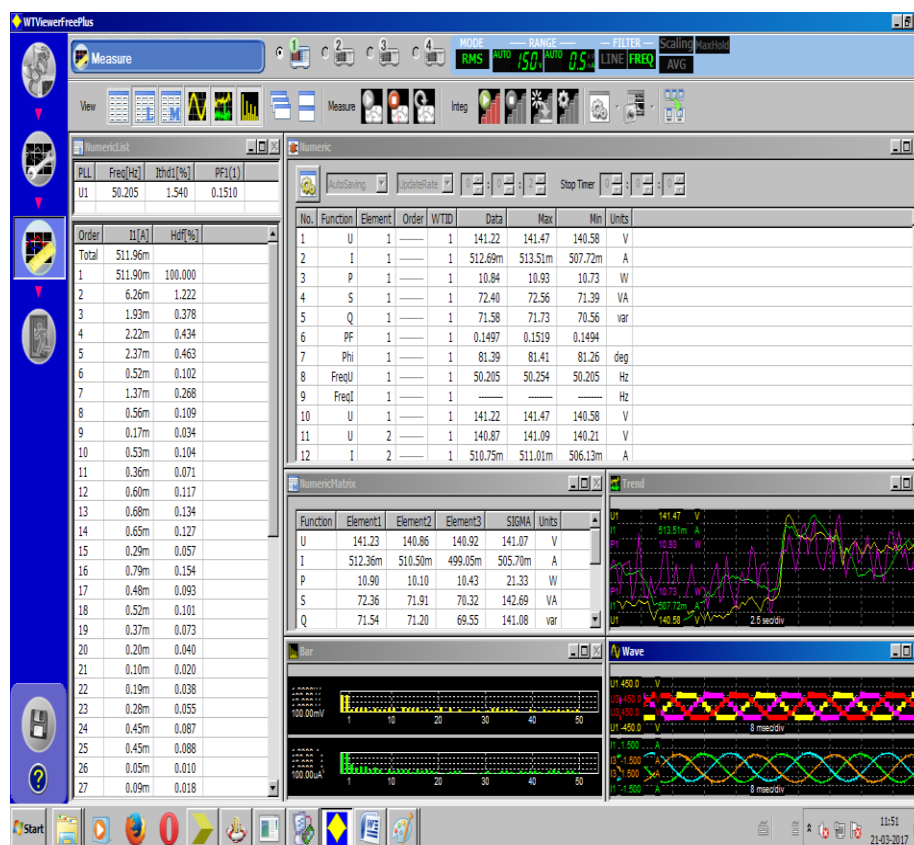


Figure 18. Experimental numeric values measured, harmonic values and waveform data obtained

6. CONCLUSION

This paper has presented the performance of seven level diode clamped inverter using phase opposition disposition approach for induction motor load. The output waveforms of phase voltage, THD spectrum of phase voltage and current, stator current and torque-speed characteristics are obtained for induction motor at various load torque values. The seven level output waveform for diode clamped multilevel inverter is obtained by applying appropriate pulses to the devices through 50 pin connector placed in spartan3ADSP FPGA kit. It is observed that the phase opposition disposition pulse width modulation method provides output with low distortion. However, this strategy can be applied to other multilevel inverter topologies as well.

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