

Selective Harmonic Elimination Based on Newton-Raphson Method for Cascaded H-bridge Multilevel Inverter

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ABSTRACT

Multilevel inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the staircase voltage waveform (from several dc sources) which reduced harmonic content. This paper presents a simple selective harmonic elimination (SHE) modulation for single-phase cascaded H-bridge (CHB) multilevel inverter. The optimum switching angle of the transcendental equations describing the fundamental and harmonic components is solved by means of the Newton-Raphson (NR) method. The proposed SHE scheme is performed through simulation using MATLAB/Simulink. This simulation results are then verified through experiment using Altera DE0-Nano field-programmable gate array (FPGA). The proposed SHE is efficient in eliminating the lowest-order harmonics and producing a higher quality output waveform with a better harmonic profile.

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1. INTRODUCTION

In recent years, the research on multilevel inverters has drawn enormous interest and this technology has been developed for various high power and medium voltage applications. There are three well-established and commercial topologies of multilevel inverters namely, neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor (FC) [1]-[3]. In most topologies, the CHB has attracted special attention as it gives continuous supply to load even if there is fault in any module, thus it is very reliable [4]. In addition, it reduces the number of components used and therefore, the cost of the inverter is less when compared with NPC or FC multilevel inverters.

Generally, modulation techniques of multilevel inverters can be categorized into high-frequency, low-frequency and hybrid switching methods. The multicarrier sinusoidal pulse-width modulation (SPWM) and space vector modulation (SVM) techniques are considered as high-switching frequency schemes [5], whereas selective harmonic elimination (SHE) technique falls under low-switching frequency group [4],[6]. Multicarrier SPWM exploits only one reference waveform which is compared to the multiple numbers of carriers (normally triangular carriers) covering all the range of reference variation. Meanwhile, the SVM is an extension of the standard 2-level space vector modulation to a greater number of levels.

Selective harmonic elimination (SHE) is a non-carrier based PWM technique. It is computed offline, where the switching angles are properly selected to eliminate the most significant low order harmonics among different level inverters [7]. Various algorithms have been developed to calculate the switching angles such as the Newton-Raphson (NR) method [4], particle swarm optimization (PSO) [8] and genetic algorithms (GA) [9]. The combination of both low and high frequency produces a hybrid modulation method.

This study would mainly concentrates on SHE modulation technique using the NR method. The proposed switching technique was adapted to the 7-level symmetrical CHB and 9-level asymmetrical CHB inverter topologies in order to prove the ability of the SHE modulation technique to eliminate the low-order harmonics and thus, reduce the total harmonic distortion (THD) of the inverter outputs.

2. RESEARCH METHOD

2.1. 7-level Symmetrical Cascaded H-bridge Inverter Topology

Figure 1 shows a 7-level symmetrical CHB inverter structure [1] which comprised of three H-bridge cells. Each H-bridge cell is made up of four power switches and a single dc voltage source connected with a dc link capacitor. Through variant of switching sequences of each cell, each inverter cell may produce three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$. In symmetrical CHB inverter, all the dc voltage sources are in equal value [10]. The number of output voltage levels are determined through:

$$n = 2i + 1 \tag{1}$$

where the inverter level is denoted as n whereas i is the number of dc voltage sources. For instance, as three CHB cells with three independent voltage sources are connected together in a cascade, a 7-level output is produced. The output voltage of the inverter, V_{inv} is the sum of the individual inverter output:

$$V_{inv} = V_{a1} + V_{a2} + V_{a3} \tag{2}$$

As for that, the output voltage of the inverter, V_{inv} consists of seven different values which are V_{dc} , $2V_{dc}$, $3V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. Table 1 lists the switching scheme of 7-level symmetrical CHB inverter.

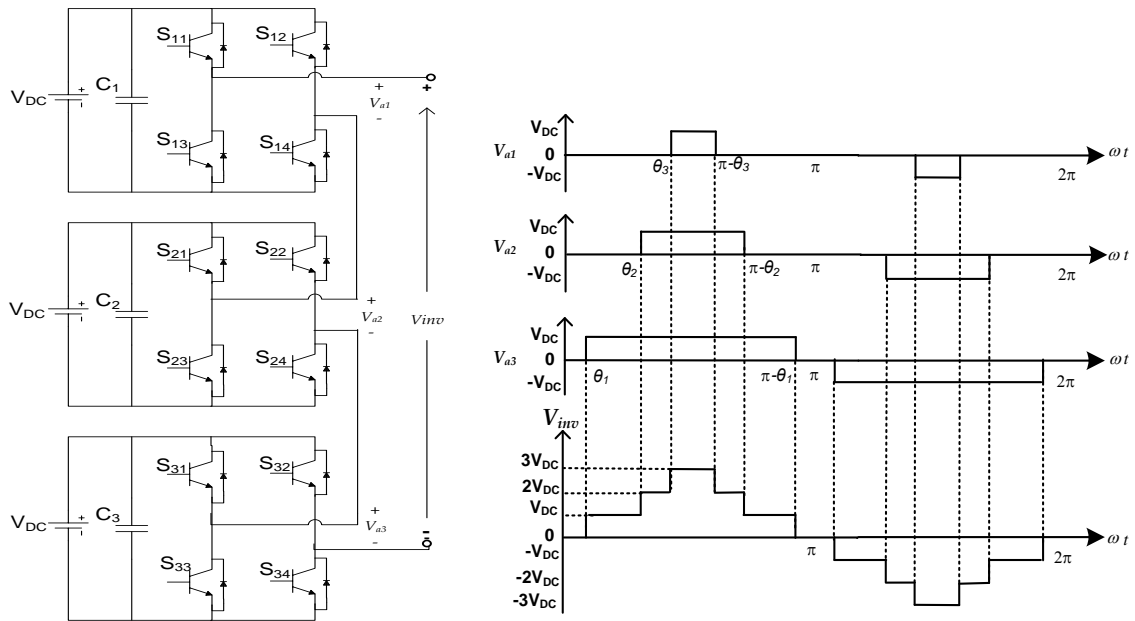


Figure 1. Single-phase 7-level symmetrical CHB inverter topology

Table 1. Switching States of the 7-level Symmetrical CHB

Voltage Level	Switches											
	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₂₁	S ₂₂	S ₂₃	S ₂₄	S ₃₁	S ₃₂	S ₃₃	S ₃₄
$3V_{dc}$	1	0	0	1	1	0	0	1	1	0	0	1
$2V_{dc}$	1	0	0	1	1	0	0	1	0	0	0	1
V_{dc}	1	0	0	1	0	0	1	1	0	0	1	1
0	0	0	1	1	0	0	1	1	0	0	1	1
$-V_{dc}$	0	1	1	0	0	0	1	1	0	0	1	1
$-2V_{dc}$	0	1	1	0	0	1	1	0	0	0	1	1
$-3V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0

2.2. 9-level Asymmetrical Cascaded H-bridge Inverter Topology

The asymmetrical term used in this paper represents the unequal dc voltage sources used at each of the CHB inverter structure [10],[11]. This topology gives an advantage of minimising the number of power switches and dc sources used to compare with the symmetrical CHB topology [12]. In symmetrical CHB inverter topology, four H-bridge cells are required to produce a 9-level output which is determined through (1). The 9-level asymmetrical CHB inverter structure as illustrated in Figure 2 shows that only two H-bridge cells are required to obtain a 9-level output voltage [13]. This can be achieved when the CHB inverter is fed with unequal dc voltage source in the ratio of 1:3. For the proposed structure, Cell 2 is supplied with higher dc voltage in order to reduce the losses since the switching patterns for Cell 2 is simpler than the switching pattern for Cell 1. In general, the number of H-bridge cells required to produce a 9-level output voltage of asymmetrical CHB inverter is determined by:

$$n = 2(1+k)+1 \tag{3}$$

where n is the number of output voltage levels and k is the ratio of dc power supply (i.e $k=3$) for 9-level asymmetrical CHB multilevel inverter case. The output of this inverter topology is given by:

$$V_{inv} = V_{a1} + V_{a2} \tag{4}$$

By proper switching sequences of both cells, the output voltage V_{a1} can be made equal to V_{dc} , 0, and $-V_{dc}$ whereas the output voltage V_{a2} can be made equal to $3V_{dc}$, 0, and $-3V_{dc}$. Thus, the output voltage of the inverter, V_{inv} consists of nine different values which are V_{dc} , $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, and $-4V_{dc}$ as listed in Table 2.

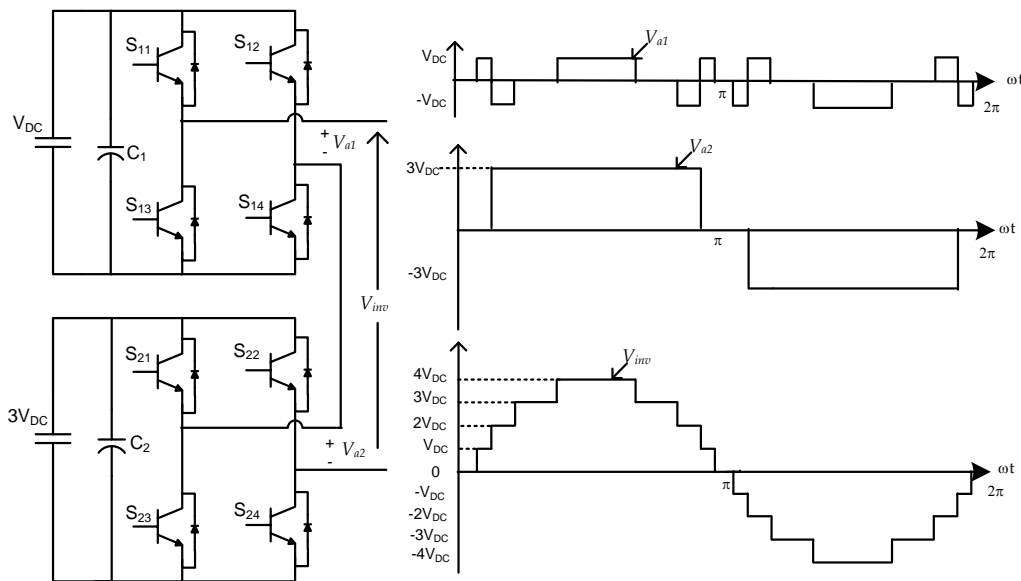


Figure 2. Single-phase 9-level asymmetrical CHB inverter topology

Table 2. Switching States of the 9-level Asymmetrical CHB

Voltage Level	Switches							
	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₂₁	S ₂₂	S ₂₃	S ₂₄
$4V_{dc}$	1	0	0	1	1	0	0	1
$3V_{dc}$	0	0	1	1	1	0	0	1
$2V_{dc}$	0	1	1	0	1	0	0	1
V_{dc}	1	0	0	1	0	0	1	1
0	0	0	1	1	0	0	1	1
$-V_{dc}$	0	1	1	0	0	0	1	1
$-2V_{dc}$	1	0	0	1	0	1	1	0
$-3V_{dc}$	0	0	1	1	0	1	1	0
$-4V_{dc}$	0	1	1	0	0	1	1	0

3. PROPOSED SHE MODULATION

As there exist many strategies for modulation, still, the SHE technique is widely accepted in higher power applications not only in the two-level inverters but also in multilevel inverter topologies. In this paper, the aim of SHE modulation is to produce a staircase waveform with an optimized steps of output voltage waveform in order to cancel some particular low-order harmonics.

Commonly, the stepped voltage for a 7-level inverter using SHE technique is shown in Figure 1. There are three positive steps (V_{dc} , $2V_{dc}$, $3V_{dc}$) during the positive half-cycle of the inverter output waveform. The Fourier expression of the inverter output voltage for the SHE modulation for 7-level inverter can be expressed by:

$$V_{inv}(\omega t) = \frac{4V_{DC}}{n\pi} \sum_{n=1,3,5}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)] \sin(n\omega t) \quad (5)$$

where $\theta_1 - \theta_3$ are the switching angles at each level in the first quarter waveform and need to satisfy the following condition: $\theta_1 < \theta_2 < \theta_3 < \pi/2$. The switching angles can be computed by solving the following equations:

$$\left. \begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= \frac{\pi V_1}{4sV_{dc}} \\ \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) &= 0 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \end{aligned} \right\} \quad (6)$$

As referred to the staircase output waveform of 9-level inverter in Figure 2, the inverter output voltage can be expressed as:

$$V_{inv}(\omega t) = \frac{4V_{dc}}{n\pi} \sum_{n=1,3,5,7}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4)] \sin(n\omega t) \quad (7)$$

with the set of the switching angle of θ_1 to θ_4 implies the same condition as in the 7-level SHE modulation technique where $\theta_1 < \theta_2 < \theta_3 < \theta_4 < \pi/2$. Sets of transcendental equations are required to obtain a proper switching angles for the adopted 9-level asymmetrical CHB inverter. The first equation indicates the fundamental voltage whereas the other equation is used to eliminate specific low-order harmonics, respectively. The resulting harmonic equations are:

$$\left. \begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) &= \frac{\pi V_1}{4sV_{dc}} \\ \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cos(3\theta_4) &= 0 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) &= 0 \end{aligned} \right\} \quad (8)$$

The relationship of the fundamental voltage V_1 with modulation index M can be formulated by:

$$M = \pi V_1 / 4sV_{DC} \quad (0 \leq M \leq 1) \quad (9)$$

where s represents the number of positive steps in a quarter waveform. This produces the desired fundamental voltage, allowing elimination of the most significant low-order harmonic components.

The sets of non-linear transcendental equations in (5) and (7) can be solved via the N-R method, one of the fastest iteration methods where it starts with an initial approximation and converging at the zero of the given set of equations. In this work, the switching angles for both CHB inverters are computed using the Matlab software. The set of switching angles is then examined for its THD to select the best solution (one with the lowest THD). The voltage THD is given as:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad (10)$$

where is V_n the rms value of the n th harmonic component and V_1 is the rms value of the fundamental component.

There are several solution sets of switching angles feasible as modulation indices increase from 0 to 1 for the 7-level CHB inverter as shown in Figure 3(a). Either of these solutions can be used to minimize the selected harmonic. For some modulation indices, no solution set is available, due to the selection of the initial angles. The analytical THD values of those which are calculated according to (9) are illustrated in Figure 3(b). The minimum THD of 10.78% was found at $M = 0.81$. At this point, the switching angles are 9.06° , 28.52° and 55.05° for θ_1 , θ_2 and θ_3 , respectively in which to cancel the 3rd and 5th harmonics of a 7-level CHB inverter.

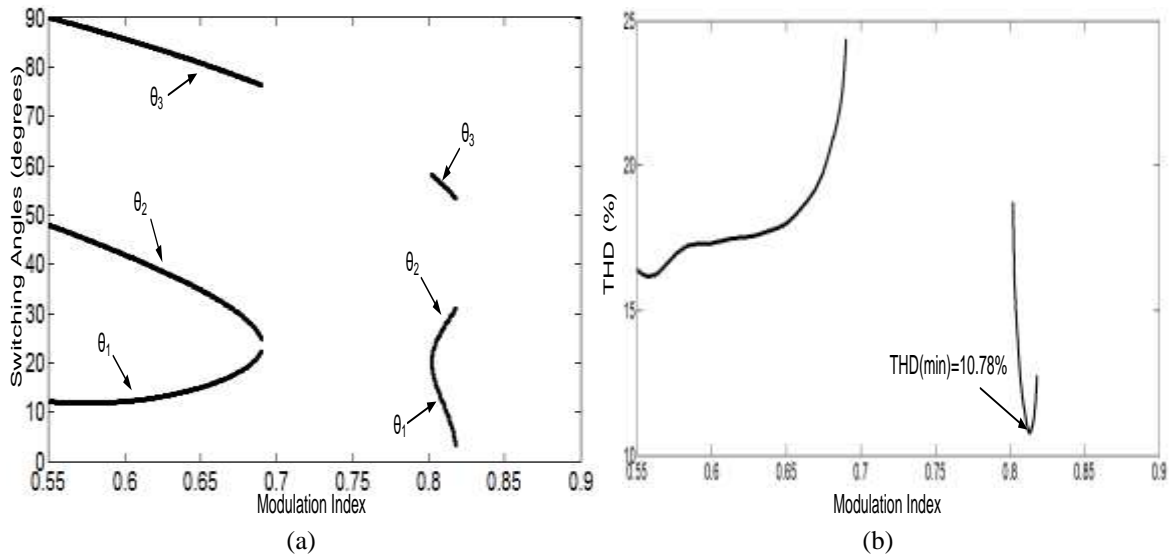


Figure 3. The N-R solutions for 7-level inverter. (a) The switching angles (b) The output voltage THD

The solution sets of switching angles to eliminate the 3rd, 5th, and 7th harmonics in the voltage output of 9-level CHB inverter are as in Figure 4(a). Figure 4(b) shows a 7.95% minimum THD when sets of switching angles of 7.5° , 21.6° , 36.8° and 60.2° are applied. In order to demonstrate the proposed SHE modulation, later, the angle and THD results will be proved in simulation and experiment works using Altera DE0-Nano FPGA.

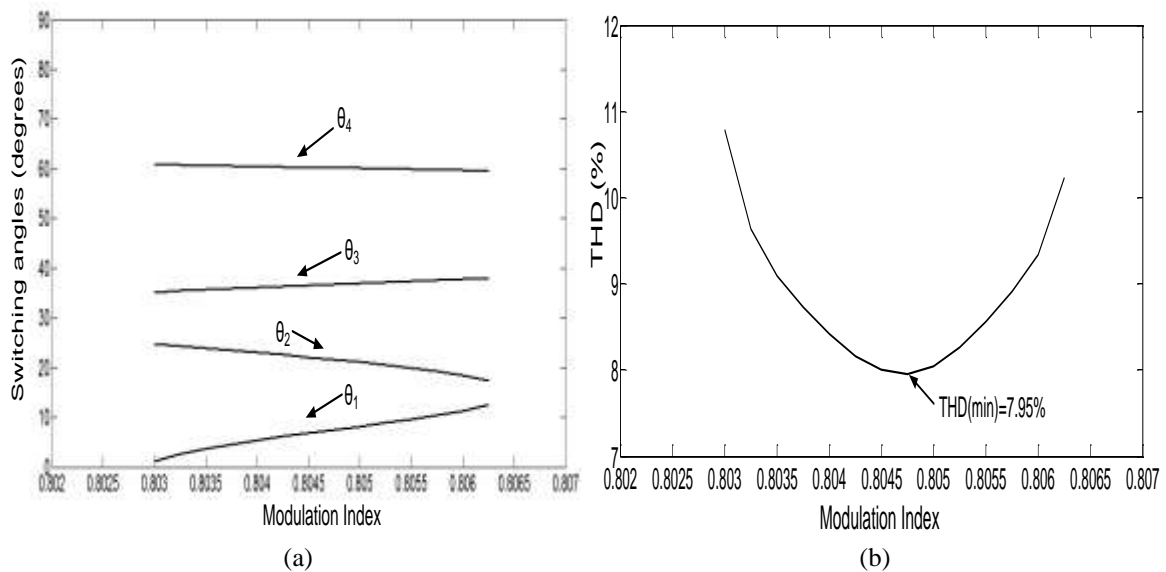


Figure 4. The N-R solutions for 9-level inverter (a) The switching angles (b) The output voltage THD

4. SIMULATION RESULTS

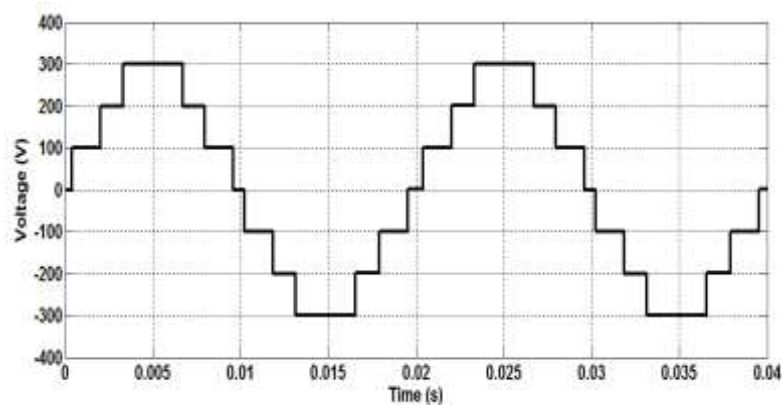
Both 7-level symmetrical CHB inverter and 9-level asymmetrical CHB topologies are simulated using Matlab/Simulink in order to verify the adopted structures with the switching strategies. The simulations are conducted by applying the set of the switching angles in order to eliminate certain harmonic contents as in Table 3.

The 7-level symmetrical CHB inverter structure is incorporated with three equal dc voltage sources of 100V in each cell. Figure 5(a) illustrates the inverter output voltage while the voltage THD is shown in Figure 5(b). The voltage THD of 7-level CHB is 11.90%, approaching the calculated value as in Figure 3(b). Note that the 3rd and 5th harmonics are eliminated in this simulation when the set of switching angle are assigned.

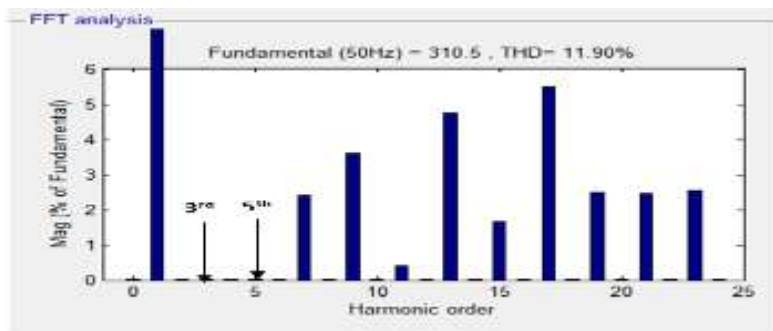
The 9-level asymmetrical CHB inverter topology consists of two unequal dc voltage sources, each source is 100V and 300V, respectively. The inverter output voltage and voltage THD are shown in Figure 6(a) and Figure 6(b), respectively. Based on the simulation results of the 9-level CHB inverter, the voltage THD is 9.40% which is lower than the 7-level CHB inverter's voltage THD. As calculated previously, the 3rd, 5th and 7th harmonic contents are eliminated.

Table 3. Switching Angles for 7-level and 9-level CHB Inverters

Cases	M	Switching Angles ($^{\circ}$)
7-level Symmetrical CHB	0.81	9.06°, 28.52°, 55.05°
9-level Asymmetrical CHB	0.8047	7.5°, 21.6°, 36.8°, 60.2°



(a)



(b)

Figure 5. The 7-level symmetrical CHB inverter. (a) The output voltage (b) The output voltage THD

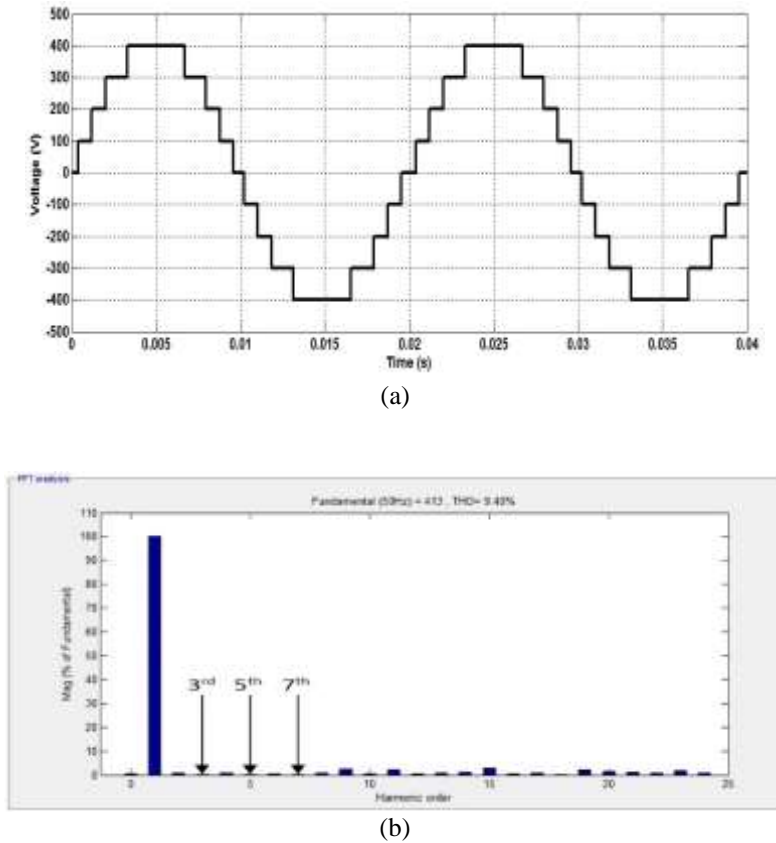


Figure 6. The 9-level asymmetrical CHB inverter. (a) The output voltage (b) The output voltage THD

5. EXPERIMENTAL VALIDATION

To validate the simulation results of both CHB structures and control algorithm, the experiment were set up as in Figure 7, utilizing DE0-nano Altera FPGA as the controller. The switching sequences with set of angels are designed in Quartus IV software by applying the Look-Up Table (LUT) techniques. The prototype of single-phase CHB used the IGBTs with built-in fast recovery diode as the power switching devices. An additional snubber circuit comprises of a resistor and a capacitor are added in parallel with each IGBT in order to minimize the large over currents and over voltages through the devices during turn ON and turn OFF period [14]. The resistor of 100Ω is used as the load of the inverter. The inverter output voltage waveform is measured and obtained using Tektronix DP04054 Digital Phosphor Oscilloscope. The output voltage THD is measured using the FLUKE 43B Power Quality Analyzer.



Figure 7. The experimental setup

Figure 8 shows the experimental results of 7-level CHB inverter when tested with resistive load, connected to three H-bridge cells. Each H-bridge cell is supplied with 60V dc voltage. Figure 8(a) illustrates the output voltage waveform of 7-level CHB inverter. The inverter output voltage THD is 10.3%. As it is obvious in Figure 8(b), the 3rd and 5th harmonics are eliminated.

The experiment for 9-level CHB inverter is conducted by using two H-bridge cells. Each H-bridge cell is connected with unequal dc voltage sources in the ratio of 1:3 ($V_{a1} = 20V$, $V_{a2} = 60V$). The results of the experiment as shown in Figure 9. The inverter output voltage waveform is as in Figure 9(a). As shown in Figure 9(b), the inverter output voltage THD generated from the 9-level CHB inverter prototype is 8.2% with the 3rd, 5th and 7th harmonic orders are eliminated.

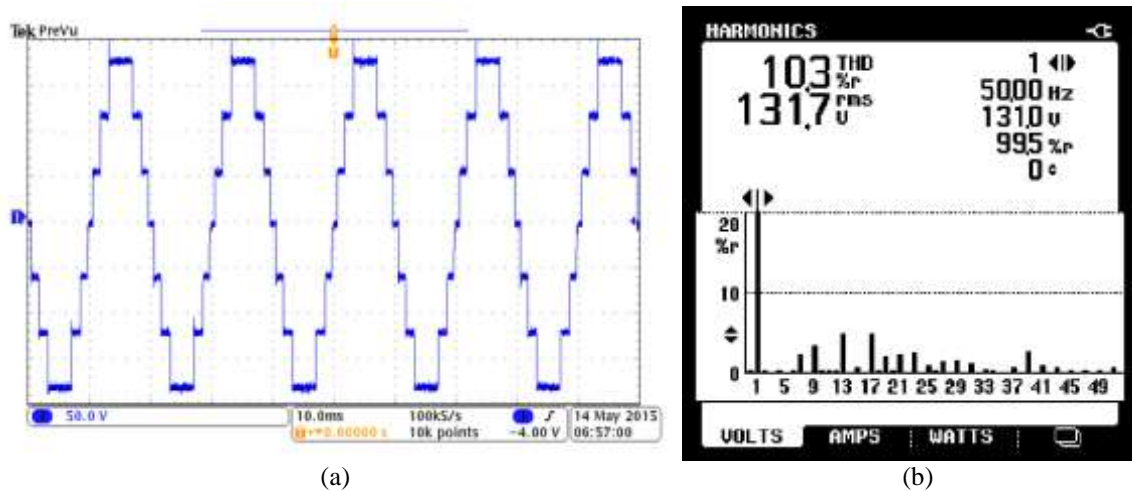


Figure 8. The 7-level symmetrical CHB inverter (a) The output voltage waveform (b) The output voltage THD

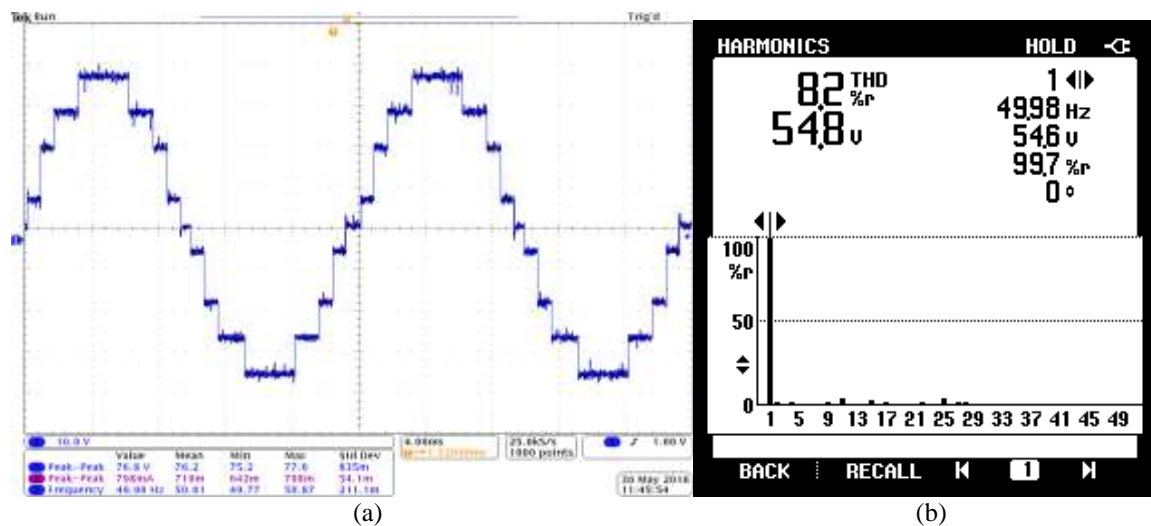


Figure 9. The 9-level asymmetrical CHB inverter (a) The output voltage waveform (b) The output voltage THD

6. CONCLUSION

This paper presented the selective harmonic elimination based on Newton-Raphson method for two CHB inverter topologies, 7-level symmetrical and 9-level asymmetrical CHB inverters. The simulations of the proposed SHE scheme were verified experimentally for a single-phase CHB inverter prototype. The proposed switching angles for both cases are capable to eliminate certain low order harmonic contents thus

help in reducing the THD in the output voltage. The results show that the THD of the 9-level asymmetrical CHB inverter is much less than the 7-level symmetrical CHB inverter. Future work of the proposed SHE modulation could be implemented for higher level of CHB structure and other multilevel inverter topologies.

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