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Five-level PWM Inverter with a Single DC Power Source for DC-AC Power Conversion

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ABSTRACT

This paper presents a circuit configuration of five-level PWM voltage-source inverter developed from the three-level H-bridge inverter using only a single DC input power source. In the proposed five-level inverter, an auxiliary circuits working as the voltage balancing circuits of the inverter's DC capacitors is presented. The auxiliary circuits work to keep stable DC capacitor voltages of the inverter, and also to reduce the capacitor size of the inverter. The unique point of the proposed balancing circuits is that it needs only a single voltage sensor to control the voltages of the two capacitors in the inverter. Moreover, a minimum number the inverter's switching devices is also an important feature of the proposed inverter topology. A simple proportional integral controller is applied to control the voltage of the DC capacitors. The proposed topology is tested through computer simulation using PSIM software. Laboratory experimental tests were also conducted to verify the proposed inverter circuits. The computer simulation and experimental test results showed that the proposed balancing circuits works properly keeping stable voltages across the two DC capacitors of the inverter using only a single voltage sensor. The inverter also works well to synthesize a five-level PWM voltage waveform with sinusoidal load current.

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1. INTRODUCTION

Currently, the application of the power inverter is increasing in many areas such as in industrial application and in the renewable energy power conversion. The research and development of the power inverters is addressed to meet the need of the power inverter having some merits such as higher efficiency, smaller in size and better output quality of its output waveforms. In the renewable energy power conversion application especially in the photovoltaic system, the power inverter works converting the DC output power of the photovoltaic system into AC power to supply the load or to inject the power generated by the photovoltaic system into the power utility network, in case of the grid connected operation [1]. The development of the power converter technology is also supported by the fast development in power semiconductor technology such as power MOSFETs and IGBTs that making faster in switching characteristics of the switches and higher power capability.

The power inverters technology especially multilevel inverters both multilevel voltage source inverter (VSI) and multilevel current source inverters (CSI) give many advantages in the development of power inverter for the renewable energy conversion. They have capability to deliver higher power with lower gradient voltage (dv/dt) or lower gradient current (di/dt) and better output waveforms resulting in reduction

of Electromagnetic Interference (EMI) noise and reduce output filter size [2], [3]. The appellation of multilevel power inverter starts from the three-level inverter, four-level inverter, five-level inverter and so on. The higher the level number the closer to the sinusoidal waveform, hence the waveform distortion will be smaller. Several multilevel inverter configurations have been developed. The three different major multilevel inverter topologies have been reported in the literatures, i.e. cascaded H-bridges multilevel inverter, diode clamped multilevel inverter, and flying capacitors multilevel inverter [2]-[4]. The cascade H-bridge multilevel inverter has a merit related with its modular structure. However, the number of the isolated DC voltage sources and the power switches can be the lack of this inverter topology. The diode clamped multilevel inverter i.e. three-level inverter circuits has been widely used in industrial and traction drive. The requirement of many capacitors in the flying capacitor multilevel inverter leads complexity in the controller for balancing the capacitor's voltages of the inverter [5]. Some hybrid topologies of multilevel inverter have been proposed in order to eliminate some drawbacks of the three main inverter topologies previously discussed.

A configuration of multilevel inverter achieved using series-connected sub-multilevel converter blocks and H-bridge inverter was discussed in [6]. Reference [7] presented another multilevel inverter configuration constructed from the basic H-bridge inverter plus additional switches operating as bidirectional switches. Yet, the bidirectional power switches used in the configurations presented in [6] and [7] can be the drawback of the circuits. In practical manner there is no bidirectional switches available. Traditionally, the bidirectional power switches made from two IGBTs or a combination of a single IGBT and four power diodes will give more power losses of the inverter. Reference [8] presented another multilevel inverter circuits derived by connecting some two-level power cell circuits. The number of power switching devices and isolated DC power sources will cause the cost and circuit complexity increase [9]. Reference [10] discussed a hybrid multilevel inverter constructed using H-bridge topology and three-level cells. This topology needs eight power switches to establish a five-level inverter circuit.

This paper presents the circuit configuration of the five-level PWM voltage source inverter composed by the H-bridge inverter and DC power modules with a single DC input source. An auxiliary circuit was implemented to the circuits to keep stable DC capacitor voltage of the inverter and to reduce the capacitor size. The operating performance of the proposed capacitor balancing circuits is examined and tested through some computer simulations and experimentally. Furthermore, some experimental tests were carried using prototype of the inverter.

2. PROPOSED INVERTER CIRCUIT CONFIGURATION

2.1. Basic Operation of Inverter Circuits

The circuit configuration of the five-level inverter is obtained by connecting the H-bridge inverter with a single DC power module. Figure 1 shows the circuit configuration of the DC power module used in the inverter circuits, and its typical output waveform [5], [11]. Figure 2 shows the circuit configuration of the five-level inverter obtained using the proposed method. As can be seen from the figures, the DC voltage sources required in this inverter topology are connected in series. Consequently, it is possible to make use of non isolated DC voltage sources. Moreover, all of the power switches are a single IGBT, no bidirectional power switch required.

The single-phase five-level inverter circuits needs a single DC power module and an H-bridge voltage source inverter with only six power MOSFETs or IGBTs switches in total. If the DC input voltage sources of the five-level inverter are assumed the same as V/2, Table 1 presents the switching states of the proposed five-level inverter for five-level output voltage waveform generation, i.e. level +V, +V/2, 0, -V/2 and -V. To obtain these DC input voltage, there are two ways. The first method is by using two isolated DC voltage sources such as from batteries, and the second method is by applying a single DC voltage source equipped with auxiliary circuits to keep stable voltage of the DC capacitors as presented in this paper.

Figure 3 shows the configuration the proposed capacitor's voltage balancing circuits used in the proposed inverter. The circuits consist of a controlled switch, a diode, a reactor and two DC capacitors. Figure 4 presents the circuits of the single-phase five-level inverter equipped with voltage balancing circuits of the DC capacitors. A single DC input voltage source is connected to the inverter. In this circuits, the balancing circuits perform the voltage balance of the two DC capacitors C_1 and C_2. It works also to minimize the size of DC capacitors. Figure 5 shows the voltage control diagram of the balancing circuits in the five-level inverter. A simple proportional integral (PI) controller is applied. In this control system, the circuit employs a single controlled switch Qc, and a single voltage sensor only to govern the DC voltage across two capacitors, C1 and C2. It is a benefit of the balancing circuits in the proposed inverter. A single DC voltage sensor is connected across the capacitor C1 to sense the capacitor voltage to obtain voltage feedback V_{C1}.

If the DC voltage source amplitude is V, in case of the five-level inverter, the voltages across the DC capacitors are set at its half, V/2.

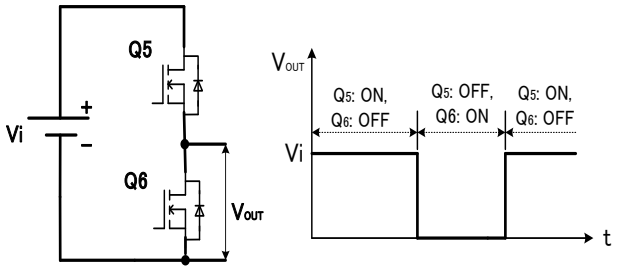


Figure 1. DC Power Module and Its Output Waveform [5], [11]

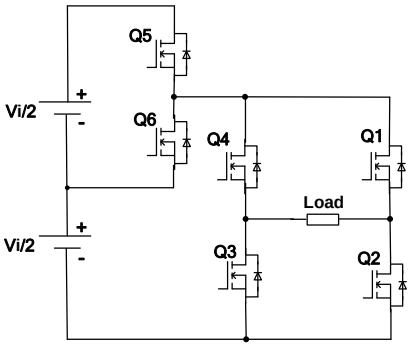


Figure 2. The Five-Level Inverter Circuits with Two DC Voltage Sources [5], [11]

Table 1. Switching States of Five-Level Inverter

Power Switches						Output Voltage (V)
Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	
0	1	0	1	1	0	+Vi
0	1	0	1	0	1	+Vi/2
0	1	1	0	0	0	0
1	0	1	0	0	1	-Vi/2
1	0	1	0	1	0	-Vi

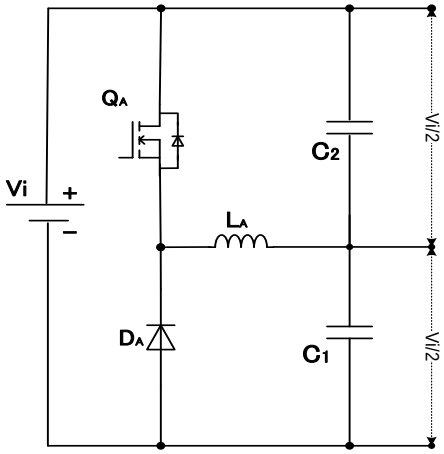


Figure 3. Proposed voltage balancing circuits [11]

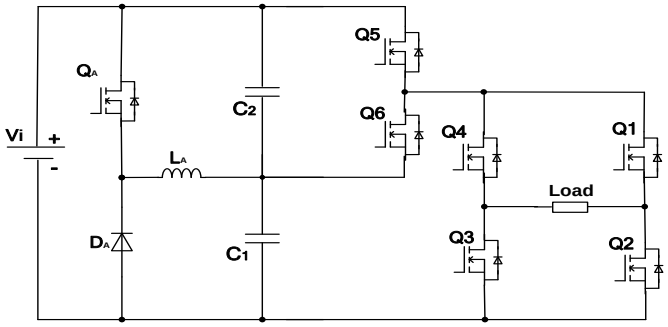


Figure 4. A five-level inverter with a single DC voltage source [11]

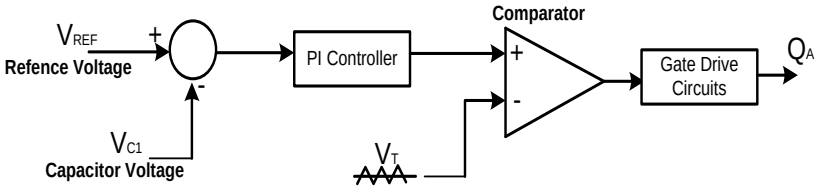


Figure 5. Control diagram of the voltage balancing circuits [11]

2.2. Pulse Width Modulation (PWM) Technique

In many commercial inverters, in order to obtain a sinusoidal output voltage or current waveform, a pulse width modulation (PWM) technique is employed together with low-pass filter. In this paper, triangular carrier based sinusoidal PWM technique is applied to evoke the gating signals of the inverter power switches to produce the five-level PWM voltage waveform. Two triangular waveforms with level shifted are used in this method as the carrier waveforms. The modulating signals utilize two sinusoidal waveforms with opposite phase. The frequency of the modulating signals (the reference sinusoidal waveforms) determines the fundamental frequency of the output voltage waveform, whereas the frequency of carrier waveforms sets the switching frequency of inverter's controlled switches [1], [5], [11], [12]. The PWM modulation technique used in the proposed inverter is shown in Figure 6.

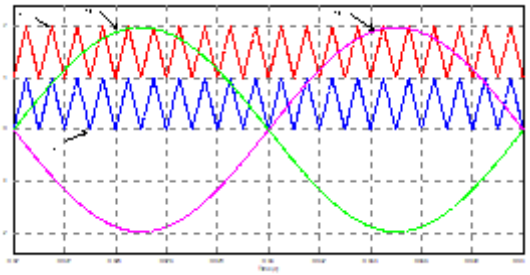


Figure 6. The carrier and modulating signal waveforms

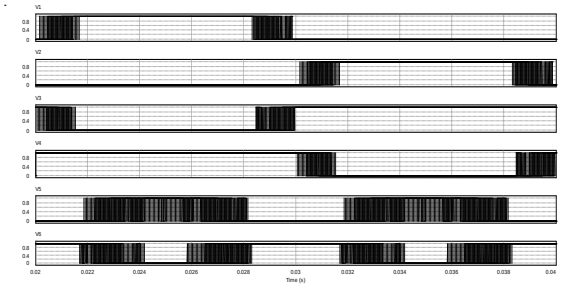


Figure 7. Gating signals of the inverter's power switches

3. COMPUTER SIMULATION RESULTS

Computer simulations are conducted by using a PSIM software in order to analyze and to test the proposed inverter and its balancing circuits. This section presents and discusses some computer simulation test results of the proposed five-level inverter circuits. The simulation test parameters are listed in Table 2. The proposed single-phase five-level inverter shown in Figure 4 is examined.

In the PSIM simulation circuits, the proposed five-level inverter circuit is connected with an inductive load, i.e. resistor R=20 Ω, inductor L=5 mH. The carrier frequency and the fundamental output voltage frequency are 22 kHz and 50 Hz, respectively. The inductor of balancing circuit Lc is 100-μH, and the DC capacitor size is 50-μF for both capacitors C_1 and C_2. The magnitude of the DC voltage source is

24 V. Figure 7 shows the computer simulation results of the PWM gating signals generated by the PWM strategy. These signal patterns are used as gating signals of the inverter. Figure 8 presents the voltage waveforms across the two DC capacitors C_1 and C_2. Stable voltage waveforms across DC capacitors (V_{C1} and V_{C2}) were obtained by the proposed balancing circuits, the magnitudes are about 12 V. Figure 9 shows the current waveforms flowing through the inductor (Lc), power switch (Qc) and diode (Dc) of the balancing circuits. Figure 10 shows the PWM output voltage waveform and load current waveform generated by the inverter. A proper five-level PWM voltage waveform was generated by the proposed inverter. Moreover, sinusoidal load current, ILoad, flows through the load.

Table 2. Computer simulation test parameters

Capacitors of balancing circuits, C_1 and C_2	50 μF
DC input voltage	24 V
Frequency of carrier signals	22 kHz
Reactor, Lc	100 μH
Power load	R = 20 Ω, L =5 mH
Fundamental output current frequency	50 Hz

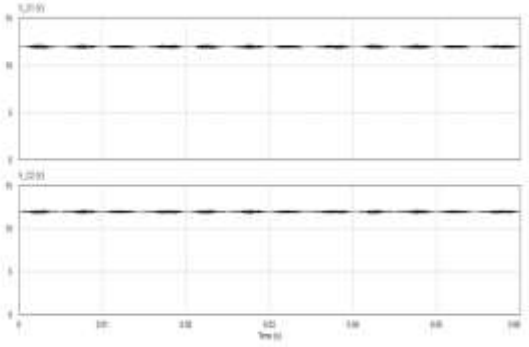


Figure 8. DC capacitor voltage waveforms of the inverter

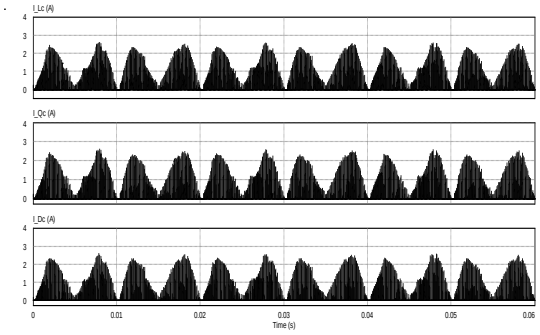


Figure 9. The current waveforms flowing through the inductor (Lc), power switch (Qc) and diode (Dc)

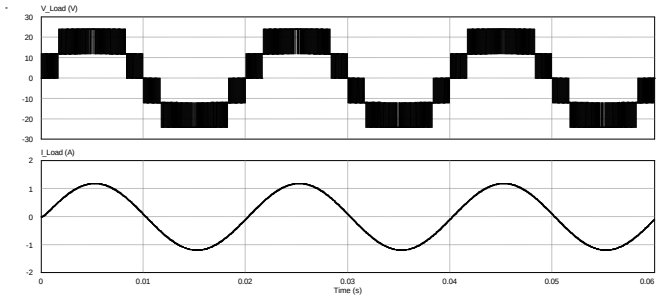


Figure 10. The PWM output voltage waveform and load current waveform

4. EXPERIMENTAL TEST RESULTS

In order to prove and to validate the proposed five-level inverter configuration experimentally, a laboratory prototype of the five-level inverter and its balancing circuits was constructed by using power MOSFETs. The experimental prototype specifications are alike with the computer simulation test parameters as listed in Table 2. A regulated DC power source is used as the DC input voltage source. Figure 11 shows the control circuits of the inverter and its balancing circuits used in the laboratory experimental test. Figure 12 and Figure 13 show the prototype of the voltage balancing circuits and the five-level inverter.



Figure 11. Control circuits of the inverter



Figure 12. The inverter's balancing circuits

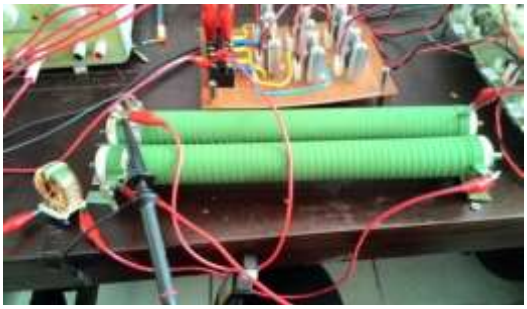


Figure 13 Inverter's power circuit and the power load

Figure 14, Figure 15 and Figure 16 show the measurement results of the gating signals used for the inverter's power switches, i.e. MOSFET Q1, MOSFET Q2, MOSFET Q3, MOSFET Q4, MOSFET Q5 and MOSFET Q6. The PWM frequency of these signals is 22 kHz, the same with the carrier signals. Figure 17 shows the dead-time value of gating signals between switches Q5 and Q6 set to be 4 µs. This deadtime was added to avoid short circuits condition between upper and lower switches of the inverter circuits. Figure 18 shows the experimental waveform of the DC capacitor voltage waveform of the five-level inverter obtained using the proposed voltage balancing ciruits. The capacitor voltage is kept at around 12 V, a half of the DC input power source 24 V. Furthermore, Figure 19 shows the output voltage waveform of the inverter presenting a five-level PWM voltage waveform and a sinusoidal load current. A proper five-level PWM output voltage waveform was succesfully obtained by using the laboratory prototype of the inverter topology.

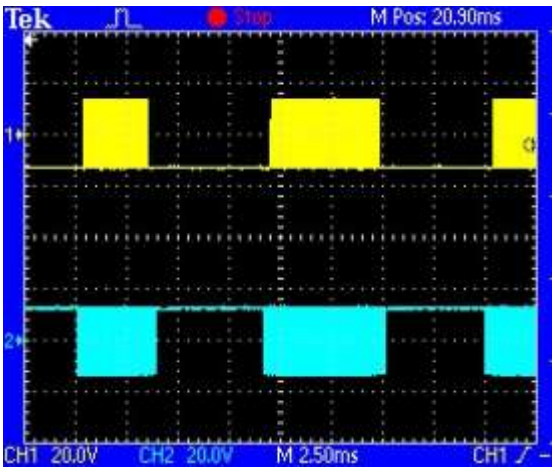


Figure 14. Gating signal of power switches Q5 and Q6

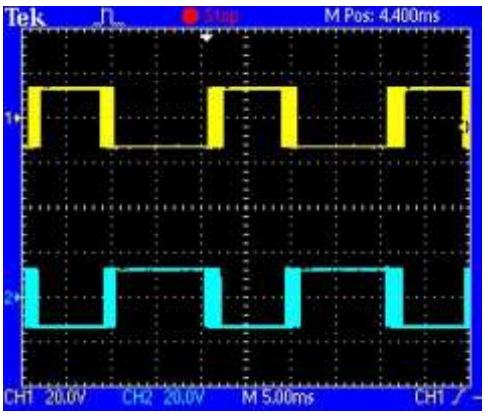


Figure 15. Gating signal of power switches Q1 and Q3

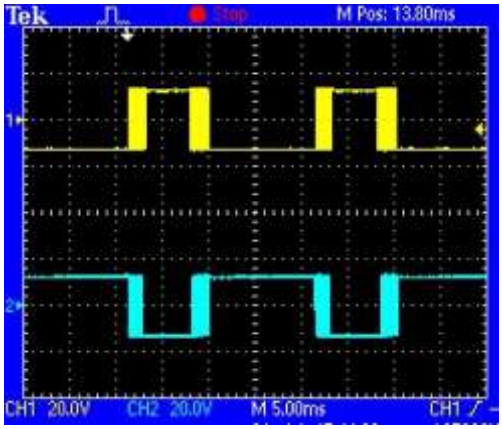


Figure 16. Gating signal of power switches Q2 and Q4

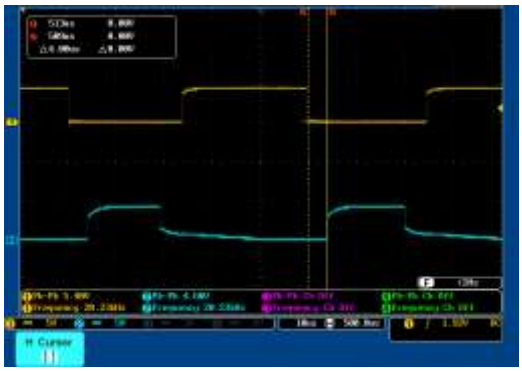


Figure 17. Deadtime of gating signals between switches Q5 and Q6

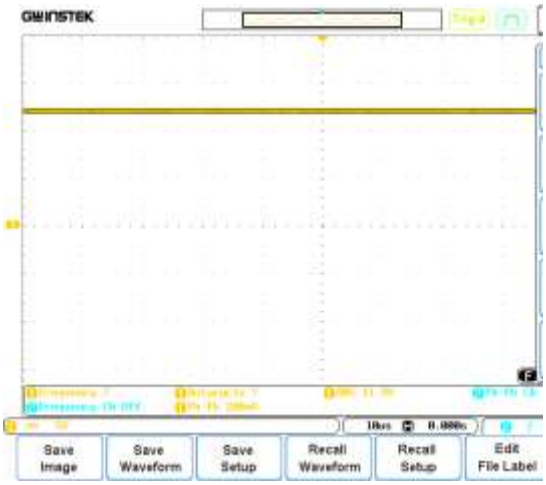


Figure 18. Experimental test result of DC capacitor's voltage

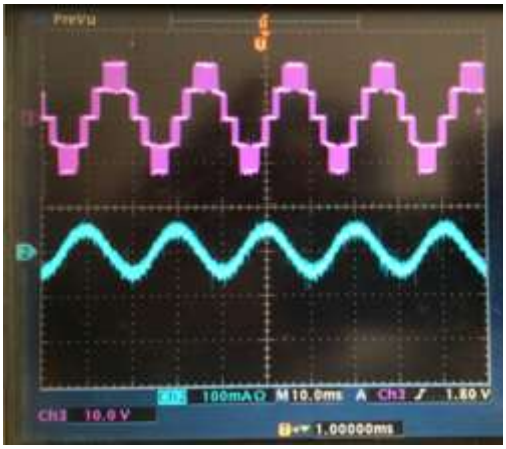


Figure 19. Five level PWM output voltage and load current waveforms

5. CONCLUSION

In this paper a five-level PWM inverter circuits with a single DC input voltage source has been presented and discussed. The five level inverter is equipped with a balancing circuits works keeping stable DC capacitor voltages of the inverter using only a single DC input power source. A single DC voltage sensor was used in the balancing circuits. The five-level inverter circuits is composed by a DC power modules and a H-bridge inverter for five-level voltage waveform generation with a single DC voltage source, and minimum number of power devices. Some computer simulations and experimental test results of the laboratory prototype have been presented to examine, and to validate the proposed balancing circuits and the five-level inverter circuits. The proposed balancing circuits worked well keeping stable DC voltages across the two DC capacitors of the inverter generating a five-level PWM output voltage waveform and a sinusoidal load current.

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