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Simulation and Analysis of Multiphase Boost Converter with Soft-Switching for Renewable Energy Application

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ABSTRACT

This paper presents the simulation design of dc/dc interleaved boost converter with zero-voltage switching (ZVS). By employin the interleaved structure, the input current stresses to switching devices were reduced and this signified to a switching conduction loss reduction. All the parameters had been calculated theoretically. The proposed converter circuit was simulated by using MATLAB/Simulink and PSpice software programmes. The converter circuit model, with specifications of output power of 200 W, input voltage range from 10~60 V, and operates at 100 kHz switching frequency was simulated to validate the designed parameters. The results showed that the main switches of the model converter circuit achieved ZVS conditions during the interleaving operation. Consequently, the switching losses in the main switching devices were reduced. Thus, the proposed converter circuit model offers advantages of input current stress and switching loss reductions. Hence, based on the designed parameters and results, the converter model can be extended for hardware implementation.

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1. INTRODUCTION

Dc/dc converters are essential equipment used in numerous electrical devices and appliances. In low voltage application, for instance, devices with renewable power like wind turbines, solar panel or fuel cell, the output voltage needs to be stepped-up to provide adequate amount of voltage output to the loads. In this case, dc/dc boost converter is commonly used as a converter to regulate the input voltage. It is also known as a step-up converter. Dc/dc converter consists of a simple structure formed by a few components, such as power switch, inductor, resistor, diode, and capacitor.

The outputs voltage can be regulated by varying the duty cycle of the Pulse Width Modulation (PWM) switching signal. The ripple outputs voltage and current are proportionally related to the switching frequencies. High switching frequency can reduce the ripple voltage and current. However, high-frequency operation often results in increased switching losses, higher electro-magnetic interference (EMI), and lower converter efficiency [1]. Therefore, many researchers use the interleaving method, which uses two or N number dc/dc converters combined together to reduce the ripple voltage and current, as depicted in [2-4]. Besides, the inductors current is reduced; whereby the total current through the circuit is based on N number of boost converter in the circuit. The interleaving method, in fact, is widely used in high power application, especially in renewable energy applications, such as photovoltaic system [3], [5], fuel cell [6], [7], and lighting systems [8], [9], as well as hybrid electric vehicle (HEV)[10].

Power losses are caused by resistance, components, passive elements, and switching losses across the semiconductor devices. These affect the efficiency, which is an important figure of merit, and have significant implications on the overall performance of the system [11]. The losses in the converters should be as low as possible to achieve high efficiency output. Besides, switching losses increase proportional to the increasing switching frequency of the converter. Converters that are operated in high switching frequency usually produce low output voltage ripple, while reducing the size and the weight of the converter. At present, most PWM converters are operated under hard switching conditions. The turn on and off of the rectangular waveform of voltage and current often change abruptly; causing switching losses, switching stresses, and producing EMI [12]. The use of an auxiliary circuit called the snubber can reduce switching losses, but not necessarily the overall losses of the converter [13].

As such, an effective technique to reduce switching losses is by adding an additional branch across the power switches, which is known as soft-switching technique. The technique can be divided into two; zero-voltage switching and zero-current switching. Soft-switching converter has gained interest among researchers to reduce switching losses in dc/dc boost converters [14-17]. Dc/dc converters with interleaved operation are fascinating techniques nowadays, since they can reduce the ripple output voltage and input current. An auxiliary circuit is placed between the switches so that the current or the voltage can be shaped in such a way that the switch can turn on and off at zero-current or voltage [14]. In zero-voltage switching, resonant capacitor is placed in series with the power switches so that it can delay the rise of voltage across the switches; thus turning it off softly with ZVS.

This paper presents the study on the multiphase/interleaved boost converter with zero-voltage switching. The proposed converter is suitable for systems with a wide fluctuating DC input voltage range, specifically in renewable energy application. A 200 W model of the converter had been simulated by using MATLAB/Simulink and PSpice software. The simulation results had been analyzed to verify the effectiveness of the proposed converter to operate with a wide range of input and load variations. Furthermore, the effect of ZVS circuit was compared with that of the conventional circuit in terms of input ripple current and output ripple voltage, as presented in the following sections.

2. PROPOSED TOPOLOGY

Figure 1 shows the circuit of the ZVS interleaved dc/dc boost converter. This circuit consists of two boost converters. The main circuit comprises of inductors (L_1 and L_2), capacitor (C_{out}), power switches (S_1 and S_2), and diodes (D_1 and D_2). Meanwhile, the auxiliary circuits consist of resonant inductors (L_{r1} and L_{r2}) and resonant capacitors (C_{r1} and C_{r2}). The resonant inductors and capacitors are placed in series and parallel with the power switches. The power switches S_1 and S_2 turn on process takes place under ZVS within a short period of time, whereas the converter operates in the same way as the conventional PWM converter most of the time.

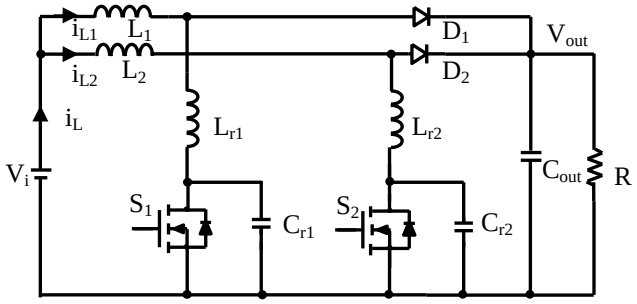


Figure 1. The interleaved dc/dc boost converter with ZVS

On the other hand, as for the interleaving method, the current through the inductors L_1 and L_2 will be reduced by two, which will then affect the reduction of the size of the inductor. The input current i_L of the proposed converter can be analyzed based on the phase current. Besides, the ripple voltage and the current ripple should be significantly lower compared to the conventional single phase dc/dc converter. Moreover, with zero-voltage switching method, the proposed converter shall reduce the switching losses and increase the overall efficiency. In terms of the electrical performance advantages, it has been also revealed that, the

size of the inductor can be smaller and lighter for interleaved boost converter compared to conventional converter topologies.

3. DESIGN PROCEDURE OF THE PROPOSED CONVERTER

3.1. Selection of the Main Inductor Values

In the interleaved converter, two output phases were alternately driven at 180 degrees out of phase. The conduction (I^2R) losses were lowered by splitting the current into two power paths. The proposed converter was principally operated and analyzed in Continuous Conduction Mode (CCM). Therefore, both inductor currents i_{L1} and i_{L2} were always positive. The maximum inductor currents for both phases were set to 5A maximum. The duty cycle was set to be less or equal to 0.5 in order to reduce the current through inductors L_{r1} and L_{r2} by increasing the input voltage V_i and by decreasing the load R.

All parameters for the main circuit were derived by using the volt-second balance theory as in [18]. The maximum and the minimum inductor currents were determined by using the average value and the change in current from Equation (1)

$$I_{max,min} = i_L \pm \frac{\Delta i_L}{2} = \frac{V_i}{(1-D)^2 R} \pm \frac{V_i DT}{2L} \quad (1)$$

Figure 2 shows the graph of the maximum inductor current with the change of duty cycle derived from Equation (1). The values of L_1 and L_2 were set to 220 µH and the load was varied from 20 Ω to 100 Ω. Higher values of inductance had been preferred to gain lesser ripple in the output. The maximum inductor current, i_{Lmax} from R=20 Ω and d=0.5 was 13.92 A. In N interleaved boost converter, the inductor current was reduced by N number of interleaved path. On the other hand, by increasing the interleaved path, the inductor current would also be reduced.

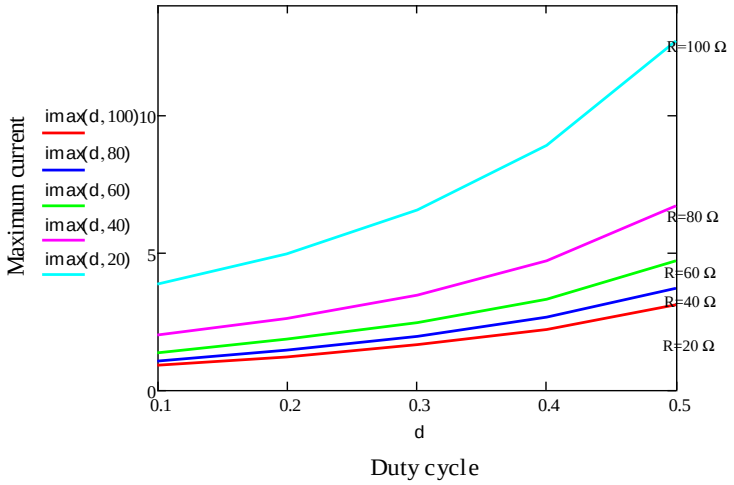


Figure 2. The variation of inductor current i_L versus duty cycle (L=220uH) for single phase boost converter

3.2. Selection of Resonant Inductors and Capacitors

According to the ZVS principle, when the main switches were turned off, C_{r1} and C_{r2} would be used to reduce the turn-off loss. The larger values of C_{r1} and C_{r2} resulted in lower turn-off loss. However, the larger values of C_{r1} and C_{r2} caused more energy to be stored. The energy stored in C_{r1} and C_{r2} was then transferred to L_{r1} and L_{r2} alternatively through resonance. It further affected the peak value of current and conduction losses of the switches. Therefore, there was a trade-off when the values of resonant inductor and capacitor were determined.

For auxiliary circuit, the values of resonant capacitor and inductor were calculated by using Equations (2) and (3), as presented in [12], whereby Q is the quality factor.

$$L_r = \frac{\Delta R_L}{\omega_o Q} \tag{2}$$

while the resonant capacitance was obtained via,

$$C_r = \frac{Q}{\omega_o \cdot \Delta R_L} \tag{3}$$

and dc transfer function was

$$M = \frac{V_o}{V_{in}} \tag{4}$$

since,

$$M = \frac{1.1}{f_s / f_o} \tag{5}$$

The design proposed in this paper was based on boost half wave ZVS converter. Equation (6) was then used to determine the values of Q and A, with n=1, adapted from those proposed in [3] and [4] by Kazimierczuk. The graphs in Figure 3 and Figure 4 were plotted using MathCAD software program based on the values determined by using Equation (6).

$$A = \frac{2\pi}{M\left\{\pi + \frac{Q}{2M} - \arccos\sqrt{1-\left(\frac{Q}{M}\right)^2} + \frac{M}{Q}\left[1-\sqrt{1-\left(\frac{Q}{M}\right)^2}\right]\right\}} \tag{6}$$

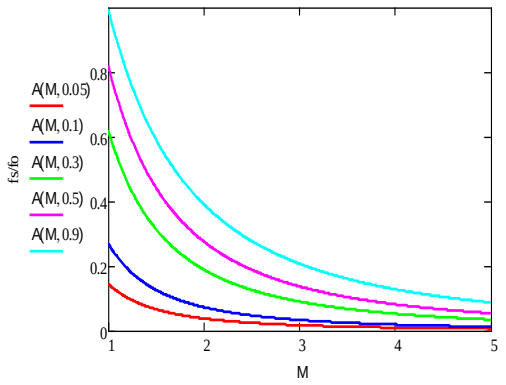


Figure 3. Normalized frequency versus voltage gain; n=1 and h≤0

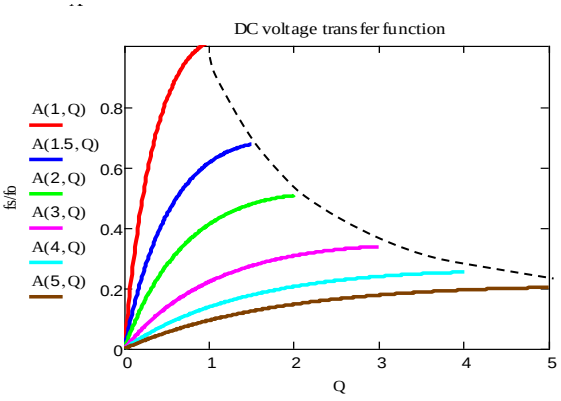


Figure 4. Normalized Frequency Versus Quality Factor; N=1 and h≤0

For Q=M, the maximum and minimum values of resonant inductor had been calculated. The values for $L_{r1,2}$ and $C_{r1,2}$ were purposelychosen to be small for calculation so that the converter could operate in various ranges of input voltage and loads. All the parameters of the components were calculated to identify the suitable values used in simulation. Nonetheless, the main inductance ($L_1$and L_2) and the capacitance (C_1 and C_2) had been very large (L_1 and L_2>> L_r, C_1 and C_2>> C_r). The ZVS interleaved dc/dc converter specifications and components parameters are presented in Table 1.

Table 1. Design specifications of the proposed ZVS interleaved dc/dc converter.

Symbol	Speed (rpm)
V_i	10V-100V
L_1 and L_2	220µH
C_1	470µF
L_{r1} and L_{r2}	10µF
C_{r1} and C_{r2}	56nF
f_s	100kHz
P_{out}	200W

4. CIRCUIT SIMULATION

4.1. Controller Design

The proposed circuit controller was realized by using Proportional Integral (PI) controller, which was suitable for step references. The transient responses must be controlled by proper selection of the controller parameters. The values of K_P and K_I were adjusted to a few values by trial-and-error to achieve optimal performance. The output voltage had been compared with reference voltage and was fed to the PI controller. There were two saw-tooth signals, which then were equated with the outputs from the PI controller to produce the PWM signals. However, the PWM switching signal generated differed by 180 degrees from each other.

4.2. Converter Characteristics

Other than that, the PSpice software program had been employed to analyze the operational characteristics of the proposed ZVS interleaved boost converter. PSpice allowed for a precise study and evaluation of electrical systems, thus optimizing the overall behavior of the power converter [19]. The components, such as the power switches, had been made available in the PSpice manufacture library whereby, every part listed had a corresponding PSpice model. The PWM switching signal was set at 100 kHz. t_r and t_f indicated the rise time and the fall time of the driver's circuit were set to 160 ns and 140 ns, respectively. All the parameters determined from the calculation matched the exact values available in the market.

5. RESULTS AND ANALYSIS

5.1. Simulation Results

The performance in different operating aspects had been evaluated by using PSpice software. Different operating modes in the simulation had been provided by changing the input voltage and load. Figure 5 shows the simulation results of the interleaved dc/dc converter with hard switching, while Figure 6 shows the soft-switching technique with 0.5 duty cycle. Figure 5(a) and Figure 5(b) shows the losses during turning on and off at switching transition phase of S_1 and S_2. As exhibited in Figure 6(c) and Figure 6(d), both switches S_1 and S_2 turned on at zero-voltage switching. The power losess (V_{ds} x I_{ds}) across switches S_1 and S_2 are shown in Figure 6(a) and Figure (b), respectively. During this condition, the measured voltage losses across single switch for hard switching and soft switching are 5.517 Watt and 2.348 Watt, respectively. It shows that, by using zero voltage switching technique, the losses across the switch had been reduced by 59.44 pecent.

Next, Figure 7 shows the simulation results for duty cycle 0.5 with 30V input voltage. It illustrates the ripple output voltage, inductor current (i_L), inductors current through L_1 and L_2, and switching signal for S_1 and S_2. The measured average inductor current in Figure 7(b) was 9.94 A. The main inductor current increased and decreased linearly by varying to the duty cycle. Additionally, the effective ripple frequency had been doubled as both the phases were generated together at the output capacitor, which caused an effortless reduction in ripple voltage, as demonstrated in Figure 7(a).

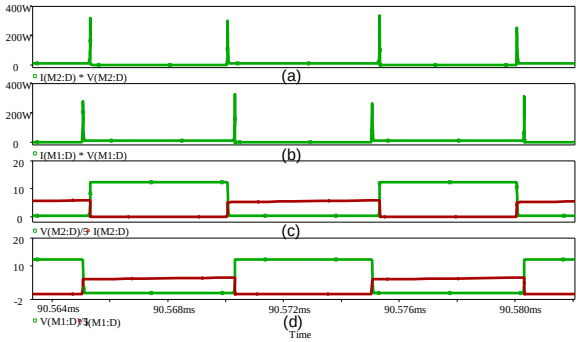


Figure 5. Interleaved dc/dc converter with hard switching at duty cycle 0.5, (a) power loss across S_1, (b) power loss across S_2 (c) V_{ds} and I_{ds} across S_1 and (d) S_2

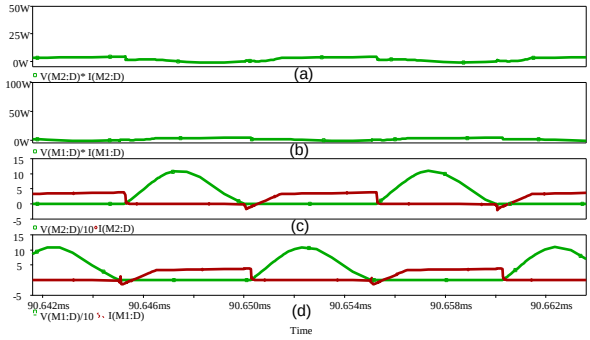


Figure 6. Simulation results for interleaved dc/dc converter with zero-voltage switching at duty cycle 0.5, (a) power loss across S_1, (b) power loss across S_2, and (c) V_{ds} and I_{ds} across switch S_1 and (d) S_2

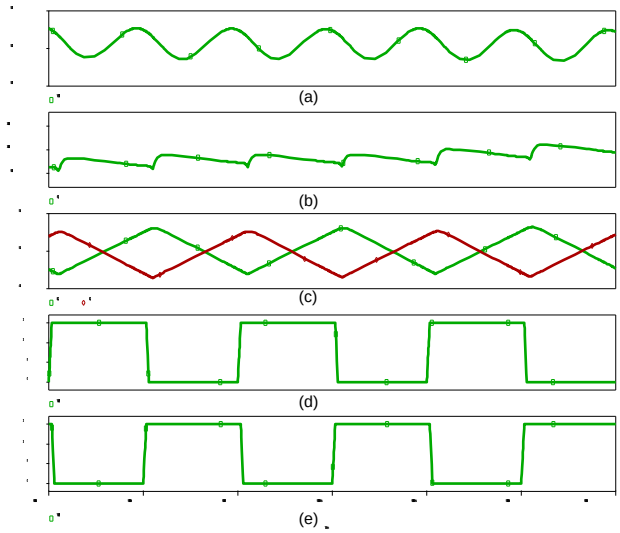
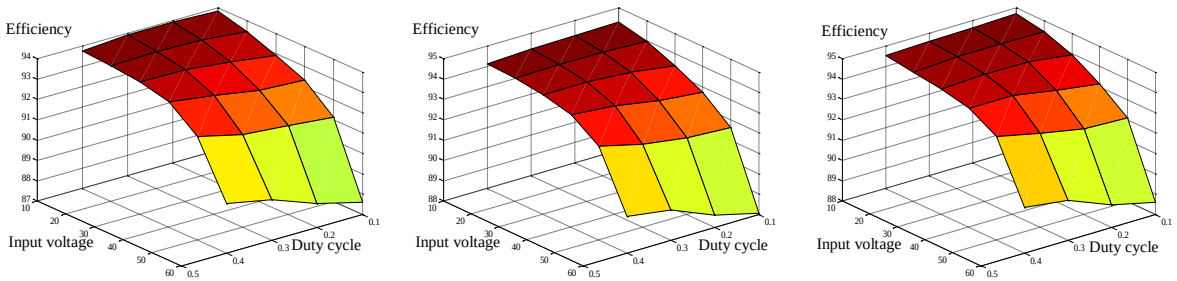


Figure 7. Simulation results for ZVS interleaved dc/dc converter with soft-switching at duty cycle 0.5, (a) ripple output voltage, (b) i_L, (c) i_{L1} and i_{L2}, (d) V_{gs1} and (e) V_{gs2}

5.2. Converter Efficiency

Figure 8 shows the converter efficiencies tested using various output loads by varying the input voltage and duty cycle. The output load was varied from 30 Ω to 100 Ω; assuming there might be some variations in the load which could affect uncertainty in the operating point. Meanwhile, the duty cycles were varied from 0.2 to 0.5 for both S_1 and S_2 in the interleaving method. Hence, the results showed that the efficiency increased linearly with the increasing output power. The highest efficiency of the converter was at 96.87% at 200 W output load, as shown in Figure 8(h). During the simulations, some operational performances, such as inductor current and voltage drain-source, had been analyzed to meet the suitable components for hardware implementation.



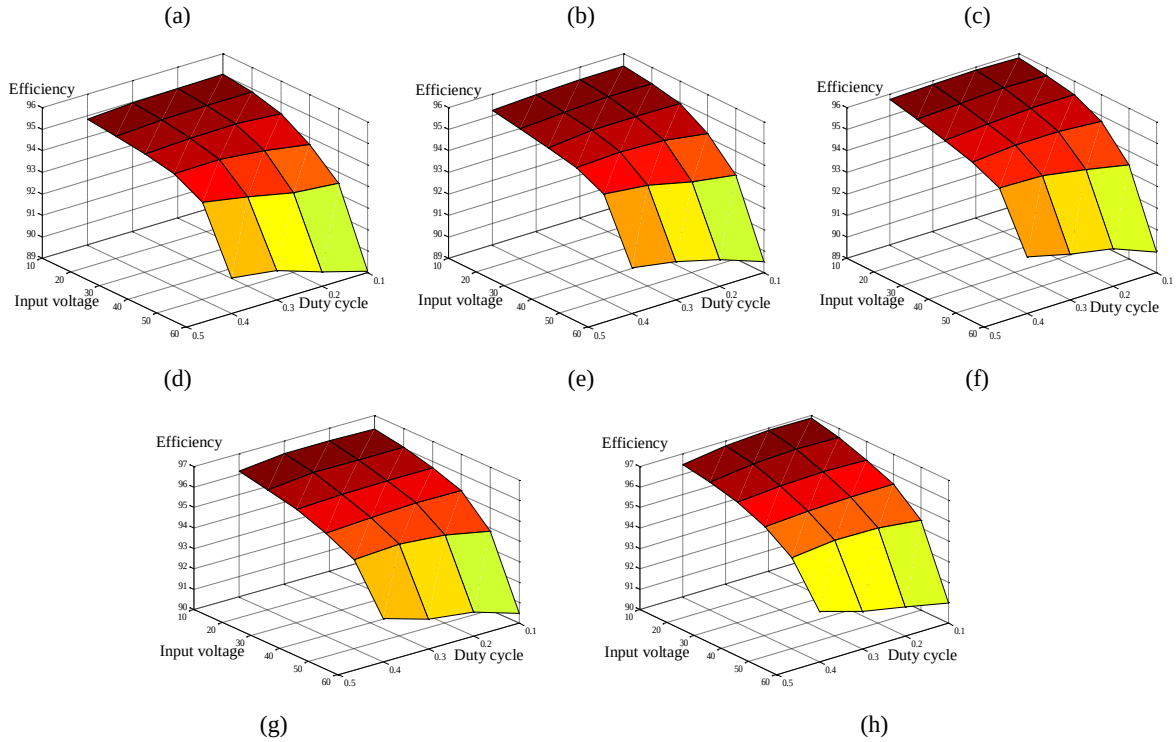


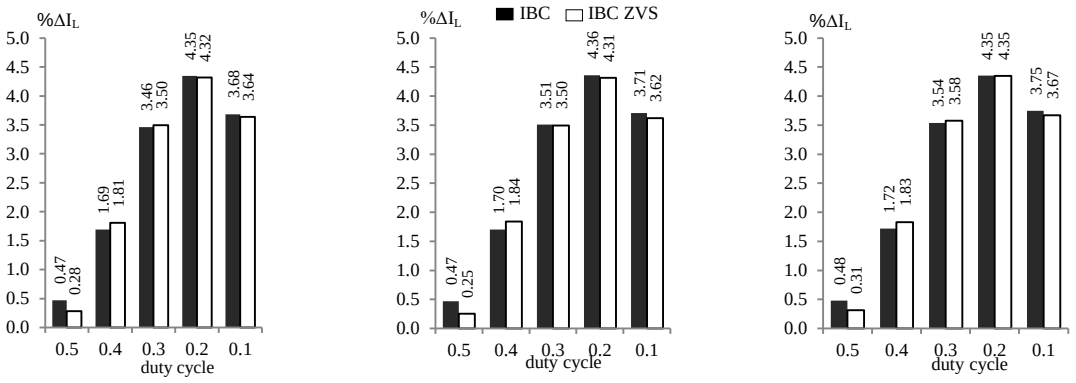
Figure 8. Results of simulations with constant load test (a) R=100 Ω, (b) R=90 Ω, (c) R=80 Ω, (d) R=70 Ω, (e) R=60 Ω, (f) R=50 Ω, (g) R=40 Ω, and (h) R=30 Ω

5.3. Analysis of the Input Current Ripple and Output Voltage Ripple of the IBC ZVS

Consequently, this analysis was done to evaluate if the interleaved boost converter had been capable for a condition associated to ZVS for the switches without increasing their input current stresses and output voltage ripple. The simulation results for IBC and IBC ZVS from PSpice software program had been analyzed in detail. In this situation, the circuit simulation was simulated for 50 m seconds and waveform began saving the data after 40 m seconds. The inductors current (i_L) for different duty cycles had also been analyzed, assuming that the ripple inductor current was constant through the simulation. Theoretically, for single phase converter, the inductor current ripple should be at maximum value at duty cycle 0.5. Nevertheless, the input current ripple was at zero for two-stage converter, while assuming all the components were in ideal state.

Figure 9 shows the simulation results in percentage of ripple for inductor current for interleaved boost and IBC ZVS. The percentages of input current ripple for both conditions had been plotted into three different output voltages. The percentages of inductor current ripples for duty cycle 0.5 were below 1% for both conditions. The inductor current ripple, nonetheless, decreased linearly with the decreasing duty cycle. Figure 10 shows the average percentage of ripple current from Figure 9(a), Figure 6(b), and Figure 6(c). There was no additional voltage and current stress across or through the semiconductor devices in comparison to the hard-switching converter counter-part, which reduced the conduction losses of the converter.

Table 2 shows the percentage of output voltage ripple for the proposed converter. Table 2 shows the ripple output voltage for conventional interleaved converter and proposed converter produce almost the same output sequence. The highest output ripple voltage was at 48 V, whose value was 0.9%. It also shows that the output ripple voltage increased with the increase of output voltage. All semiconductor devices in the proposed converter were not subjected to any additional voltage and current stress. The two primary sides, however, had been parallel to handle the large input current and to minimize the input current ripple.



(a) (b) (c)

Figure 9. Percentage difference for ripple current i_L of IBC and IBS ZVS associated with V_{out} at (a) 48V, (b) 36V, and (c) 24V

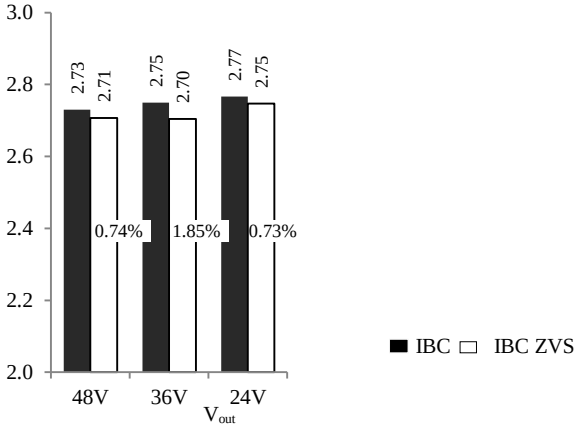


Figure 10. Average percentage differences for IBC and IBS ZVS.

Table 2. Simulation results for output voltage ripple for IBC and IBC ZVS.

		Percentage Output Voltage Ripple					
		48-V		36-V		24-V	
		IBC	IBC ZVS	IBC	IBC ZVS	IBC	IBC ZVS
Duty cycle	0.5	0.6	0.7	0.4	0.5	0.3	0.3
	0.4	0.9	0.9	0.6	0.6	0.4	0.4
	0.3	0.8	0.8	0.6	0.7	0.4	0.4
	0.2	0.6	0.6	0.4	0.4	0.2	0.3
	0.1	0.3	0.3	0.2	0.3	0.1	0.2

6. CONCLUSION

A simulation on ZVS for interleaved dc/dc converter has been presented in this paper; although it requires additional auxiliary resonant circuits and devices with control complexity, which had increased the cost of the converter, decreased its reliability, and generated extra losses that eventually adversely influences the efficiency of the converter. Nevertheless, the switching losses during turn off of the switches have been greatly reduced. This study has also shown that the input ripple current and the output ripple voltage will not be affected by the presence of auxiliary circuit. However, switching losses during turn off of the switches still exist. These have been eliminated by employing the zero-current switching technique (ZCS). All the parameters, which are based on the design, can be clearly identified for hardware implementation.

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REFERENCES

[1] N. Altintas, A. F. Bakan, and I. Aksoy, "A Novel ZVT-ZCT-PWM Boost Converter," *IEEE Trans. POWER Electron.*, vol. 29, no. 1, pp. 256–265, 2014.
[2] M. Rezvanyvardom, E. Adib, and H. Farzanehfard, "New Interleaved Zero-Current Switching Pulse-Width Modulation Boost Converter with One Auxiliary Switch," *IET Power Electron.*, vol. 4, no. 9, p. 979, 2011.
[3] D. Jung, Y. Ji, S. Park, Y. Jung, C. Won, and S. Member, "Interleaved Soft-Switching Boost Converter for Photovoltaic Power-Generation System," *IEEE Trans. POWER Electron.*, vol. 26, no. 4, pp. 1137–1145, 2011.
[4] J. Wen, T. Jin, and K. Smedley, *"A New Interleaved Isolated Boost Converter for High Power Applications,"* Twenty-First Annu. IEEE Appl. Power Electron. Conf. Expo. 2006. APEC '06., pp. 79–84, 2006.
[5] C. Tang, Y. Chen, Y. Chen, Y. Chen, and Y. Chang, "Multi-Mode Interleaved Boost Converter for Photovoltaic Power Systems with Low-Voltage Ride-Through Capability," 2013, pp. 1096–1101.
[6] V. Samavatian and A. Radan, "A novel low-ripple interleaved buck–boost converter with high efficiency and low oscillation for fuel-cell applications," in *International Journal of Electrical Power & Energy Systems*, 2014, vol. 63, pp. 446–454.
[7] G. C. H. Kang and B. L. W. Lee, *"Design Consideration of Interleaved Converters for Fuel Cell Applications,"* in International Conference on Electrical Machines and Systems, 2007, pp. 238–243.
[8] C. Zheng, S. Member, W. Yu, J. J. Lai, and H. Ma, *"Single-Switch Three-Level Boost Converter for PWM Dimming LED Lighting,"* in Energy Conversion Congress and Exposition (ECCE), 2011, pp. 2589–2596.
[9] S.H.Hosseini, S. K. Haghighian, S. Danyali, and H. Aghazadeh, *"Multi-Input DC Boost Converter Supplied by a Hybrid PV / Wind Turbine Power Systems for Street Lighting Application Connected to the Grid,"* in Universities Power Engineering Conference (UPEC), 2012, pp. 1–6.
[10] F. Khoucha, A. Benrabah, O. Herizi, A. Kheloui, F. Khoucha, A. Benrabah, O. Herizi, and A. Kheloui, "An Improved MPPT Interleaved Boost Converter for Solar Electric Vehicle Application," in *IEEE POWERENG 2013*, 2014.
[11] Muhammad H. Rashid, *Power Electronics Handbook*, 3rd ed. Elsevier, 2011.
[12] A. B. Afarulrazi, M. U. Wahyu, T. Taufik, S. Aizam, and Jumadril, "Design Study of Zero Voltage Switching for DC/DC Boost Converter," *Appl. Mech. Mater.*, vol. 785, pp. 136–140, 2015.
[13] Taufik, P. Luther, and M. Anwari, *"Digitally Controlled ZVS Quasi-Resonant Boost Converter with M-type Switch,"* in International Conference on Intelligent and Advanced Systems, 2007, pp. 823–828.
[14] M. K. Kazimierczuk, "Design-Oriented Analysis of Boost Zero-Voltage- Switching Resonant DC / DC Converter," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 126–136, 1988.
[15] S. S. Park, J. Yu, Y. Jung, C. Won, and S. Member, "Analysis and Design of a Soft-Switching Boost Converter With an HI-Bridge Auxiliary Resonant Circuit," *IEEE Trans. POWER Electron.*, vol. 25, no. 8, pp. 2142–2149, 2010.
[16] Y. Hsieh, T. Hsueh, and H. Yen, "An Interleaved Boost Converter With Zero-Voltage Transition," *IEEE Trans. POWER Electron.*, vol. 24, no. 4, pp. 973–978, 2009.
[17] R. C. N. Pilawa-podgurski, S. Member, A. D. Sagneri, J. M. Rivas, D. I. Anderson, D. J. Perreault, and S. Member, "Very-High-Frequency Resonant Boost Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1654–1665, 2009.
[18] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics Converters, Applications, and Design*, 3rd ed., vol. 4. John Wiley & Sons, Inc., 2007.
[19] C. Buccella, C. Cecati, and H. Latafat, "Digital Control of Power Converters—A Survey," *IEEE Trans. Ind. INFORMATICS*, vol. 8, no. 3, pp. 437–447, 2012.