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A Study on 3-phase Interleaved DC-DC Boost Converter Structure and Operation for Input Current Stress Reduction

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ABSTRACT

This paper analyses a 3-phase interleaved DC-DC boost converter for the conversion of low input voltage with high input current to higher DC output voltage. The operation of the 3-phase interleaved DC-DC boost converter with multi-parallel of boost converters is controlled by interleaved of switching signals with 120 degrees phase-shifted. Therefore, with this circuit configuraion, high input current is evenly shared among the parallel units and consequently the current stress is reduced on the circuit and semiconductor devices and contributes reduction of overall losses. The simulation and hardware results show that the current stress and the semiconductor conduction losses were reduced approximately 33% and 32%, respectively in the 3-phase interleaved DC-DC boost converter compared to the conventional DC-DC boost converters. Furthermore, the use of interleaving technique with continuous conduction mode on DC-DC boost converters is reducing input current and output voltage ripples to increase reliability and efficiency of boost converters.

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1. INTRODUCTION

In recent years, renewable energy (RE) i.e., photovoltaic and wind become an increasingly important source of energies. Sustainable power sources are the better alternatives contrasted with non-sustainable power sources since the RE sources do not pollute surrounding environment. However, the voltage levels obtained from those energy sources are typically low and unregulated. Besides that, low input voltage from the RE sources will produce high current which needs to be managed by power converter [1-4]. Hence, a suitable power converter is required to increase and regulate output voltage level with high input current [5], [6]. Existing conventional DC-DC boost converter is widely used for boosting very low input voltage to very high output voltage level for supplying loads [7-11].

However, the conventional DC-DC boost converter not able to manage high input current if the input voltage is very low. In addition, high input current at low voltage side causes increasing of current stress and semiconductor devices losses in the converter. Therefore, interleaving technique is one of the attractive option to solve decrease the current stress at low voltage side [7], [10], [12]. This is because, the input current is evenly shared according to number of phases considered, thus consequently it reduces input current stress and semiconductor losses. Interleaving or generally is a variation technique of paralleling technique of multiple switching cells where the switching instants are phase-shifted with a switching period. The implementation of interleaved DC-DC boost converter has several advantages such as reducing current stress, reducing input current and reducing output voltage ripple [7], [13].

This paper focuses on 3-phase interleaved DC-DC boost converter design consideration to reduce high current stress at low voltage side. In addition, semiconductor switching devices losses reduction is also discussed. Two converters, i.e., conventional and 3-phase interleaved DC-DC boost converters are considered for a comparison. First, principles of 3-phase interleaved DC-DC boost converters are described. Then, the converter design principle in terms of parameter selection is discussed for both converters. The current stress and semiconductor conduction losses are also described. Simulation and experimental results of the conventional and 3-phase interleaved DC-DC converters are analyzed and discussed.

2. PRINCIPLE OF CONVERTER DESIGN

Table 1 shows the important expressions for the converter design parameters estimation. Meanwhile, Table 2 shows the initial specifications of the converter parameters. The minimum inductor value must be calculated because it will determine which mode the boost converter will operate whether in continuous current mode (CCM) or discontinuous conduction mode (DCM). All the parameters that been calculated are used in the conventional DC-DC boost converter and 3-phase interleaved boost converter for simulation and hardware implementation purposes.

Table 1. Parameters and Expression

Parameter	Expression	
Output voltage, V_{out} (V)	$V_{out} = \frac{1}{1-D} V_{in}$	(1)
Boost ratio, β	$\beta = \frac{1}{1-D} = \frac{V_{out}}{V_{in}}$	(2)
Inductance, L_{min}, (H)	$L_{\min} = \frac{D(1-D)^2 R}{2f}$	(3)
Capacitance, C_{min} (F)	$C_{\min} = \frac{D}{rRf}$	(4)

Table 2. Initial Parameters

Parameter	Value
Input Voltage, V_{in} (V)	25
Output Voltage, V_{out} (V)	50
Switching Frequency, f (kHz)	25
Ripple factor, r (%)	1
Power, P (W)	25

3. PRINCIPLE OF 3-PHASE INTERLEAVED DC-DC BOOST CONVERTER OPERATION

Figure 1 shows the 3-phase interleaved DC-DC boost converter circuit. The proposed configuration circuit consists of three similar boost inductors, L_1, L_2, and L_3, power switches, S1, S2 and S3, and power diodes D1, D2, and D3. Each phase of the converter is linked with an output capacitor filter C, and a load, R. Each phase is switched with same duty ratio D, but each phase is phase-shifted by 360°/n which n is the number of phases. In this configuration, the phase shift is 120° between each phase. The interleaved circuit is formed by three independent boost switching units. Fundamentally, each phase of the converter will operate in the same manner as the conventional boost converter. The continuous conduction mode (CCM) is selected because of its advantages than the discontinuous conduction mode (DCM) and it is suitable for the interleaved boost converter operation.

For this interleaved boost converter, there are five modes of operations. The first mode is when S1, S2, and S3 closed, the second mode is S1 closed, S2 and S3 opened, the third mode is S2 closed, S1 and S3 opened, fourth mode S3 closed, S1 and S2 opened and lastly S1, S2, and S3 opened. During the time opened (t_{open}), the change of time is (1-D)T while during the time closed (t_{closed}), the change of time is DT. Figure 2 shows the timing diagram of the switching signals with 120° phase-shifted between signals.

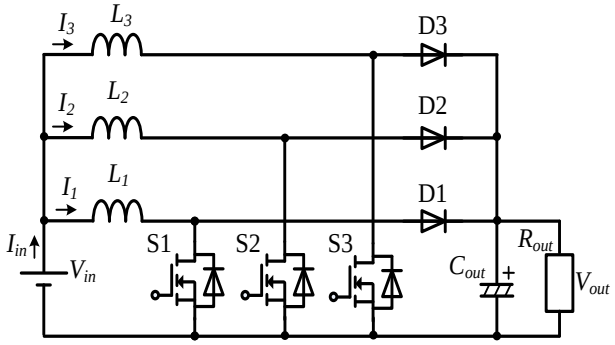

Figure 1. 3-phase interleaved DC-DC boost converter

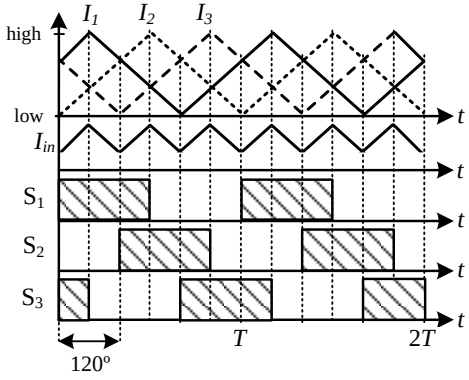

Figure 2. Phase currents (inductor curents), input current and MOSFETs gate signal waveforms

3.1. Current Stress Reduction

The designed 3-phase interleaved DC-DC boost converter circuit configuration has special features of current stress reduction at the input side and voltage ripple reduction at the output side. The current stress reduction feature is benifited to manage high input current at low input voltage. The input current I_{in} in the interleaved converter is the sum of the current flowing through all inductors. Then, the high input current from low input voltage can be shared among the three parallel phases. Therefore, lower current rating of the converter components can be considered. Besides, the average of the inductor currents I_1, I_2 and I_3 are evenly distributed with the phase shift of 120º because the power switches S1, S2 and S3 operates in interleaved manner with same duty cycle, *D*. As a result, the input current and output voltage ripple will be lower due to ripple cancellation. Figure 2 show the timing diagram of switching signals.

3.2. Semiconductor Conduction Los Reduction

Pincipally, high current stress will give bad results on the semiconductor devices in boost converter circuit. The conduction loss of the MOSFET is expressed as follows:

$$P_{cond} = I_{DS}^{\ 2} \times R_{DS(ON)} \times DT \quad (5)$$

where P_{cond} is the conduction loss, I_{DS} is the conduction current and R_{DS} is the ON-resistances of the MOSFET. Meanwhile *D* is the duty cycle and *T* is the one-cycle period. Thus the conduction loss in each semiconductor device is reduced when interleaving switching technique is used.

4. SIMULATION AND EXPERIMENTAL RESULTS

Table 3 shows the simulation and experimental specifications for conventional DC-DC boost converter and 3-phase interleaved DC-DC boost converter.

Table 3. Specifications

Specification	Value
Input voltage/Output voltage, V_{in} /V_o (V)	25/50
Load Resistance, *R* (Ω)	100
Inductance (conventional), *L* (mH) Inductance (interleaved), L_1, L_2, L_3 (mH)	1
Duty Cycle, *D*	0.5
Boost Ratio, *β*	2
Capacitance, *C* (μF)	470
Output Ripple, *r* (%)	1
Switching Frequency, *f* (kHz)	25
Power, *P* (W)	25

4.1. Input Current and Output Voltage Ripple

Same specifications are applied for both converters in this analysis. From the simulation results, it shows that input current and output voltage ripples in the 3-phase interleaved DC-DC boost converter have reduced compared to the conventional DC-DC boost converter as shown in Figure 3 and Figure 4, respectively. The experimental results show a good agreement with the design values, i.e., input current and output voltage ripples as shown in Figure 5 and Figure 6, respectively. Therefore, it is proved that the input current and output voltage ripples are greatly reduced in the 3-phase interleaved DC-DC boost converter compared to the conventional DC-DC boost converter.

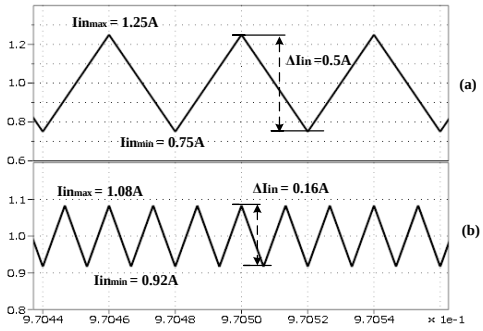

Figure 3. Simulation results of input current ripple: (a) Conventional DC-DC boost converter, (b) 3-phase interleaved DC-DC boost converter

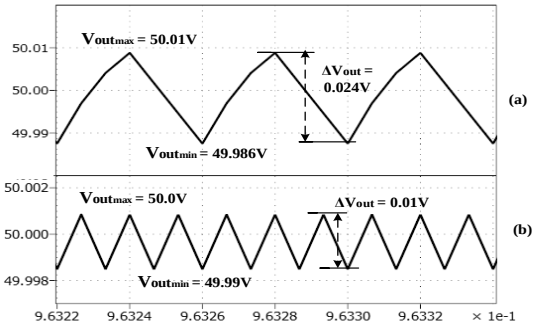

Figure 4. Simulation results of output voltage ripple: (a) Conventional DC-DC boost converter, (b) 3-phase interleaved DC-DC boost converter

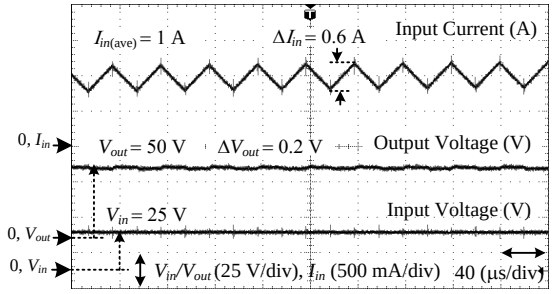

Figure 5. Experimental results of conventional DC-DC boost converter: Input current and input voltage and output voltage

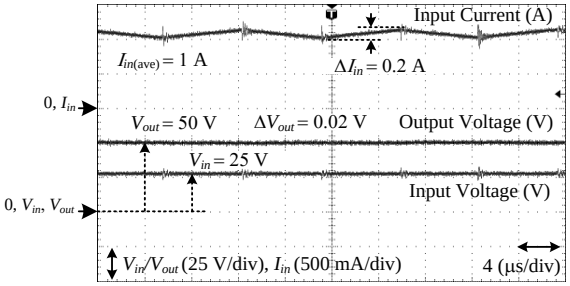

Figure 6. Experimental results of 3-phase interleaved DC-DC boost converter: Input current, input voltage and output voltage

4.2. Current Stress and Semiconductor Conduction Losses

From the experimental results as shown in Figure 7 and Figure 8, current stress (each phase) in the 3-phase interleaved DC-DC boost converter is reduced approximately 1/3 of the input current as compared to the conventional DC-DC boost converter. This is due to the three interleaving circuits at the input side and cause the phase currents are evenly distributed. In addition current stress on semiconductor devices are also reduced and leads to reduction on conduction loss of the semiconductor devices as expressed in (16).

Figure 9 and Figure 10 show the relationship between current stress and number of phase and the relationship between conduction loss and number of phase, respectively. It shows that when number of phase is increased, the current stress in each phase is reduced accordingly. Consequently conduction loss on semiconductor devices are also reduced. Meanwhile, Figure 11 and Figure 12 show the current stress on semiconductor devices in conventional and 3-phase interleaved DC-DC boost converter. It is obvious that in the 3-phase interleaved DC-DC boost converter the current stress in reduced according to the number of phase. Therefore, it is strongly agreed that by considering multiphase interleaved DC-DC boost converter, it reduces the current stress at low voltage and also conduction losses on semiconductor devices. Thus the overall converter reliability and efficiency are increased.

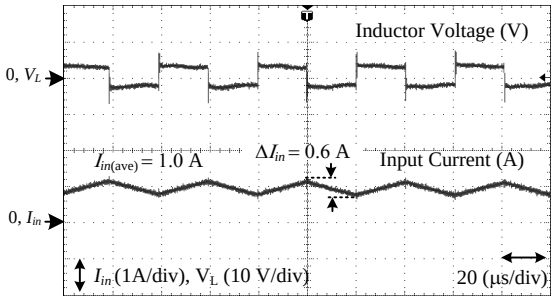

Figure 7. Inductor current (same as input current) for conventional DC-DC boost converter

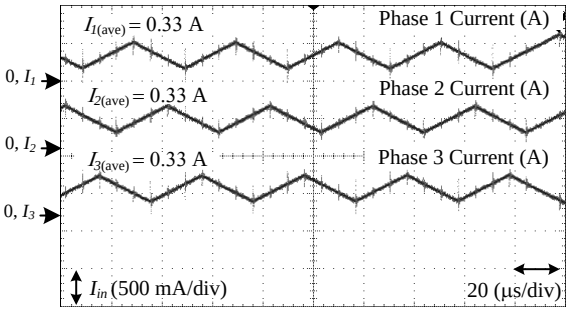

Figure 8. Inductor current (each phase) for 3-phase interleaved DC-DC boost converter

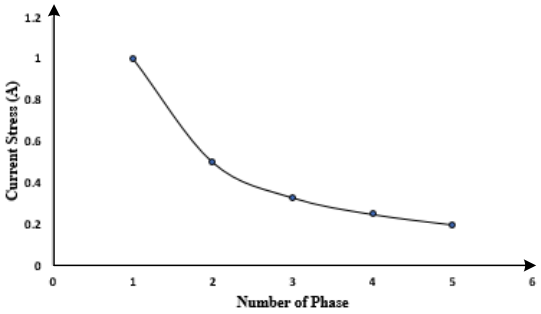

Figure 9. Current stress againts number of phase

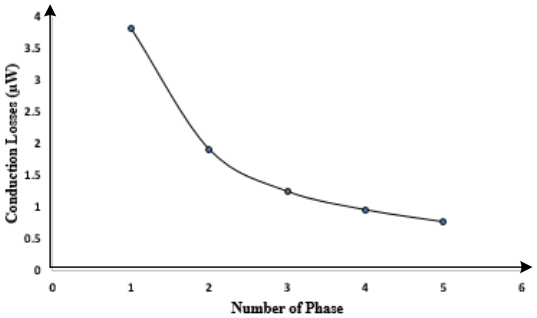

Figure 10. Conduction losses against number of phase

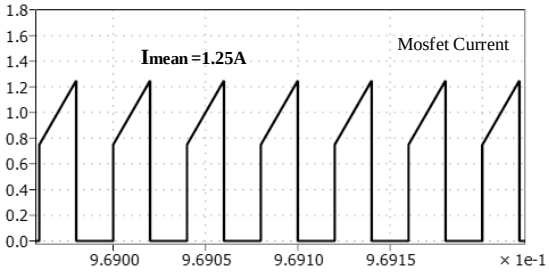

Figure 11. Semiconductor current stress in the conventional DC-DC boost converter

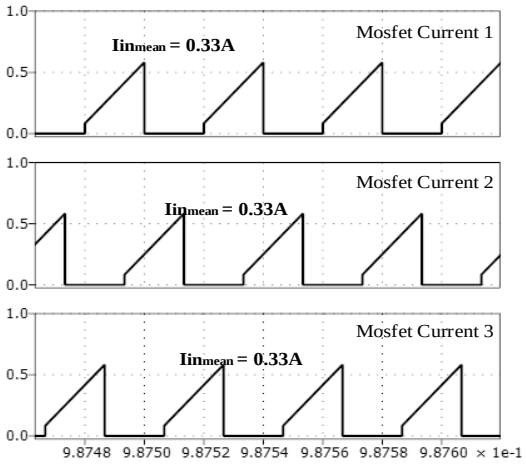

Figure 12. Semiconductor current stress in the 3-phase interleaved DC-DC boost converter

5. CONCLUSION

This paper has discussed and compared several parameters of the conventional DC-DC boost converter and 3-phase interleaved DC-DC boost converter. Based on the analysis, the current stress and the semiconductor conduction losses were reduced approximately 33% and 32%, respectively in the 3-phase interleaved DC-DC boost converter compared to the conventional DC-DC boost converters. In addition, due to multiphase interleaved configuration, it minimizes the semiconductor conduction losses in the converter. Besides, the input current and output voltage ripples were reduced due to interleaving switching technique. Therefore, with this circuit configuration, it can be considered in the RE applications whereby usually the voltage source is low and input current is high.

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