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A New Structure of the Nine Level Inverter Used as Active Power Filter with a Reduced Number of Swiches

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ABSTRACT

In the scope of this work, a new structure of the nine level inverter is proposed using a reduced number of power switches. This inverter is used as a shunt active power filter to compensate harmonic currents and the reactive power. The modeling and simulation of the proposed model were carried out in Matlab/Simulink environment. The simulation results show that the filtering performances were achieved despite the reduction of the switches number. It was found that the current waveform becomes purely sinusoidal with a reduction in the harmonic distortion rate (THD) to 2.68%. This implies good compensation of both harmonics and reactive power with a power factor closer to unity. Reducing the switches number allows reducing the switching losses and lowering the duration of the applied voltage supported by the semiconductors. The proposed topology also allows to get simple structure of the inverter with a reduced cost.

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1. INTRODUCTION

The inevitable use of control systems, including static power converters based on electronic components, can leads to a serious problem of electrical network pollution [1]. Therefore, a degradation in the electrical power quality appears in low quality of output voltage with high harmonic distortion, high electromagnetic inductive effects, high switching frequency and voltage stress applied on the switches [2]-[3].

Multilevel inverters are considered as an efficient solution to overcome the problem of electrical network pollution [4]-[5]. Recently, they are being extensively used in several application areas of medium and high power. They have a significant advantages in most electrical systems such as AC machines control, renewable energy converters and used in the electrical power quality improvement **[**6]-[7] in order to reduce the common mode voltage, minimize the voltage stress on power switches and to supply lower harmonic components in output voltage and current.

Several topologies of multilevel inverters have been proposed and applied in various fields [8]. The most known are: Neutral Point Clamped (NPC) inverters, Multiple Point Clamped (MPC) inverters the Flying Capacitors (CF) inverter [9] and the bridge cascade H-bridge inverter [10]-[11]. These conventional topologies require a large number of power switches to achieve a good output voltage quality with a high number of voltage levels [12]-[13].

Research activities in this field show that as the number of levels increase, the number of semiconductor switches is increased [14]. Therefore, the large number of power switches provoke a crowding in the circuit, difficulty in switches control, considerable energy losses and a high investment cost [15].

These drawbacks attracted the attention of researchers and becoming a challenge to the scientists for developing other topologies by reducing the switches number and maintaining the quality of the output voltage [16]-[17].

Conventional nine level inverter requires sixteen switches and three DC sources separately [18]. A reduction in the number of semiconductor switches for the nine level cascaded multilevel inverter has been reported in Reference [19] using twelve switches. The number of power switches for the nine level inverter has been more reduced to ten switches. Knowing that this inverter has been used for power supply AC motors [20].

In the scope of this work, a nine level ten-switch MLI topology is proposed. This inverter is used as a shunt active power filter to compensate harmonic currents generated by nonlinear loads and at the same time to compensate the reactive power. The proposed topology consists of four DC sources and built of three identical structures, each one is placed on a separate phases with a reduced number of power switches (30 IGBT) relative to conventional systems (48 IGBT). The active filter control used in this study is divided into two parts. The first deals with the harmonic isolator based on the instantaneous power theory (*pq* theory), [21]-[22] in order to extract harmonic currents. The second part is devoted to the logic signals generation to control the filter switches using the Pulse Width Modulation (PWM) technique. This type of control allows the injection of a compensation current equal to the reference one to obtain a sinusoidal form of the supply current into the network. The control of the DC bus voltage is performed by a Proportional Integral (PI) regulator used to correct the appropriate error value between the reference and the injected currents.

The simulation tests were performed in Matlab/Simulink environment. The results showed that the filtering performances have been well improved using the proposed nine level MLI topology with ten-switch. This improvement appears in the remarkable reduction of the harmonic currents and in the waveform of the supply current which becomes purely sinusoidal and in phase with the voltage. The simulation shows also that the three phase voltages have the same amplitudes.

2. NINE LEVEL TEN-SWITCH TOPOLOGY DESCRIPTION

The location of the new active power filter proposed in this work is illustrated in Figure 1. It is placed in parallel to the nonlinear load and the three-phase supply source. It is placated as close as possible to the nonlinear load in order to prevent harmonics propagation in the distribution network and getting high power quality [22].

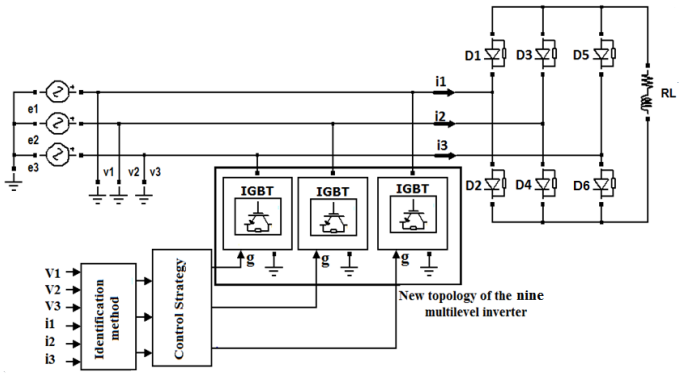

Figure 1. The proposed nine level active power filter location in the network.

The block diagram of the nine level ten-switch inverter topology is illustrated in Figure 2. It is mainly composed of three identical structures by phase. Each structure is composed of 10 IGBT power switches instead to 16 IGBT power switches in the conventional system [23]. The DC bus voltage (V_{DC}) can generate nine levels, namely: V_{DC}, $V_{DC}/2$, $V_{DC}/3$, $V_{DC}/4$, 0, $-V_{DC}/4$, $-V_{DC}/3$, $-V_{DC}/2$ and $-V_{DC}$. The V_{DC} voltage is uniformly distributed over four identical capacitors (*C1, C2, C3* and *C4*) connected in series. The four switches *k1, k2, k3* and *k4* are used to form the H-bridge, while the switches *k5, k7* and *k9* are connected in series with *k6, k8* and *k10*, respectively.

To maintain the zero level at the inverter outlet, *k1* and *k3* are turned on (Figure *3-i*). Whereas, *k1* and *k4* are turned on to get $Van=V_{DC}$ on Figure *3-a*. To invert the output voltage ($Van=-V_{DC}$), *k2* and *k3* are turned on Figure 3-b. *k1, k7* and *k8* are switched on to generate $3V_{DC}/4$ on Figure 3-c and *k2,k9* and *k10* are

switched on to generate $-3V_{DC}/4$ Figure 3-d. *k1*, *k5* and *k6* are turned on to generate $V_{DC}/2$ level Figure *3-e* and to obtain lower inverter voltage $-V_{DC}/2$, *k1*, *k7* and *k8* switches are turned on Figure *3-f*. The $V_{DC}/4$ level appears when the switches *k1*,*k9* and k10 are switched on Figure 3-g,where as to produce $-V_{DC}/4$, *k2*, *k7* and *k8* are turned on Figure *3-h*.

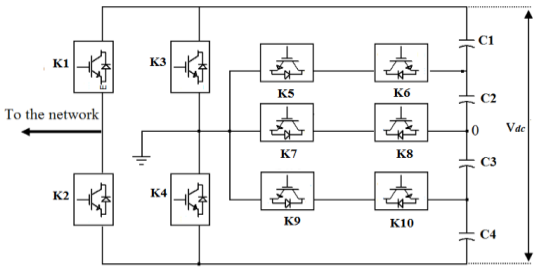

Figure 2. The structural diagram of the proposed nine level ten-switch Inverter.

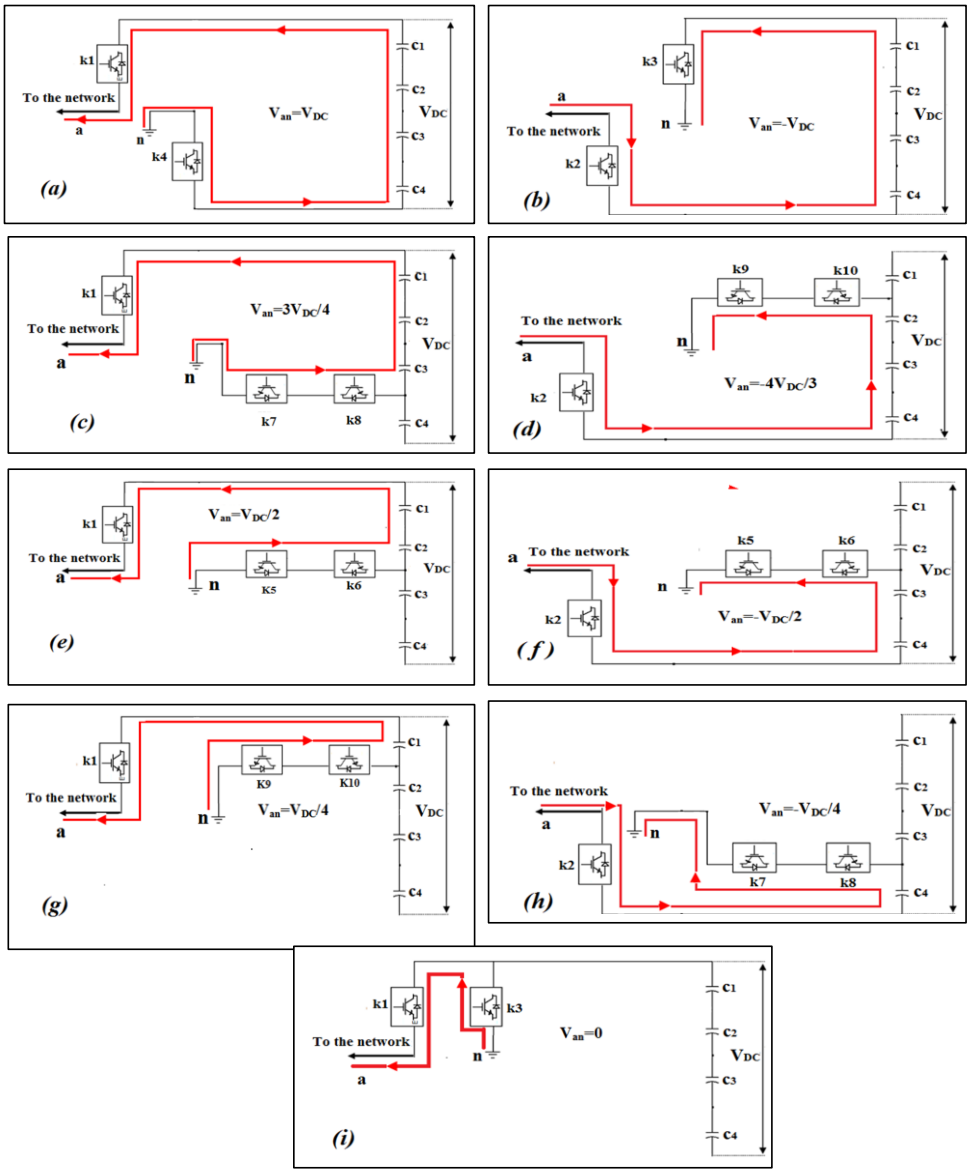

Figure 3. The possible configurations of the proposed nine level inverter.

3. IDENTIFICATION OF THE HARMONIC CURRENT

To get a high filtering quality, reference current identification method is the most efficient technique used to extract harmonic currents. There are several algorithms with different degree of complexity, such as the technique of instantaneous powers *(PQ)* introduced by *H. AKAGI* to extract reference harmonic currents [24]-[25]. The *CLARK* transformation is used to convert the balanced three-phase voltages *(v1,v2, v3)* or/and currents *(i1, i2, i3)* to the biphase system defined by components (*vα, vβ)* and *(iα, iβ),*respectively as presented by the following equations.

$$\begin{bmatrix} i\alpha \\ i\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i1 \\ i2 \\ i3 \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} v\alpha \\ v\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v1 \\ v2 \\ v3 \end{bmatrix} \quad (2)$$

Where, α and β axes coincide with the real and imaginary axes of the complex plane.Thus, the three phase voltage and current system can be expressed as follows:

$$\begin{cases} v = v_\alpha + jv_\beta \\ \mathrm{i} = i_\alpha + ji_\beta \end{cases} \quad (3)$$

So, the complex apparent power is given by:

$$\mathrm{S} = \left(v_\alpha + jv_\beta\right)\left(i_\alpha + ji_\beta\right) \quad (4)$$

The instantaneous active power is obtained by equation (5) and the instantaneous reactive power is calculated by equation (6).

$$\mathrm{P} = \left(v_\alpha i_\alpha + v_\beta i_\beta\right) \quad (5)$$

$$\mathrm{q} = \mathrm{j}\left(v_\beta i_\alpha - v_\alpha i_\beta\right) \quad (6)$$

The instantaneous power P and q can be decomposed in two terms; the first is corresponding to its mean value *($\bar{p}$, $\bar{q}$)* and the second term is corresponding to the fluctuation power *($\tilde{p}$, $\tilde{q}$)*. A second order high-pass filter is used to separate the power components related to the harmonic and to the fundamental. The separation scheme is illustrated in Figure 4.

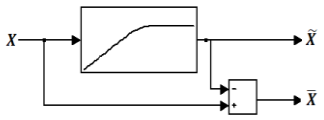

Figure 4. Power separation shame.

The cutoff frequency is selected depending on the load, allowing the passage of the powers harmonic components and block the passage of continuous components of active and reactive power of the fundamental. After separating the powers, we can calculate the harmonic and the reactive current simultaneously from the following matrix.

$$\begin{bmatrix} i\alpha_{ref} \\ i\beta_{ref} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ \bar{\mathrm{q}} \end{bmatrix} + \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} \tilde{\mathrm{p}} \\ \tilde{\mathrm{q}} \end{bmatrix} \quad (7)$$

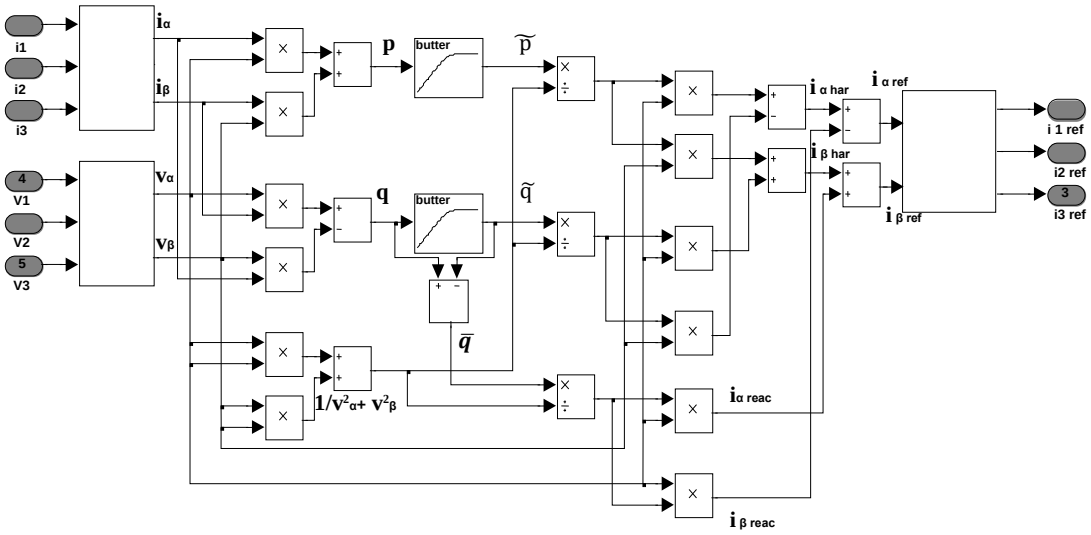

Figure 5. Identification scheme of the harmonic and reactive currents.

4. ACTIVE FILTER CONTROL STRATEGY

After determining of reference currents by the instantaneous power technique the control of IGBT switches is carried out by the comparison between reference currents (iref1, iref2, iref3) and eight triangular carriers using the Phase Disposition Pulse Width Modulation (PDPWM) method as presented i**n** Figure 6 [26]. This comparison will generates logic signals to the IGBTs as illustrated in the logic flowchart presented in Figure 7.

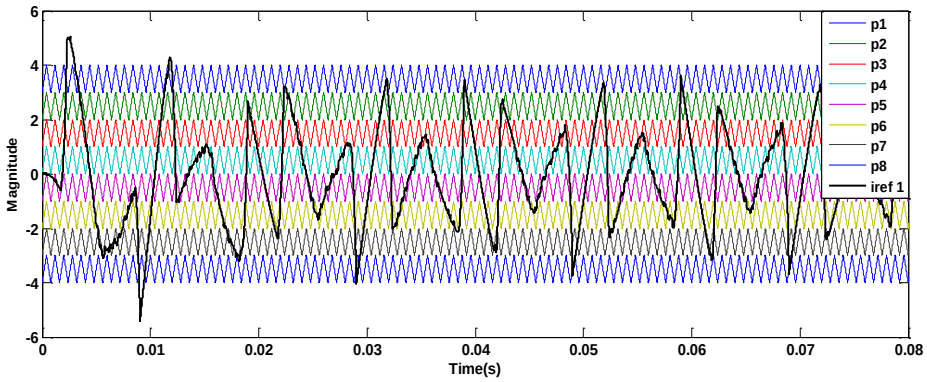

Figure 6. Eight triangular carriers disposed in phases.

5. DC BUS VOLTAGE REGULATION

It is recommended that the DC bus voltage across the capacitors (*C1, C2, C3, and C4*) of the remains constant. The regulation of DC voltage is necessary in order to limit the fluctuations and prevent semiconductors failure. It is therefore important to find a controller which is insensitive to parameter variations and disturbances and also appropriate to parameters closed loop control. Switches commutation can generate fluctuations in the V_{DC} voltage, capacitor losses and a delay in the control system. For these reasons, the propesed nine level active filter is used as a controlled rectifier, aiming to compensate the DC bus voltage variations by transferring a small quantity of AC active power to the other side of the DC current filter. For this purpose, the control of the DC bus voltage is performed by a Proportional Integral (PI) regulator used to correct the appropriate error value between the reference and the injected currents.

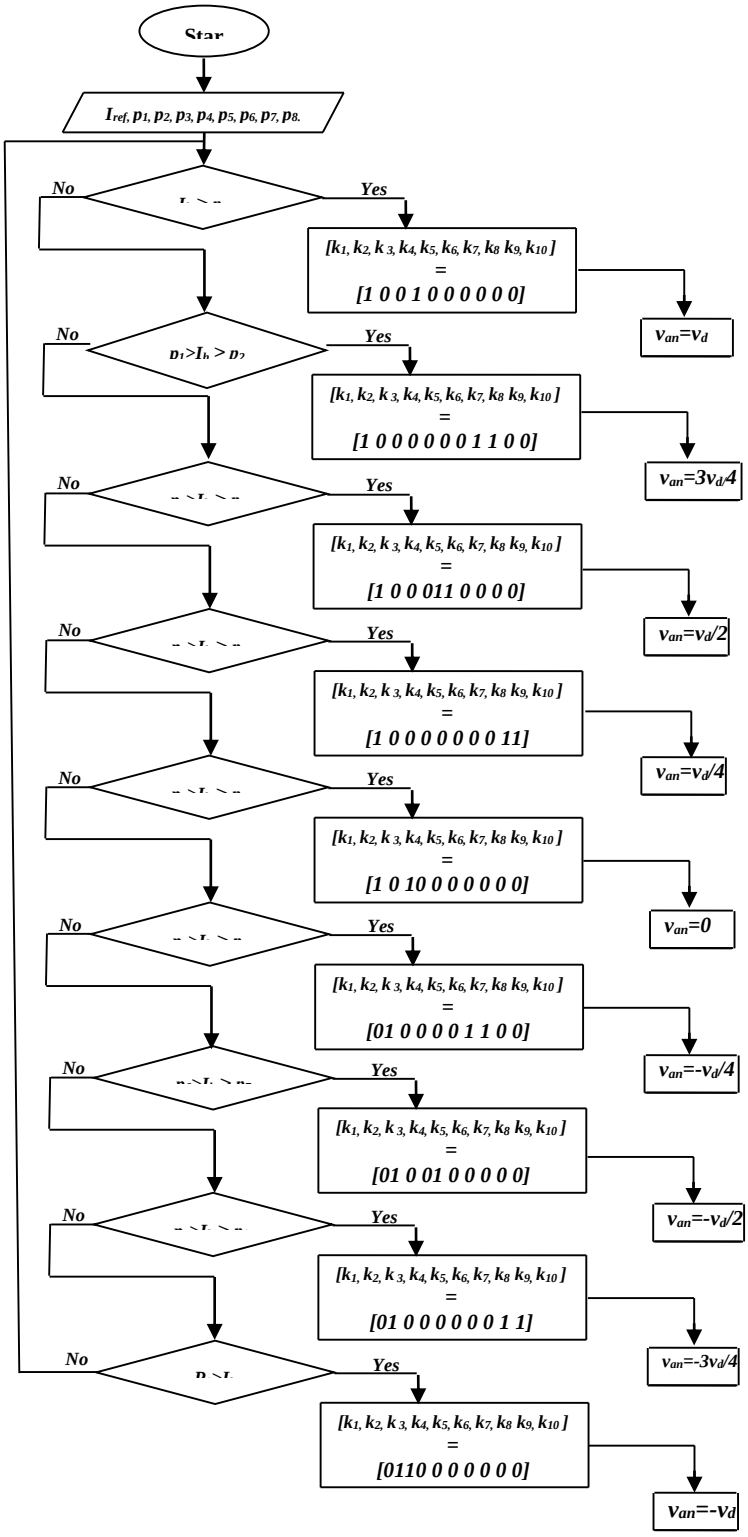

Figure 7. Logic signals generation flowchart.

6. MODELING AND SIMULATION

The nine level inverter topology proposed in this work has been modeled as illustrated in Figure 8. The simulated model is composed of three-phase supply sources, a polluted load and a nine level parallel active power filter. The simulation is performed using Matlab/Simulink environment. The obtained

simulation results relate to the phase (1) of the current. Whereas the phases (2) and (3) are shifted by 120° from each other's. The blocs diagram simulation parameters are presented in Table 1.

Table 1. Simulation parameters.

Source supply		Pollution load		Ninen level active power filter	
Vs	*220 V*	$L_{C\text{-}input}$	*0.003 H*	*Vdc*	*1000 V*
Ls	*0.003 H*	$L_{C\text{-}output}$	*0.001 H*	*Lf*	*0.01 H*
		R_C	*20* Ω	*Rf*	*10* Ω
				f_s *(switching frequency)*	*10 kHz*

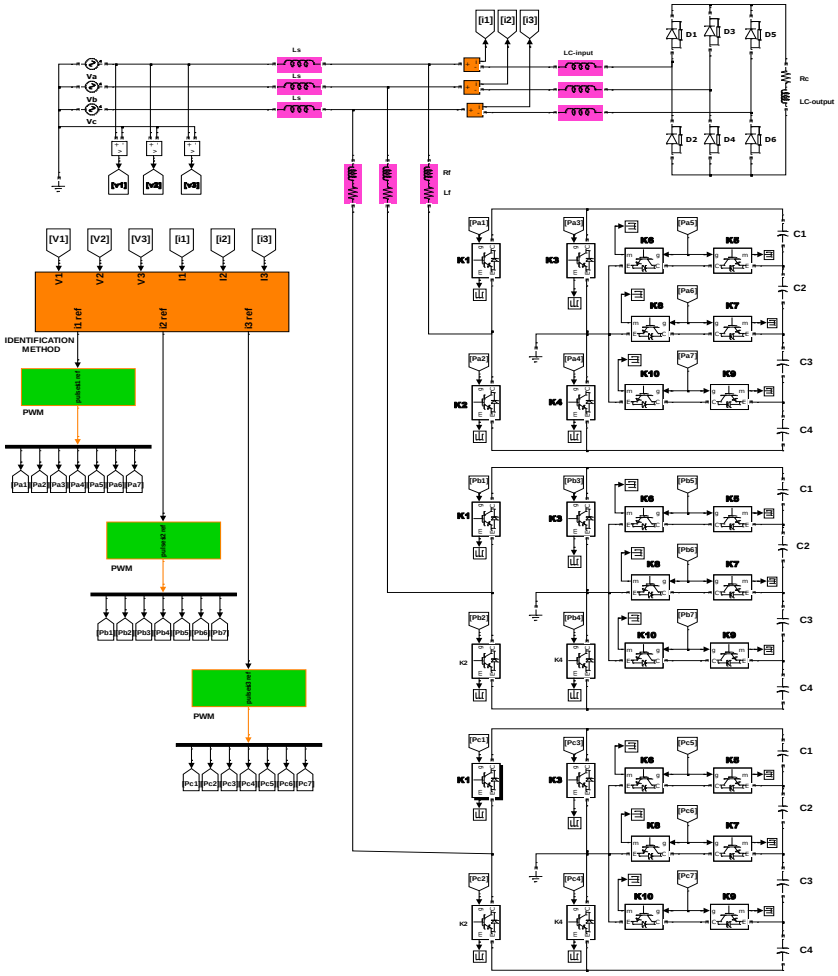

Figure 8. Modelling strategy of the proposednine level inverter.

7. RESULTS AND DISCUSSION

The main operating characteristics of the shunt active power filter, namely: the supply voltage, the switches pulses, output voltage, the identified harmonic and injected currents as well as the line current and its frequency spectrum were presented before and after filtering in figures 9-15.The waveforms of these parameters are presented for evaluation and comparison study. In addition, active and reactive powers before and after filtering, as well as the shift between the current and the voltage source are also presented.

7.1. Before filtering

Figure 9 shows the source voltage, load current and load current spectrum before filtering. It is clear that the supply voltage has a pure sinusoidal waveform. However, the associated load current presents a

distortion in the waveform as estimated by the harmonic frequency spectrum with a high harmonic distortion rate (THD) of 27.41% which largely exceeds the recommended value (THD<5%) [27].

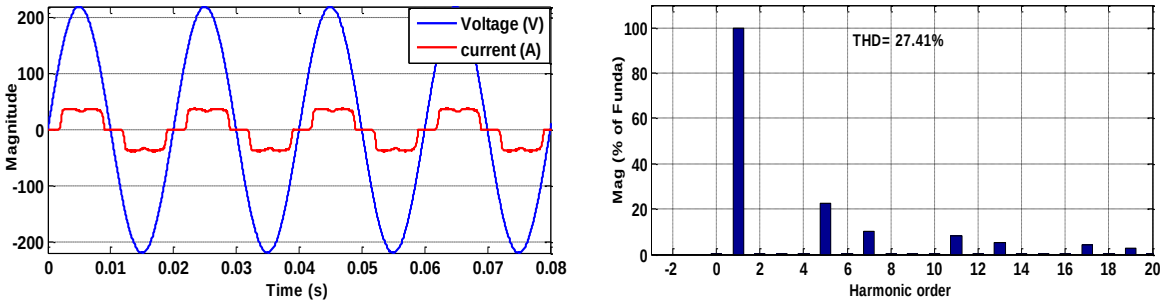

Figure 9. Supply voltage, load current and load current spectrum (fundamental) before filtering.

7.2. After filtering

Figure 10 shows the waveform of the injected current (injected by the proposed inverter) and the harmonic current identified by the instantaneous power method (PQ). It can be seen that the response time of the proposed nine level inverter is very short (about 0.14s), which reflects the robustness of the harmonic current identification method.

The line current and its frequency spectrum after filtering are illustrated in figure 11. The injected current from the proposed active power filter makes the supply current waveform purely sinusoidal. The harmonic frequency spectrum shows the elimination of almost all the harmonics with an estimated THD of 2.68%. This presents a significant reduction in the THD value by about 90% in comparison to that before filtering (THD=27.41%).

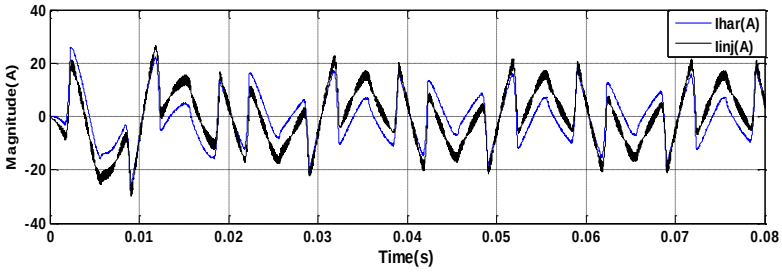

Figure 10. Identified harmonic and injected currents.

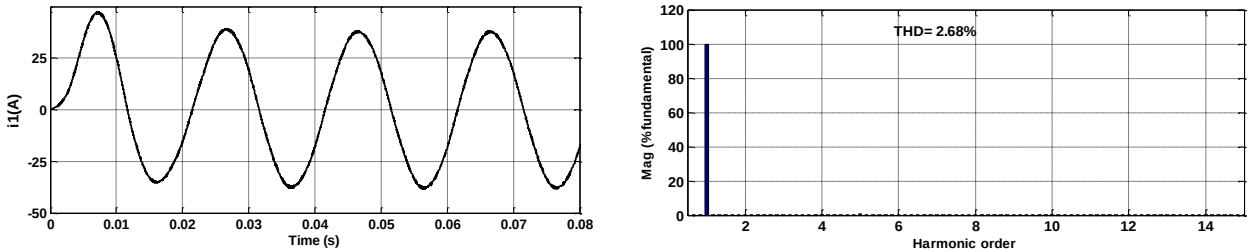

Figure 11. Line current and its frequency spectrum after filtering.

7.3. Switches pulses

Figure 12 shows the pulses of the switches *K1*, *K2*, *K3* and *K4*. A significant decrease is observed in the opening intervals with an increase in the switches closing intervals. As a result, reducing the switching number allows a decrease in the switching losses with a reduction in the duration of the applied voltage

supported by the semiconductors. The required condition that the switches (*K1*, *K2*) or (*K3*, *K4*) does not conduct the current simultaneously is verified to avoid short-circuit.

Figure 13 shows clearly the nine voltage levels, namely: *1000V, 750V, 500V, 250V, 0V, -250V, -500V, -750V, -1000V*, provided by the proposed active power filter. Despite the reduced number the switches, the proposed model appears able to provide nine levels of voltage.

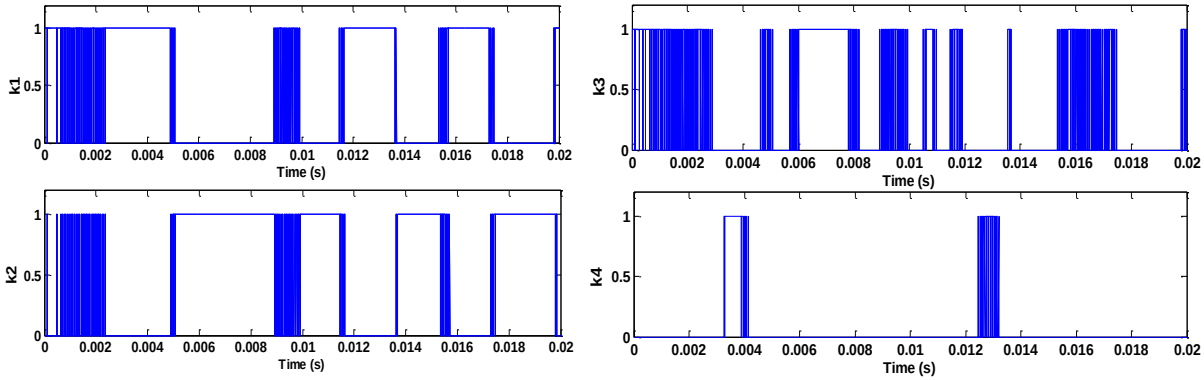

Figure 12. Opening and closure sequences of the switches (*K1*, *K2*, *K3* and *K4*).

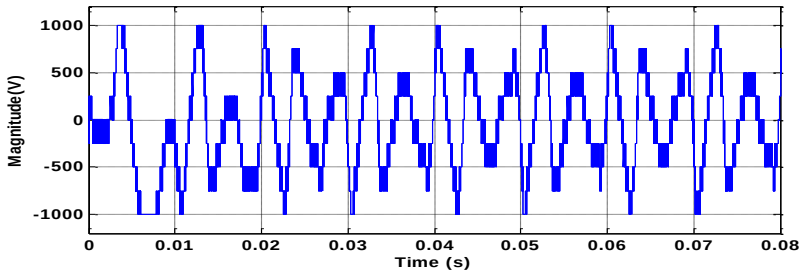

Figure 13. Output voltage showing the nine level of the proposed MLI.

7.3. Power factor

The reactive and active power before and after filtering are illustrated in figure 14. The simulation shows a drop in the reactive power close to zero with a reduction of about 1800VAR.While, the active power increases from 2900W to about 3900W. The phase shift between the current and the voltage source is shown in figure 15. It is clear that combining between: the identification method, the control strategy algorithm and the proposed topology (nine level MLI) allows to the source current to be in phase with the supply voltage with a power factor (cosφ) close to unity. Figure 16 illustrates the currents (i1, i2, i3) which have sinusoidal waveforms with balanced phases 1, 2 and 3. Furthermore, the waveforms of the currents have the same amplitudes with the same frequencies.

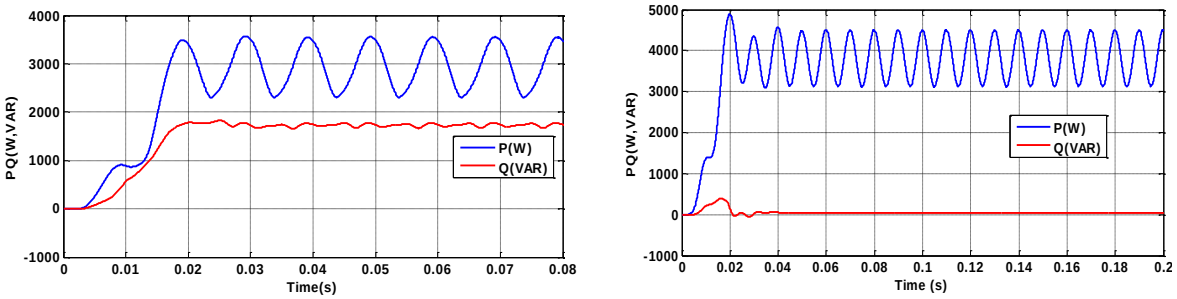

Figure 14. Reactive power and active power before and after filtering.

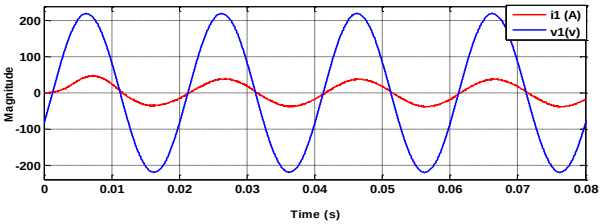

Figure 15. Phase shift between the current and the voltage source.

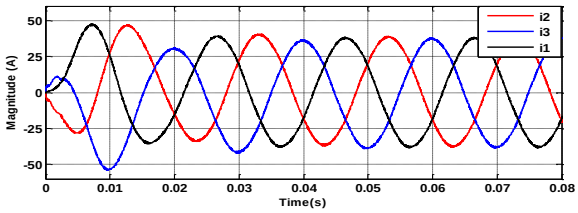

Figure 16. currents waveform after filtering.

7.4. Comparative analysis with previous studies

The comparative study between the proposed topology and some previous topologies [28]-[30] is presented in Table 2. The comparison shows that a nine level inverter can be realized with ten IGBT transistors for each phase. Unlike conventional systems such as NPC and cascade type inverters [29][30] which require sixteen IGBT transistors, the proposed nine-level topology having less crowded and less expensive structure while maintaining the system performances.

Table 2. Comparison with previous studies

Reference	Inverter type	Switching number/phase	THD (%)	Area of use
Haddad et al. [28]	Seven-level	12	2.27	Shunt active power filter
Rajasekar et al. [29]	Nine-level	16	2.93	Shunt hybrid active power filter
Lada et al. [30]	Nine-level	16	3.15	Shunt active power filter
Present study	Nine-level	10	2.68	Shunt active power filter

8. CONCLUSION

In this work, a new structure of nine level inverter is proposed using ten power switches by phase instead to sixteen IGBT in the conventional system. This inverter is used as a shunt active power filter to compensate the harmonic currents and the reactive power. The simulation was carried out in Matlab/Simulink environment. From the results obtained in the scope of this study, the following conclusions may be drawn:

1. The current waveform become purely sinusoidal with a reduction in the harmonic distortion rate (THD) from 27.41% to 2.68%.
2. Reducing the number of switches reduces switching losses.
3. Reducing the switching number reduces the duration of the applied voltage on the semiconductors.
4. Despite the reduced number of switches, the proposed model is able to provide nine level of voltage.
5. The three currents of the network have the same amplitudes with balanced phases.
6. Good compensation of the harmonics and reactive power is obtained with a power factor closer to unity in accordance with IEEE standards.
7. Reducing the number of power switches allows to get simple structure of the inverter with a reduced cost.

REFERENCES

[1] Chebabhi A, Fellah MK, Abdelhalim K, Benkhoris MF. Fuzzy logic controllers for three levels shunt active power filter compensated by three-levels stabilizing space vector modulation to fixed switching frequency and switching lasses reducing under unbalanced load. *The Mediterranean Journal of Measurement and Control*. 2015; 11(1): 357-366.

[2] Kannan R, Jagabar Sathik MA, Selvam S. A New Symmetric Multilevel Inverter Topology Using Single and Double Source Sub-Multilevel. Inverters *Journal of Power Electronics.* 2015; 15(1): 96-105.

[3] Kale M, Özdemir E. Corrigendum to Harmonic and reactive power compensation with shunt active power filter under non-ideal mains voltage. *Electric Power System Research*. 2005; 74(3): 363-370.

[4] Bassi HM. A Modulation Scheme for Floating Source Multilevel Inverter Topology with Increased Number of Output Levels. *International Journal of Electrical and Computer Engineering (IJECE)*. 2016; 6(5): 1985-1993.

[5] Jyothi B, Gopala Rao MV. Performance Analysis of 3-Level 5-Phase Multilevel Inverter Topologies. *International Journal of Electrical and Computer Engineering (IJECE)*. 2017; 7(4): 1696-1705.

[6] José R, Jih-Sheng L, Fang Zheng P. Multilevel Inverters: A Survey of Topologies, Controls, and Applications. *IEEE transactions on industrial electronics.* 2002; 49(4): 724-737.

[7] Bouzidi M, Benaissa A, Barkat S. Sliding mode Control using 3D-SVM for Three-phase Four-Leg Shunt Active Filter. *International Journal of Power Electronics and Drive System (IJPEDS)*. 2013; 3(2): 147-54.
[8] Krishna K, Alekh R, Pallavee B, Lalit Kumar S, Shailendra J. Multilevel Inverter Topologies with Reduced Device Count. *IEEE Transactions on Power Electronics*. 2016; 31(1):135-151.
[9] Patricio C, Jose R. Model predictive control of multilevel cascaded h-bridge inverters. *IEEE Transactions on Industrial Electronics*. 2010; 57(8): 2691-2699.
[10] Ilhami C, Ersan K, Ramazan B. Review of multilevel voltage source inverter topologies and control schemes. *Energy Conversion and Management*. 2011; 52(2): 1114-1128.
[11] Rosli O, Rasheed M, Marizan S., Tamijis MR. Comparative Study of a Three Phase Cascaded H -Bridge Multilevel Inverter for Harmonic Reduction. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2015; 14(3): 481-492.
[12] Sathik MJ. A new multilevel inverter topology using less number of switches. *International journal of engineering science and technology (ijest).*2011 vol. 3(2): 1500-1510.
[13] Ehsan NA, Halim MY. Implementation of a New Multilevel Inverter Topology. *IEEE Transactions on Industrial Electronics*. 2012; 59(11): 4148-415.
[14] Gnana Prakash M, Balamurugan M, Umashankar S. A New Multilevel Inverter with Reduced Number of Switches. *International Journal of Power Electronics and Drive System (IJPEDS)*. 2014 5(1): 63-70.
[15] Vipul K, Arvind M, Abid HS. A New Model of H-Bridge Multilevel Inverter for Reduced Harmonics Distortion. *Journal of Engineering Research and Applications*. 2014; 4(11): 30-35.
[16] Zhong D, Leon MT, Burak O, John NC. Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter. *IEEE Transactions on Power Electronics*. 2009; 24(1): 25-33.
[17] Devarajan N., Reena A. Reduction of switches and DC sources in Cascaded Multilevel Inverter. *Bulletin of Electrical Engineering and Informatics*. 2015; 4(3): 186-195.
[18] Sudha T. Comparison between Cascaded Multilevel Inverter and Reduced Switch Multilevel Inverter. *International Journal for Research in Applied Science & Engineering Technology (IJRASET)*. 2016; 4(5): 500-510.
[19] Anilkumar KK, GeethaB, EldhoseKA.ReversingVoltage Nine Level Inverter Topology with Universal Control. *Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering*. 2014; 3(5): 108- 115.
[20] Rajeevan PP, Sivakumar K, Gopakumar K, Patel C, Abu-Rub H. A Nine Level Inverter Topology for Medium-Voltage Induction Motor Drive with Open-End Stator Winding. *IEEE Transactions on Power Electronics*. 2013; 60(9): 3627-3636.
[21] Saad S, Zellouma L. Fuzzy Logic Controller for Three Level Shunt Active Filter Compensating Harmonics and Reactive Power. *Electric Power Systems Research*. 2009; 79(10): 1337-1341.
[22] Zahzouh Z, Khochmane L, Haddouche A. A New Multilevel Active Power Filter Using Switches Meticulously Controlled. *International Journal of Power Electronics and Drive System (IJPEDS)*. 2015; 6(1): 168-177.
[23] Young CM, Chu NY, Hsiao YC, Li CZ. A Single Phase Multilevel Inverter with Battery Balancing. *IEEE Transactions on Power Electronics*. 2013; 60(5): 1972-1978.
[24] Hadj Benali F, Azzouz F. Comparison of Instantaneous Reactive and Notch Filter Algorithms Seven Level Parallel Active Filter. *International Journal of Electrical and Computer Engineering (IJECE)*. 2017; 7(4): 1788-1779
[25] Balamurugan CR, Natarajan SP, Bensraj R, Shanthi B. A Review on Modulation Strategies of Multi Level Inverter. *Indonesian Journal of Electrical Engineering and Computer Science.* 2016; 3(3): 681-705.
[26] Akagi H. New trends in active filters for power conditioning. IEEE Transactions on Industry Applications. 1996; 32(6): 1312-1322.
[27] Duffey CK, Stratford RP. Update of Harmonic Standard IEEE-519: Recommended Practices and Requirements for Harmonic Control in Electric Power System. *IEEE Transactions on Industry Applications*. 1989; 25(6): 1025-1034.
[28] Haddad M, Ktata S, Rahmani S, Al-Haddad K. *A nonlinear control strategy for three-phase seven-level Shunt Active Power Filter*. 16th international conference on Sciences and Techniques of Automatic control & computer engineering. 2015; 576-581.
[29] Rajasekar S, Senthilkumar A, Shasi Kumar Y, Ajay-D-VimalRaj P. Power quality enhancement using cascaded multilevel inverter based shunt hybrid active power filter. *International Journal of Engineering, Science and Technology*. 2011; 3(9): 37-46.
[30] Lada YM, Sabiq Safiuddin M, Johar Akbar MG, Mohamad Riduwan MN, Gan Chin K. Reduction of *Harmonic using Single Phase Shunt Active Power Filter based on Instantaneous Power Theory for Cascaded Multilevel Inverter*. Power and Energy (PECon), 2016 IEEE International Conference. Melaka, Malaysia. 2016; 702-706.

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