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# Digital Control of Three-Phase Cascaded Multilevel Inverter Using FPGA Wavect Tool

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**ABSTRACT**

The multi carrier modulation technique is the most employed PWM technique for cascaded multilevel inverter (CMLI) since this control strategy can be easily extended to higher number of levels of output compared to space vector PWM technique. This paper proposes a modified multi carrier PWM technique for three-phase CMLI. The proposed PWM technique has been implemented using MATLAB Xilinx System Generator, which automatically generate code from system model. The hardware implementation of the three-phase CMLI has been carried out to substantiate the working of proposed PWM technique. Novel FPGA Wavect digital controller is used to generate the PWM pulses, which is a real time simulator and controller. This digital controller improves the accuracy of the hardware implementation. Hardware implementation of proposed control strategy for three-phase CMLI with RL load proves that the proposed PWM technique results in improved power output quality with reduced harmonic components.



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## 1. INTRODUCTION

Multilevel inverters are widespread converters, which have most application ranging from medium to high power applications such as power converters in STATCOM for VAR compensation, in HVDC transmission, in medium and high voltage variable speed induction motor drives, in PV power generation, UPS, flexible AC transmission system etc. Cascaded multilevel inverters are used in most of the above mentioned applications because of its modular and flexible topology. The use of identical power cells makes cascaded multilevel inverter to have modular structure, which reduces the cost of the converter as well [1]-[5]. A single phase cascaded multilevel inverter is constructed by connecting H- bridge inverters in series. A three-phase cascaded multilevel inverter is composed of three single phase H-bridges, which will produce output voltages with balanced phase. The objective of PWM fed three-phase inverters is to have a controlled magnitude and frequency output voltages with the constant input voltage source [6]. As the number of output level in the multilevel inverter increases the complexity of control strategy also increases. To obtain balanced three-phase output voltages different modulation technique discussed in literature [7]-[11] are:

a. Selective Harmonic Elimination Technique (SHE PWM)
b. Space Vector PWM technique (SVPWM)
c. Sine PWM Technique (SPWM)

In SHE PWM technique, appropriate switching angles are found to eliminate odd harmonic of particular interest and to control the fundamental voltage. Hence selected harmonics are eliminated with the smallest number of switching. An elementary drawback associated with such method is to obtain the arithmetic solution of nonlinear transcendental equations which include trigonometric terms. Due to high complexity, solving the harmonic elimination non linear equations real time operation is considered impractical. Also SHE PWM provides highest power quality only at fundamental switching frequency [8].

In SVPWM technique, the voltage reference is provided using a revolving reference vector which is also used to control the output voltage magnitude and frequency. In SVPWM the DC bus is utilized more efficiently with reduction in harmonic distortion compared to SHE PWM and SPWM technique. The SVPWM technique can increase the fundamental component by up to 15% that of SPWM. SVPWM technique is extensively used in speed control of AC drives, brushless motors and permanent magnet synchronous motors. The drawback of this technique is, as the number of output level on the inverter side increases the redundant switching states and the complexity of selecting switching states increases. This leads to intensive calculation for vector frames [7]-[8] and [10].

The drawback of implementation complexity in SHE PWM technique and SVPWM technique can be overcome by Multi Carrier PWM (MCPWM) of SPWM technique. MCPWM technique is extensively used in cascaded multilevel inverters as it is less complex, easy to implement even for higher number of levels at inverter output and easy control of output voltage magnitude and frequency [12]-[14]. In MCPWM technique the three-phase reference modulating waves which have 120° phase shift are compared with a common triangular carrier wave to generate corresponding switching pulses for three phase inverter. The output voltage magnitude and frequency can be controlled by changing the magnitude and frequency of modulating signal. The voltage varies linearly from 0% to 78.5% which results in poor DC bus voltage utilization. Hence voltage range has to be improved by increasing the DC bus utilization at the same time reducing the harmonics [7].

In this paper an effort has been made to address the drawback of poor voltage utilization of SPWM technique. This paper uses a new modulating wave elliptical wave [15]-[16] replacing sine modulating wave in SPWM technique. This result in increased DC bus utilization as in case of SVPWM technique to improve output voltage range and reduce the harmonics. The simulation of proposed modulation technique is carried out on MATLAB Xilinx System Generator (XSG) platform. The control strategy can be implemented by use of readily available system generator blocks and subsystems. XSG tool extract automatic code from the system model to realize the hardware in a particular FPGA bit stream. This type of design approaches result in increased productivity and reliability [17]-[20].

To validate the simulation results, the proposed control strategy is implemented digitally using FPGA Wavect controller and generated pulses were applied to Semikron make Three-phase 5-level cascaded H-bridge inverter with RL-load. The Wavect software tool makes the hardware implementation more accurate. The Wavect is a real time capturing and plotting of analog voltage and current signals. It can have a direct link to MATLAB Simulink software. Using this software the algorithms can be schematically represented in XSG Simulink environment and the generated code can be transferred to FPGA controller for hardware implementation. Voltage, current and speed sensors present in the tool makes ADC and sensor interfacing simple [21].

The simulation results and hardware implementation results of the proposed PWM technique for a three-phase 5-level cascaded inverter closely agrees with each other. The range of the output voltage of the inverter has increased indicating higher DC bus utilization. The Wavect controller has resulted in reducing the implementation time of the control strategy.

## 2. MODIFIED MULTICARRIER PWM TECHNIQUE

### 2.1. Generation of Elliptical Modulating Wave Using XSG

In the proposed MCPWM technique, the ellipse wave is compared with triangular carrier wave. The equations used to generate the elliptical wave are given by [15]:

$$A = a(i) + r \times \cos(t) \quad (1)$$

$$B = b(i) + V_m \times \sin(t) \quad (2)$$

Where in the equation (1) and (2):
r - is the radius of the elliptical wave which represents the frequency and
Vm - is the amplitude of the elliptical wave.
A and B are the Coordinates of elliptical wave at any instant of time t.

Figure 1 shows the algorithm for generating the elliptical wave. The required frequency and amplitude of the modulating elliptical wave is given as the input. The initial x-axis coordinates and y-axis coordinates are calculated from the input data. The elliptical wave is drawn from the calculated (a, b) coordinates from (0 to 2π). The elliptical modulating wave generated on MATLAB XSG platform using logic blocks is shown in Figure 2. The counters and ROM blocks are used to create elliptical wave for a frequency of 50Hz.

For a frequency of 50Hz, the time period is 0.02 sec.

The total steps for the counters with clock period of 25nsec, $\frac{0.02}{25n} = 8{,}00{,}000$

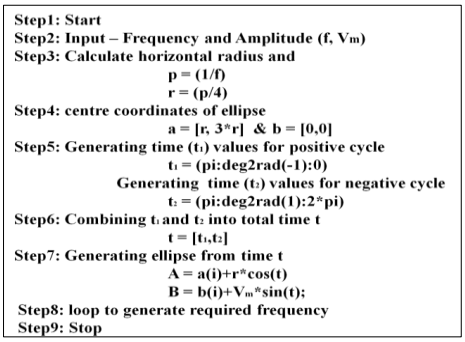



Figure 1. Algorithm for generating Elliptical Wave

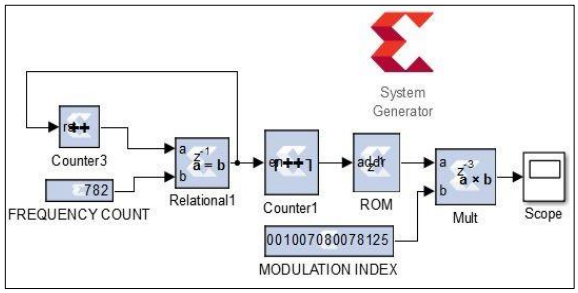



Figure 2. Generation of ellipse wave using XSG

The counter used to generate elliptical modulating wave should count from 0 to 7,99,999. With ROM block holding the depth of 1024 bytes leads to count of = $\frac{800000}{1024} \approx 782$

(782 X 1024) count is split into two steps. The counter3 in Figure 2 will count from 0 to 782 and counter1 will count from 0 to 1023. The equations to generate the elliptical wave are stored in ROM and magnitude of the elliptical wave is set by modulation index block. Similarly, the four carrier waves are generated with a frequency of 2000Hz. For a frequency of 2000Hz, the time period is 0.5msec.

The total steps for the counters with clock period of 25nsec, $\frac{0.5m}{25n} = 20{,}000$

The counter used to generate carrier wave should count from 0 to 19,999. In this case, the counter3 counts from 0 to 20 and counter1 from 0 to 999 to generate a triangle wave.

Among the variants of MCPWM technique, Phase Disposition PWM (PDPWM) technique is selected to generate the PWM pulses to verify the performance of elliptical modulating wave. In the PDPWM technique, elliptical modulating wave of frequency 50Hz is compared with four triangle waves which are phase disposed one above the other, having the same amplitude of 1V and frequency of 2000Hz. The control logic block of PDPWM technique is implemented using MATLAB XSG blocks. The generated triangle waves and elliptical wave which are plotted in a single scope and the switching pulses generated from the comparison is shown in Figre 3.

The PDPWM technique is implemented using both 'elliptical' and 'sine' wave as reference and the generated pulses from two methods were applied to single phase CMLI to analyze the performance [14]. Figure 4 shows the comparison between no-load output voltages of the inverter with two modulating waves. In the elliptical wave PDPWM technique, the switching pulses are of increased width around the peak voltage. Output peak voltage is available for 8 ms as shown in Figure 4a compare to sine wave PDPWM technique wherein the peak output voltage is available for 6ms. The equations (3) to (6) shows the DC bus utilization in both cases [22]. This contributes to increased peak and rms value of the output voltage and current of CMLI in case of elliptical modulating wave. The reduction in the DC bus availability in elliptical wave for remaining time of the cycle contributes for increased current harmonics.

For sine modulating wave the output voltage,

$$V_s = \frac{1}{\pi}\left[\int_0^{2\pi/10} V_d + \int_{2\pi/10}^{8\pi/10} 2V_d + \int_{8\pi/10}^{\pi} V_d\right] \quad (3)$$

$$V_s = 1.6V_d \quad (4)$$

For elliptical modulating wave the output voltage,

$$V_E = \frac{1}{\pi}\left[\int_0^{\pi/10} V_d + \int_{\pi/10}^{9\pi/10} 2V_d + \int_{9\pi/10}^{\pi} V_d\right] \quad (5)$$

$$V_E = 1.8V_d \quad (6)$$

In present work, proposed elliptical PWM technique is applied to three-phase CMLI inverter and performance of the inverter has compared with traditional PDPWM technique. The simulation results and hardware results are compared in the further sections.

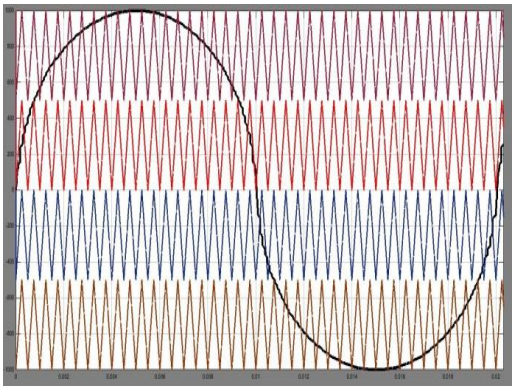


Figure 3. Switching Pulses from PDPWM Technique

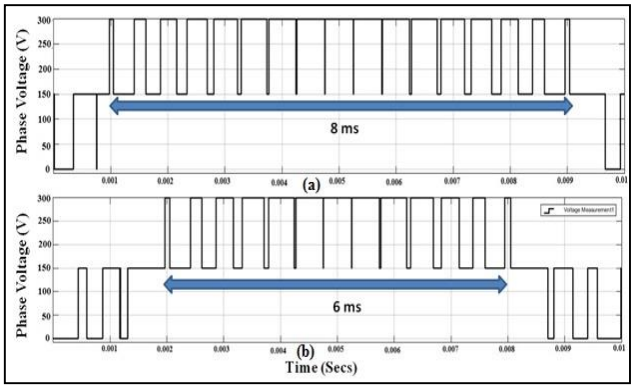



Figure 4. Comparison of Output Phase Voltages

## 3. SIMULATION RESULTS

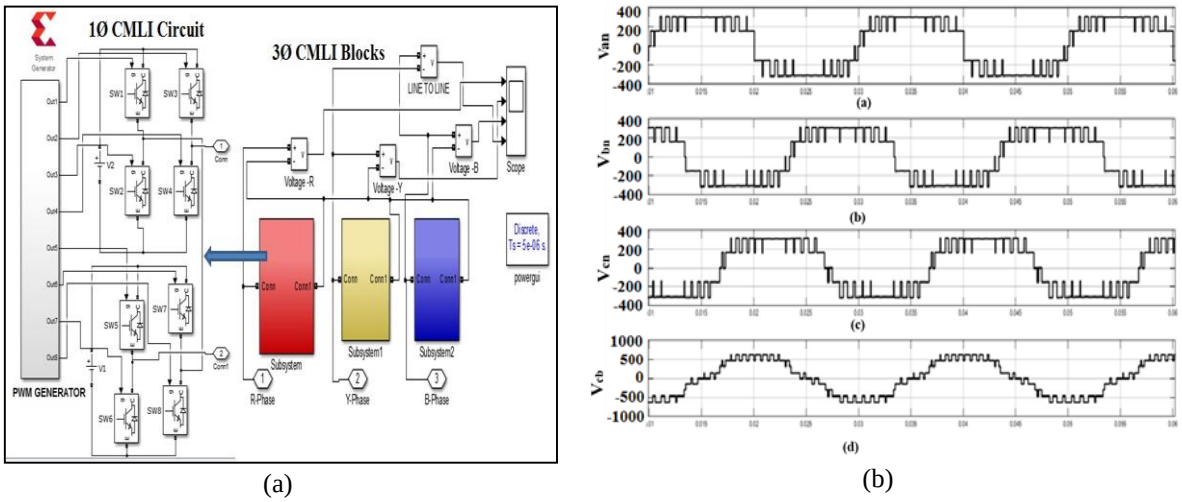
In order to verify the validity of the proposed modulation technique, a three-phase 5-level CMLI was built. For N level inverter, the number of output voltage levels of line voltage and phase voltage are given by $n_{line}$ and $n_{phase}$ respectively, given by equation (7) and (8). Where, 'm' is the number of cells in each phase of the cascaded inverter circuit.

$$n_{line} = (4m + 1) \quad (7)$$

$$n_{phase} = (2m + 1) \quad (8)$$

The PDPWM controller designed using XSG blocks is used to generate pulses for three-phase inverter with modulating wave having 120° phase shift of each. After the fault diagnosis and the performance analysis of the controller module, modifications are made according to design to meet requirements of three-phase inverters. After that the PWM pulse generated from the control strategy are given to three – phase 5-level CMLI. Fig. 5 show the three-phase CMLI implemented on XSG platform. Figure 5a shows circuit for single phase CMLI (red) and its PWM subsystem. Similarly another two phases which are 120° phase shift will constitute the three-phase CMLI. The input DC voltage of 150V is given to all six voltage sources in three-phase CMLI. The load resistance R= 400Ω and L= 40mH is connected in star across the output of CMLI. The output three-phase voltages and line voltage are measured across the load. The waveforms of phase and line voltages are shown in Figure 5b. The performance of the proposed PDPWM technique for modulation index ma = 0.8 are shown in Figure 6.

For a SPWM inverter with the DC link voltage of $V_{dc}$ the maximum output rms line voltage will be only 0.612* $V_{dc}$ [23]. Where in case of SVPWM, the maximum line voltage output of inverter will be 1.15* (0.6128 $V_{dc}$), hence there is an increase in the output by 15.47% [24]. Therefore, SPWM inverter is not able to meet rated voltage demand of load as met by SVPWM inverter for the same DC bus.




(a) (b)

Figure. 5 a) Simulation circuit of Three-phase 5-level cascaded inverter using XSG b) Output voltage of Three-phase 5-level inverter with 120° phase shift

From the simulation results it can be noticed that the output line voltage of inverter in case of 'sine' modulating wave is 364.5V at $m_a$=1, where as in case of 'elliptical' modulating wave the output line voltage of the inverter is 412.1V at $m_a$=1. From the proposed elliptical modulating wave, the output rms line voltage will be equal to 1.13 * (0.612* $V_{dc}$), which has resulted in 13% increase in the output voltage.The frequency spectrum of the output line voltage is shown in Fig. 6b. The output voltage and current in proposed PDPWM technique is increased with reduction in THD. The proposed PDPWM technique produces improved rms value of the inverter output voltage of 330V, when compared to traditional PDPWM technique which produces a voltage of 292V for modulation index of 0.8 with same circuit condition. And also %THD of the output voltage has reduced to 18.09% in the proposed PWM technique as compared to 21.87% in traditional PDPWM technique.

Table 1 shows the simulation results of three-phase 5-level CMLI with RL load for variation in the modulation index from 0.4 to1. The performances of proposed and traditional PDPWM techniques are compared for voltage and current and their respective %THD. Also the active powers in both cases were calculated from active power measurement from simulink library. From the simulation results it is clear that the proposed PWM method results in improved DC bus utilization to produce better output parameters compare to traditional SPWM technique.

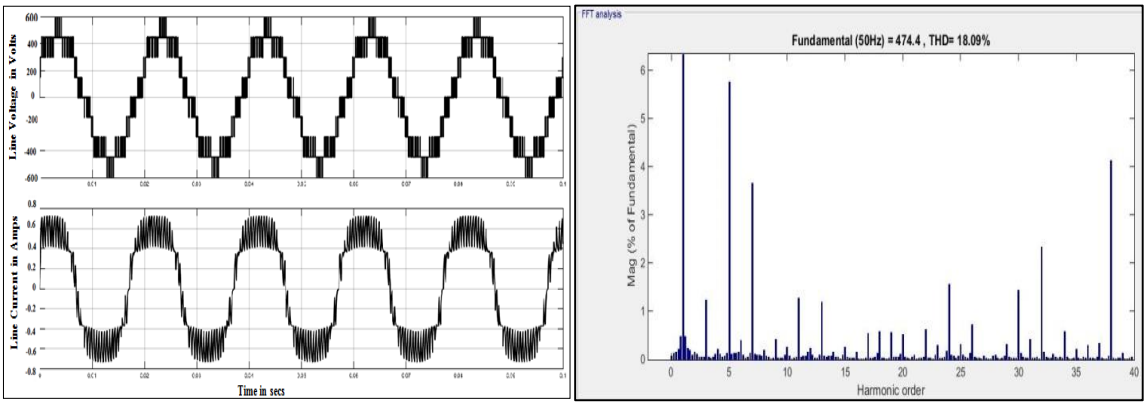
## 4. HARDWARE IMPLEMENTATION

For hardware implementation a three-phase 5-level inverter of Semikron make was used with RL -load connected in star fashion. The input to the inverter is from diode bridge rectifier with blocking voltage capacity of 1600V. DC capacitor bank connection for each inverter input source ensures the constant DC voltage. The photo of experimental set up is as shown in Figure 7. The H-Bridge of the each phase inverter consists of four V-IGBT=6, generation trench V-IGBT with CAL4, soft switching 4 generation CAL-diode. It has increased power cycling capability with integrated gate resistor and low switching losses at high di/dt. Gate driver controls the IGBTs dynamic behavior and its short circuit protection. Each driver drives two switches in a module. Snubber circuit of two capacitor of each 4700µF/450V is connected in series and a resistor of 2700Ω/20W across each capacitor for voltage balancing.

The digital control circuit Wavect is having Xilinx FPGA Zynq™-7000 SoC XC7Z020-CLG484-1with Dual ARM® Cortex™-A9 MPCore™ ,Which have capability Up to 667 MHz operation along with NEON™ Processing / FPU Engines. The memory allocation in the board is given by 512 MB DDR3 and 256 Mb Quad-SPI flash with full size. The Wavect digital board is having isolated voltage and current sensors four each for feedback from inverter circuit. It has AC/DC voltage and current measurement +/- 0-1000V and 0-25A respectively and output is instantaneous. The controller has dual, 200 KSPS-1MSPS 16 bit 4x2 channel Simultaneous sampling for ADC 15 V, 24 PWM out. Hence the kit supports three-phase, 5-level cascaded inverter with 8 switches per phase.

The Wavect software tool has 32 virtual input/output registers/ports for control and monitoring of digital controller signals. It has 32 digital probes which can capture and plot real time signals. Real time storage of data for post analysis makes the software reliable. The data stored can be analysed further for

parametric analysis. It has Gigabyte Ethernet Communication with the board for programming, controlling, monitoring and capturing at high data R/W rate.




(a) (b)

Figure. 6 (a) Output Voltage and Current waveform (b) THD and FFT window of three-phase cascaded multilevel inverter with RL load from simulation at $M_a$ = 0.8 for 'Ellipse'

Table 1 Simulation Results for RL Load

| | $M_a$ | $V_{ab}$ volts | %THD | $I_a$ amps | %THD | P watts |
|---|---|---|---|---|---|---|
| SINE WAVE | 1 | 364.9 | 17.22 | 0.525 | 14.25 | 146.4 |
| | 0.8 | 292 | 21.87 | 0.42 | 20.87 | 124.8 |
| | 0.6 | 218.9 | 25.8 | 0.315 | 22.14 | 90.46 |
| | 0.4 | 146 | 42.4 | 0.21 | 40.59 | 24.35 |
| ELLIPSE WAVE | 1 | 412.1 | 17.39 | 0.59 | 20.88 | 155.6 |
| | 0.8 | 330 | 18.09 | 0.476 | 25.85 | 132.7 |
| | 0.6 | 247.6 | 25.17 | 0.357 | 25.18 | 103 |
| | 0.4 | 165 | 40.55 | 0.238 | 40.4 | 25 |

The gate pulses generated with PDPWM technique from the Wavect controller are applied to the three-phase inverter with RL- load as shown in Fig. 7. The input to each phase of the inverter is 150V DC from diode rectifier. The resistance value of 400Ω and inductance of 40mH are connected in star connection as load. The carrier frequency was maintained at 2000Hz with modulating frequency of 50Hz.

The output line and phase voltages, phase currents are measured and displayed on the plot1 window in the system automatically from the Wavect tool. The voltage waveforms are captured for 1 second and stored for analysing total harmonic distortion in Simulink tool.

The output voltages, current and total harmonic distortion which are analysed from the stored data from the experiment were found to be closely matching with simulation results. The THD measured from the hardware implementation is less when compared to simulation results. Fig. 8 show the measured output voltage and current profile from experimental setup in the case of proposed PDPWM technique. The output line voltage of the proposed elliptical modulation technique has resulted in improved quality when compared to traditional PDPWM method. The rms value has increased drastically almost 30-40V without over modulation. This shows that the elliptical modulating for PDPWM technique is able to increase the inverter output rms line voltage by almost 13% compare to sine modulating wave. Fig. 9 shows the frequency spectrum of the proposed modulation technique for the output line voltage analysed from the captured data at modulation index of 0.8. The THD has reduced to 18.74% when compared to 21.65% in sine PDPWM technique. This shows that the proposed elliptical wave PDPWM technique is effective in improving quality of the line voltage of the three-phase inverter.

Figure 9 shows the active power, reactive power and apparent power are measured from the Wavect tool with $m_a$ = 0.8. There is an increase in the apparent and as well as active power delivered to load. This result is because of increased rms value of output voltage and current in this method. The power factor is also well maintained as in the case of traditional PDPWM technique. The performance of the proposed modulation technique is compared with traditional PWM technique and Fig. 10 shows the comparison graph of both modulation techniques. As the rms voltage and current increases the active power increase at the load side of the inverter which shows the proposed modulation technique's outstanding performance compared to

traditional PDPWM technique. There is an increase of almost 40-50W of active power in proposed PDPWM technique. If the load is operated with the modulation index between the ranges 0.4 to 0.9, then the performance of proposed PWM technique outstand the conventional method to improve the efficiency of the three-phase CMLI. This is achieved with tradeoff of increase in the current harmonics which can be further addressed by including proper filters at the output side of inverter.

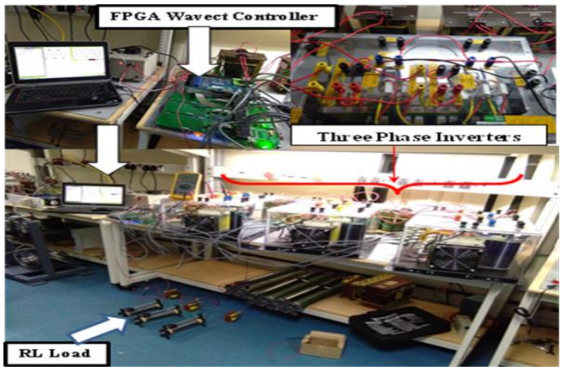



Figure 7. Hardware Setup of three-phase cascaded multilevel inverter with Semikron kit and WAVECT software

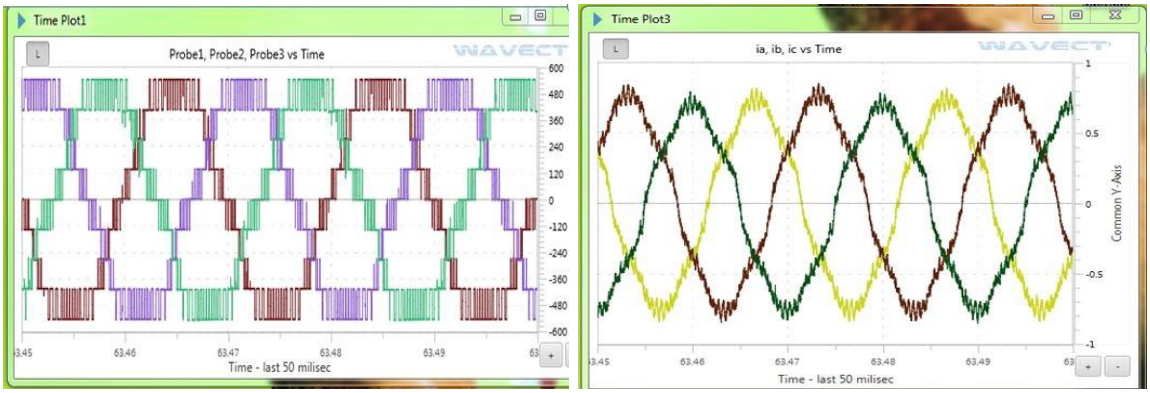



Figure 8. Output Voltage and Current waveform of three-phase 5-level cascaded inverter with RL load from experimental setup using WAVECT tool at $M_a$ = 0.8 for 'elliptical' PDPWM Technique

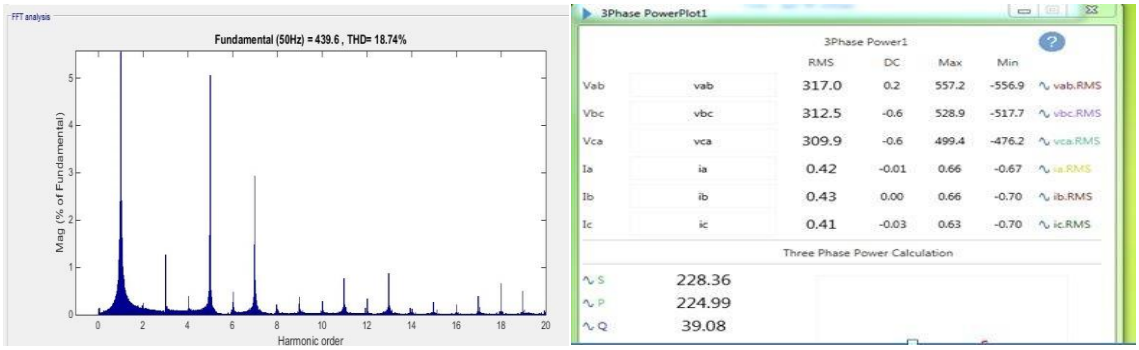
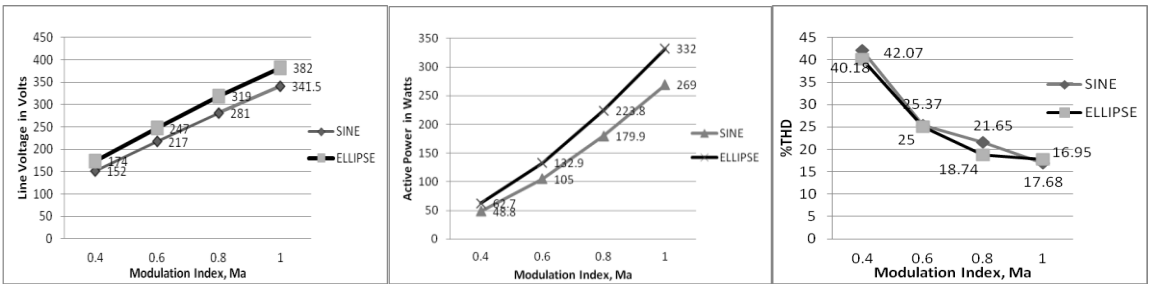



Figure 9. THD analysis of output voltage with RL load from experimental setup using WAVECT tool at $M_a$ = 0.8 for 'elliptical' PDPWM Technique.




(a) (b) (c)

Figure 10. Performance comparison of two PDPWM techniques for a) Line voltage Vs $M_a$ b) Active Power Vs $M_a$ and c) %THD Vs $M_a$

## 5. CONCLUSION

This paper proposes the elliptical wave as modulating wave for multicarrier PWM technique. The performance evaluation of three-phase 5-level CMLI inverter is carried out using MATLAB /SIMULINK XSG tool for both proposed and traditional PWM techniques. The simulation results were verified by hardware implementation of three-phase CMLI inverter with Semikron kit. Control strategy has been implemented using FPGA Wavect tool. The digital implementation of control strategy has resulted in reduced time and accurate results from the experimental setup.

The proposed modulation technique has resulted in improved performance of three-phase CMLI with respect to output rms voltage of 13%, active power of 23% and reduction of %THD. Hence the proposed PWM technique has been able to overcome the drawback of SPWM technique by increased DC bus utilization which improves the output voltage range. The proposed PWM technique can be used to drive inductive load where active power and power factor of the load plays key role.

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