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Experimental Prototype Model of IDVR for Bidirectional Voltage Compensation

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ABSTRACT

Interline Dynamic Voltage Restorer (IDVR) is an optimum solution to compensate voltage sag in multiple lines. The IDVR consisting of two or more DVRs connected to different feeders in a power system sharing a common DC link energy. This paper presents the hardware implementation of novel bidirectional voltage sag compensation by the IDVR in multiple feeders at same instance. A two line feeder power system with IDVR installed is considered. The IDVR is implemented using two VSI with filter. The control system of IDVR is developed using DSPACE.

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1. INTRODUCTION

The amount of sensitive loads added into the electrical power distribution system has escalated in recent years. Consequently the power quality plays a vital role in effective operation of sensitive loads. Most of the sensitive loads on the distribution side are electronic equipment. These electronic equipment loads are easily affected and have less tolerance towards the power quality problems. Hence the power quality problems are considered as the most significant problems on the distribution side of power systems. One of the major and frequently occurring power quality problems is voltage sag. Voltage sag is referred to as the drop in voltage magnitude from 10 to 90 percent of the nominal value, for a duration of half cycle to one minute [1]. The existing traditional methods for mitigation of voltage sag are replaced by the Flexible AC Transmission Systems (FACTS) devices to overcome the limitations of traditional methods like limited voltage capability and creating additional losses [2].

There are various FACTS devices incorporated on the transmission and distribution side of the power systems to eliminate different voltage and power distortions. Among the FACTS devices connected at the distribution side, Dynamic Voltage Restorer (DVR) has been utilized for the voltage sag mitigation. Though the functionality of DVR is to inject series voltage into the incoming three phase or single phase network, however, the injection of series voltage necessitates the injection of real and reactive power into the system. The real power injection is provided through the DC link supported by external energy source. The external energy source may be capacitor bank, battery, any DC source. Thus, when the duration of voltage sag occurrence is long or during multiple voltage sags, more amount of energy is required. Therefore in the event of long or deep voltage sags, DVR requires large external energy which is one of the drawbacks of the

DVR. Due to the increasing number of sensitive loads, almost every feeder on the distribution side has at least one sensitive load connected to it. Therefore, there will be conditions where more than one feeder needs to be compensated at one instance of time. Connecting one DVR to multiple feeders is not possible because the topology of DVR is designed for compensation of single feeder and connecting multiple DVRs to multiple feeders with external energy storage will be uneconomical. This is the second major constraint of DVR implementation. Hence these drawbacks of DVR can be accomplished with extended version of DVR known as Interline Dynamic Voltage Restorer (IDVR).

IDVR comprises of two or more DVRs connected to different distribution feeders sharing a common DC link. So, if one DVR functions in voltage compensation mode, the second DVR functions in power mode to provide the necessary energy to the DVR working in voltage compensation mode. The ability of IDVR to replenish the dc link power while compensating can reduce the size of the DC link required. Most of the research on this functionality of IDVR has been proposed in the literature [3]–[7].

Since several DVRs are connected to multiple feeders, the voltage compensation in multiple feeders can be performed with one device at one instance. This type of compensation is called as bidirectional compensation. This second major advantage of IDVR is covered in this paper. A two feeder IDVR system is considered and a voltage sag is created in the considered two feeders at same time. An extensive control algorithms are developed in both DVRs of IDVR for the voltage sag mitigation in the feeders. The bidirectional compensation technique of IDVR is analyzed with experimental results obtained from the laboratory prototype model of IDVR developed using DSPACE 1103. The following sections covers about the mathematical modelling of IDVR, control system of IDVR and experimental results which are obtained from the prototype model of IDVR.

2. MATHEMATICAL MODELLING OF IDVR

The schematic network layout of two line or two feeder IDVR is shown in Figure. 1. IDVR consists of two DVRs having a common DC link. The two DVRs of IDVR are connected to two different feeders with the aid of series injection transformers. The IDVR consists of a control system, a voltage source inverter and the filter. In Figure.1, V_{b1} and V_{b2} are the bus voltages of feeder 1 and feeder 2 respectively. The two loads, Load 1 and Load 2 are considered as the sensitive loads connected to feeder 1 and feeder 2 respectively. V_{l1} and V_{l2} are the load voltages of load 1 and load 2. When a sag occurs at say load 1, then the DVR 1 injects the voltages V_{inj1} to maintain the V_{l1} equal to V_{s1}

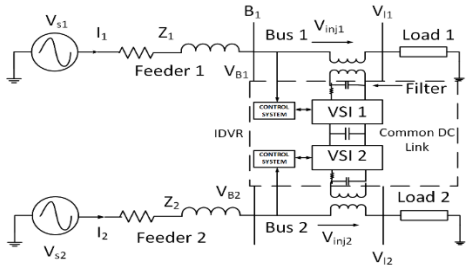

Figure 1. Schematic Layout of IDVR

2.1. Inverter Modelling

According to Figure. 1, the voltage sources of two feeders V_{s1} and V_{s2} are given the by equations 1 and 2 respectively.

$$V_{s1} = I_1 Z_1 + V_{inj1} + V_{l1} \quad (1)$$

$$V_{s2} = I_2 Z_2 + V_{inj2} + V_{l2} \quad (2)$$

(Note: $V_{inj} = V_{DVR}$)

Neglecting losses in the both feeders equations (1) and (2) can be written as

$$V_{inj1} = V_{s1} - V_{l1} \quad (3)$$

$$V_{inj2} = V_{s2} - V_{l2} \quad (4)$$

From equations (3) and (4), the voltage injected from the IDVR is difference of supply and load voltages of the feeder. Hence, the inverter voltage rating of IDVR can be determined if the amount of voltage sag that needs to be compensated by the IDVR is known.

Figure 2 represents the one line diagram of one of the feeder shown in Figure 1. According to equations (3) and (4) if $V_s = V_L$ then $V_{DVR} = 0$ which implies there is no need for compensation. The need for voltage compensation is only if $V_s \neq V_L$.

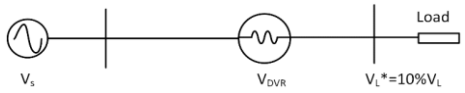

Figure 2. One line diagram of one of the feeder shown in Figure (1)

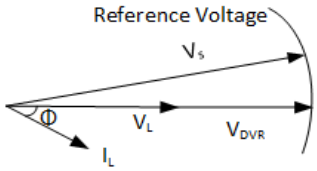

Figure 3. Phasor diagram of in phase method compensation

The voltage compensation by the IDVR will be initiated when

$$V_L^* < V_s \quad (5)$$

where $V_L^* = V_L - (0.10 * V_L)$

Therefore the V_{DVR} is given as

$$V_{DVR} = V_S - V_L^* \quad (6)$$

Hence the voltage rating of the two voltage source inverters shown in Figure. 1 can be determined by using equation (6).

The voltage rating of inverter can be determined by using equation (6) only when the in phase compensation method is considered [8].

The phasor diagram of the in phase compensation method is shown in Figure. 3.

In the in phase method of compensation, the voltage injected by the DVR is in phase with load (sagged) voltage. Figure.3 represents the phasor diagram of in phase compensation. The injected voltage V_{DVR} is in phase with load voltage. As shown in Figure. 3 the load current is having a phase difference with injected voltage, hence the DVR should inject active power along with reactive power to the load nearly at all times. In this paper, the voltage sag mitigation by the IDVR is performed using the in phase voltage compensation method. The reason for choosing the in phase methods over various voltage compensation methods is because the inverter rating with in phase compensation is less compared to the other methods like energy saving method, quadrature compensation method etc. [8]. From Figure. 3 the real power of the each DVR of IDVR is

$$P_{DVR} = V_{DVR} \times I_L^* \times \cos\phi \quad (7)$$

where

V_{DVR}: Voltage injected by the DVR

I_L: Load current

$\cos\phi$ = Power Factor

Therefore using equations (6) and (7) the power and voltage rating of the inverter of IDVR can be determined.

2.2. DC Link Capacitor Modelling

Designing the DC link of IDVR is very essential because the energy for IDVR to mitigate the voltage sag is supplied from the DC link. As the voltage source inverters are used as the building blocks of IDVR to mitigate the voltage sag, a capacitor is connected at the DC link of two DVRs of IDVR which is shown in Figure. 1.

The expression for the DC link power is given as

$$P_{DC} = P_{DVR1} + P_{DVR2} + P_{losses} \quad (8)$$

where P_{DVR1} and P_{DVR2} are power required by the two DVRs of IDVR for mitigating the voltage sag and P_{losses} is the losses in the DVR system.

Assume $P_{losses} = 0$ then

$$P_{DC} = P_{DVR1} + P_{DVR2} \quad (9)$$

Since a capacitance is used as the DC link, the DC link power P_{DC} can also be expressed as

$$P_{DC} = \Delta W_{DC} \div t \quad (10)$$

where ΔW_{DC} is the energy provided by the DC link capacitor. Whenever the IDVR compensates the voltage sag, the energy provided by the DC link link capacitor is expressed as

$$\Delta W_{DC} = \frac{1}{2} \times C \times (V_{DC\max}^2 - V_{DC\min}^2) \quad (11)$$

V_{DCmax}: DC link voltage
V_{DCmin}: Permissible DC link voltage (The maximum limit below which the DC link voltage should not decrease)
From equation (9) and (11) the DC link capacitance is given as

$$C = \frac{2 \times (P_{DVR1} + P_{DVR2})}{(V_{DC\max}^2 - V_{DC\min}^2) \times t} \quad (12)$$

The DC link voltage is

$$V_{DC\max} = \frac{3\sqrt{3}}{\prod} \times V_S \quad (13)$$

where V_s is source voltage of the feeder to which the IDVR is connected.
In equation (12) if the amount of voltage compensated by the two DVRs of IDVR is equal then $P_{DVR1} = P_{DVR2} = P$. The capacitance is given as

$$C = \frac{4 \times P}{(V_{DC\max}^2 - V_{DC\min}^2) \times t} \quad (14)$$

Hence using the proposed equations from (6) to (14) the rating of the IDVR can be determined. The proposed control system for IDVR is explained in the following section.

3. CONTROL SYSTEM OF IDVR

The major function of control system of IDVR is to detect the voltage sag in the line to which IDVR is connected and then to regulate the IDVR for proper voltage injection to mitigate the voltage sag. The control system designed in this paper is for a single phase IDVR system.

Figure 4 represents the block diagram of the control system of IDVR. The source voltage and load voltage are fed to the input of the control system. The following are working steps for algorithm in control system:

Step 1: The load voltage is given to a control block. The control block checks whether $V_L = V_L^*$, where V_L^* is obtained from equation (5).
Step 2: The reference and load voltages are computed with the following equations.

$$V_{ref}^* = \sqrt{\frac{1}{T}\int_{t-T}^{T} V_S(t)} \quad (15)$$

$$V_{L1}^* = \sqrt{\frac{1}{T}\int_{t-T}^{T} V_L^*(t)} \quad (16)$$

Where $T = \frac{1}{f}$, f is the fundamental frequency.
Step 3: The voltage error is calculated

$$V_{err} = V_{ref}^* - V_{L1}^* \quad (17)$$

Step 4: The error is fed to a proportional integral controller.
Step 5: The proportional Integral controller regulates the voltage error

$$V_{err}^* = V_{err} K_P + V_{err} \frac{K_i}{S} \quad (18)$$

Step 6: The regulated voltage error is given to the input of the PWM logic for generating the required gate pulses to the single phase inverter.

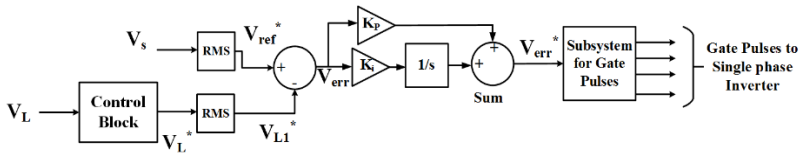

Figure 4. Control System of IDVR

Therefore, whenever a voltage sag is detected, the control system detects the sag and generates the required gate pulses to the inverter for the voltage injection. This control system is present in the building blocks of the DVRs of a considered IDVR. With the modelling equations and the control logic, a test system with IDVR is simulated. The experimental results obtained from laboratory prototype model of IDVR are explained in the next section paper.

4. EXPERIMENTAL RESULTS

A two line IDVR laboratory prototype model is shown in Figure 5. The prototype model is developed for experimental verification of bidirectional compensation of IDVR. The schematic layout of hardware set up is shown in Figure 6. The parameters of prototype model are given in Appendix I. Due to laboratory technical constraints the total experiment is performed in low voltage levels. A voltage source of 25V is fed to each feeder. The voltage source of each feeder is fed to a resistance of 90Ω. The loads of each feeder are rated to 100Ω. A double pole single throw switch is provided to add an additional load of 100Ω for both feeders so that the voltage sag is created in both feeders at same instance of time. The voltage source inverters shown in Figure 5 are PWM based voltage source inverters having insulated gate bipolar transistor (IGBT) switches. The LC filters are present to filter the harmonics in injected voltage and current present at the output of the voltage source inverter. The implementation of algorithms of control system of IDVR system are accomplished with DSPACE DS1103 control board.

Figure 7 and Figure 8 represents the load voltages of feeder 1 and feeder 2 in the absence of IDVR. Consider one feeder in the experimental set up in the absence of IDVR. The total resistance in feeder before switch is open is 190Ω. The current in the feeder 1 is 0.13A. Therefore, the load voltage of feeder is 13V (0.13A*100Ω) which can be observed in Figure 7. The second feeder voltage is also similar because the two feeders have same parameters ratings. The second feeder voltage is 13V which can be observed in Figure 8.

The load voltages of two feeders are dropped to 8V at 0.15S when switch is closed. After closing switch the total resistance in each feeder is 140Ω. Hence the current is 0.17A and the load voltage is 0.17*50= 8.9V. Hence a voltage sag is applied in both feeders at same time between 0.15s to 0.5 s. The load voltage in both feeders (Figure 7 and Figure 8) is observed to be restored to 13V, when switch is open. The set value of IDVR to initiate compensation is 20.7V (90% of VS=25V). The compensation algorithm starts to compensate as the load voltage observed is 13V and 8V during sag condition. .

In the presence of IDVR, the load voltages of both feeders are given in Figure 9 and Figure 10. Whenever the load voltage is less than the compensation limit, the control system of IDVR senses the voltage error and regulates the PWM logic to generate the gate signals to the voltage source inverter. The inverter injects the necessary voltage into the system so that the voltage sag is mitigated. As observed in Figure 9 and Figure 10, the load voltage in two feeders is maintained to 25V by the IDVR and the voltage sag between the intervals of 0.15 to 0. 5 seconds is compensated by the IDVR at same instance of time. Therefore the bidirectional voltage compensation with IDVR is verified with the experimental results.

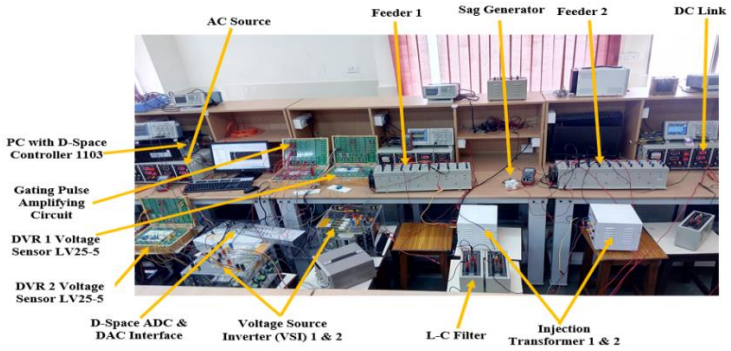

Figure 5. Laboraotry Protoype Model of IDVR

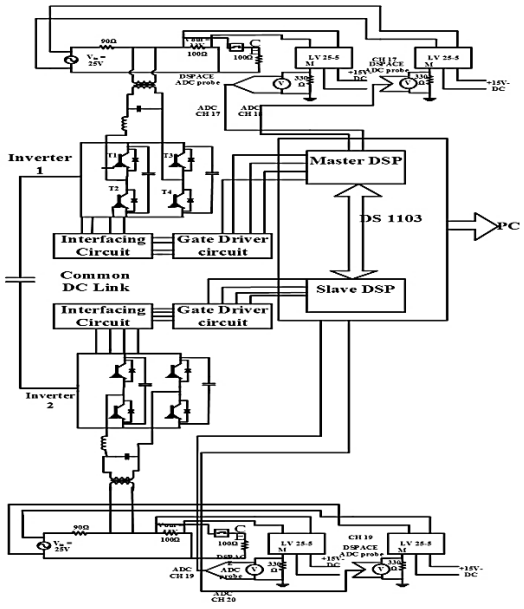

Figure 6. Schematic diagram of hardware prototype

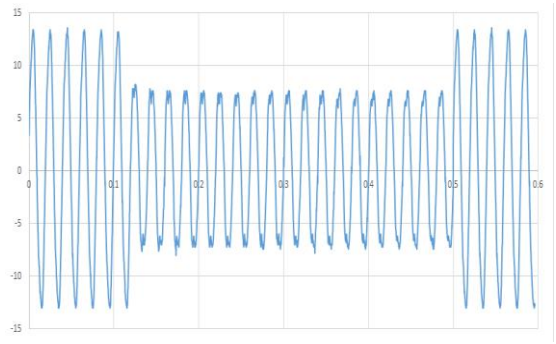

Figure 7. Load Voltage of Feeder 1 in the absence of IDVR

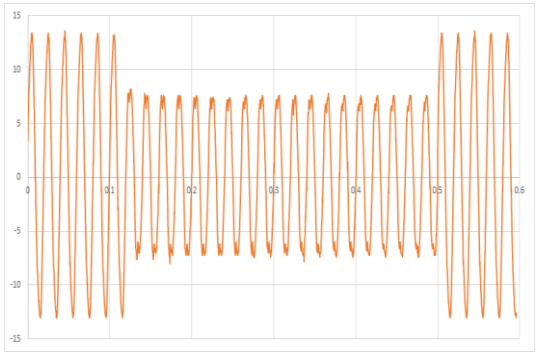

Figure 8. Load Voltage of Feeder 2 in the absence of IDVR

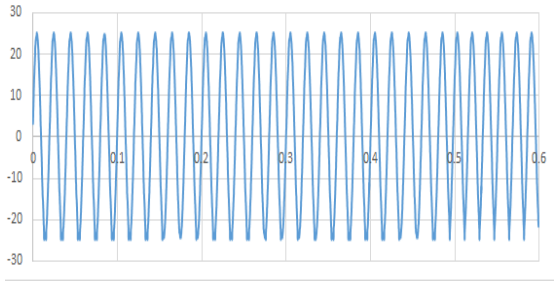

Figure 9. Load Voltage of Feeder 1 in the presence of IDVR

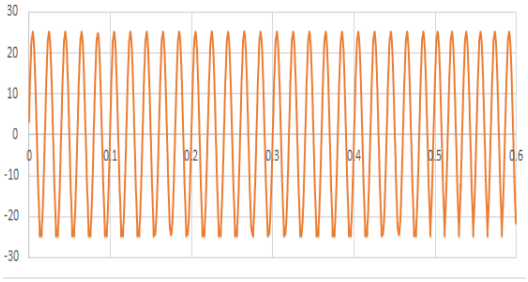

Figure 10. Load Voltage of Feeder 2 in the presence of IDVR

5. CONCLUSION

This paper proposes the concept of bidirectional compensation of IDVR. A test system comprising of a two feeder IDVR system is considered. The voltage sag is applied in two feeders at same instance and the effectiveness of IDVR in mitigating the voltage sag in both feeders at same instance is verified with experimental setup. The experimental results are obtained by developing a laboratory prototype model of IDVR. A control system for IDVR is developed for sensing the voltage error and regulating the IDVR to inject the required voltage for the mitigation of voltage sag. The experimental results have proven the efficient operation of IDVR in mitigating the voltage sag in two feeder topology at same instance. Hence IDVR can be utilized for multi-level feeder voltage compensation.

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APPENDIX I

• Voltage Source of two Feeders	1Φ, 25V, 50Hz
• Feeder Resistance of two Feeders	90Ω
• Load Resistance of two Feeders	100Ω
• DC link Voltage	50V
• DC link capacitor	500μF
• Ripple filter for DVR 1	R=5Ω, C=10μF
• Ripple Filter for DVR 2	R=5Ω, C=10μF
• Values of PI controller for two DVR1 and DVR 2	K_p= 0.2, K_i= 10
• PWM switching frequency	10KHz

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