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A Novel Single Phase bridgeless AC/DC PFC converter for Low Total Harmonics Distortion and High Power Factor

Santhi MaryAntony[1], Godwin Immanuel[2]
School Of Electrical And Electronics, Sathyabama University, Chennai, India

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ABSTRACT

Now day's the power factor has become a major problem in power system to improve the power quality of the grid, as power factor is affected on the grid due to the nonlinear loads connected to it. Single phase bridgeless AC/DC power factor correction (PFC) topology to improve the power factor as well as the total harmonic distortion (THD) of the utility grid is proposed. By removing the input bridge in conventional PFC converters, the control circuit is simplified; the total harmonics distortion (THD) and power factor (PF) are improved. The PI controller operates in two loops one is the outer control loop which calculates the reference current through LC filter and signal processing. Inner current loop generates PWM switching signals through the PI controller. The output of the proposed PFC topology is verified for prototype using MATLAB circuit simulations. The experimental system is developed, and the simulation results are obtained.

Corresponding Author:

Santhi MaryAntony,
School of Electrical and Electronics,
Sathyabama University Chennai, India.
Email: msanthimary@gmail.com

1. INTRODUCTION

The purpose of improving power quality of the AC system has become excessive interest from years ago. There is huge usage of power electronic devices, such as variable speed drives, uncontrolled rectifiers and other switching devices, these devices affects the power quality of the utility grid significantly .To decrease harmonics in transmission lines, the Research on active power factor correction (PFC) techniques has taken on an accelerated path typical PFC converter topologies are boost Buck- boost [8], buck and SEPIC [2-5].The boost converter is rarely used in practical applications, as the input current can be easily formed into a sinusoidal waveform to maintain unity power factor. However, the boost PFC converter [8] has a restricted capability since the peak value of the AC input voltage must be lesser than the DC output voltage. On the other hand, the DC output voltage of the buck PFC is lower than the peak of the AC input voltage, which reduces the cost and the rating of the component. A buck PFC converter [9-11] gives an alternative for low-voltage applications such as a 48V DC bus. The buck converter has high efficiency for entire input voltage range with distorted input current that comfortably crosses the limits imposed by IEC requirements.

A buck PFC AC/DC converter provides an alternative option for low-voltage applications [15]. Unlike in the boost chopper, the output voltage of the buck chopper is lower than the peak of the input ac voltage, and this significant feature allows the low voltage rating of switching devices to be used in the converter, which can significantly reduce the component cost [17]. On the one hand, depending on the application, a resonant converter can be excluded from the buck converter topology. The input current of the buck PFC converter has dead zones along the cycle, which requires extensive passive filtering to improve the power factor [16]. The conventional SEPIC converter can supply a high-power factor in wide range of voltage conditions [12-13]. The output voltage could be reduced or increased without the need of inversion with the SEPIC converters [14].

This introduces a new topology for single phase bridgeless AC/DC PFC converters. This used to reduce the THD and increasing PF of the operation. In Section1 Proposed SEPIC converter combines the bridge and DC-DC stages into one stage. Section2 analyses operation of the proposed SEPIC PFC converter. In Section3 component selection and control circuit design are presented. The simulation results of the conventional and proposed SEPIC converter are presented. Summary and future work is provided in it.

2. NEED FOR IMPROVING POWER FACTOR

Power factor is the ratio of Real power flowing to the load to the apparent power in the circuit. Ideal power factor is 1 and device consumes all the power it draws. The range of power factor is lies between to -1 to +1. The benefits of power factor correction is

i. To reduce losses
ii. To protect devices from high currents
iii. Power quality is improved
iv. Reduction of electricity bills

Power factor is dependent on load so vary according to the loads. Linear loads with lower power factor can be corrected with passive network of capacitors or inductors. Non-linear loads with lower power factor can destroy the current from the system. In such active or passive networks is used to avoid the distortion of current and by improving the power factor.

3. PROPOSED BRIDGELESS SEPIC PFC CONVERTER

Proposed SEPIC converter combines the bridge and DC-DC stages into one stage .We simplified the controller circuit by eliminating the input bridge in conventional PFC converters, the total harmonic distortion [THD] and power factor [PF] are improved. The proposed converter is able to reduce the THD 2.83% from5.72% and improve the power factor to 0.998.The proposed bridgeless SEPIC PFC converter topology provides much better performance than conventional SEPIC PFC converter. The proposed converter single phase bridgeless SEPIC PFC is better for lower power equipment especially those requiring high quality input power .The operation of the conventional SEPIC PFC converter circuit can be separated in to two modes depending on the position of the switches. When the switch Q_1 switched on, output diode D acts as reverse biased. The input inductor L1 gets charge, then output inductor L_2 and AC input capacitor C_1 creates a resonant circuit. Here, load draws current from the output capacitor C_0. During this time of operation, the voltage of the input inductor will be equal with the rectified AC voltage V_{ac}. Input capacitor voltage and output inductor voltage are also equal to V_{ac} during this first mode of operation. In the second mode, the Q1switch is turned off, then the diode D is forward biased and L_1, C_1, L_2 creates a loop. The load is directly connected to the inductors during in second mode, which will discharge them during the mode of operation Figure 1.

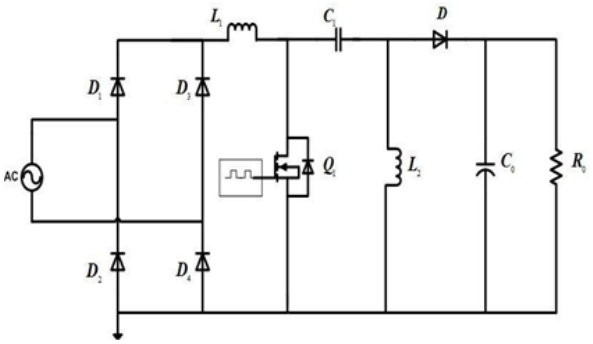


Figure 1. Conventional SEPIC PFC converter

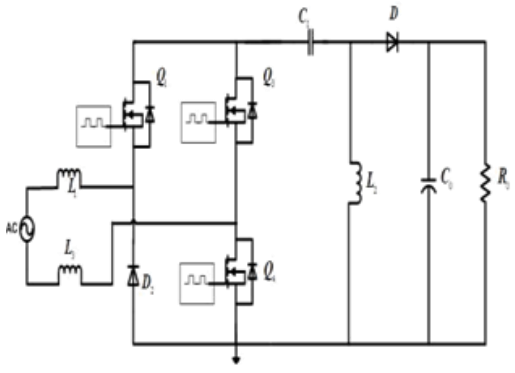


Figure 2. Proposed SEPIC PFC converter circuit

The proposed bridgeless SEPIC PFC converter bridge diode system replaced with three active switches which is shown in Figure 2. When all the switches such as $Q_{1,}$ Q_3 and Q_4 turn on, input inductor currents are linearly increasing. The output inductor voltage is equal to the capacitance voltage C_1 which was equal input voltage before all the switches are turned on. Thereby, $^{i}_{L2}$ reduces linearly. This mode ends by turning off $Q_{1,}$ Q_3 and $Q_{4.}$ By turning $Q_{1,}$ Q_3 and Q_4 off, Diode D starts to conduct. Then Input inductors current reduces linearly and output inductors current increases linearly until the diode current extinguishes. When D turns off, output side is detached from the input side, the current through the inductors freewheel at the input side. Working modes for proposed SEPIC PFC converter is provided.

4. PRINCIPLE OF OPERATION

Since the proposed SEPIC converter circuit consists of two symmetrical structures as shown in Fig. 3, this circuit is mainly used for the positive half cycle structure. Suggesting that the circuit working in a positive half cycle of a switching period Ts can be divided into three working modes and it can be defined as follows.

Mode 1. In this mode, Q1, Q3 and Q4 switches are turned on. In this mode of operation shown in fig. 1, the output inductor currents decreases and input inductor current increases linearly at a rate of proportional to the input voltage Vac.

Mode 2. In this mode, Q1, Q3 and Q4 switches are turned off, but Q1 and Q4 are conducting through anti parallel body diodes shown in fig.2. Then forward diode D is turned on, providing a path for the input and output inductor currents. In this mode, the input inductor currents are linearly decrease, at the rate of proportional to the output voltage V_{dc} and output inductor current linearly increase.

Mode 3. In this mode, all the active switches are turned off, as shown in below fig 5. Q1 and Q4 are conducting through anti parallel body diodes. This mode ends by the next switching cycle. In this mode, the inductors L1, L2 and L3 currents are equal. The switch voltage and diode voltage are equal input voltage V_{ac} and output voltage V_{dc} respectively.

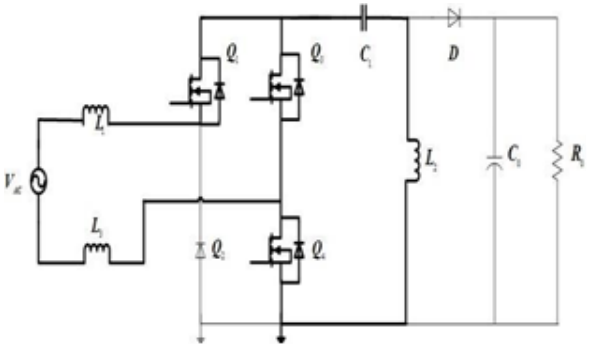


Figure 3. Circuit diagram for Mode 1

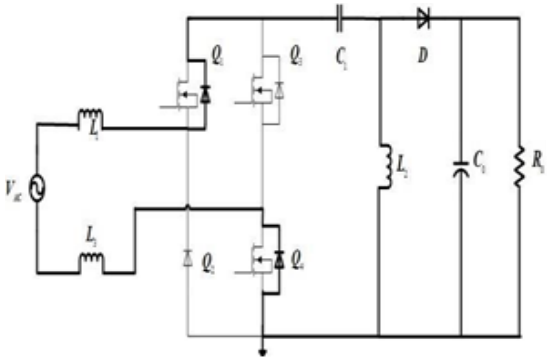


Figure 4. Circuit diagram for Mode 2

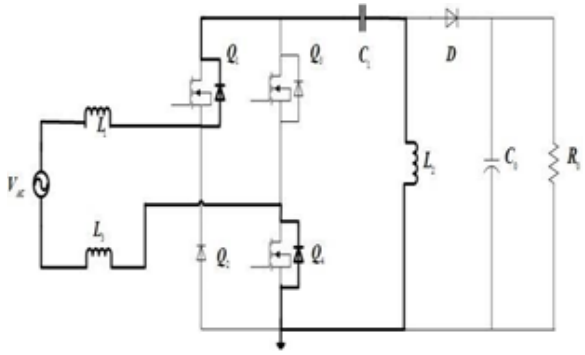
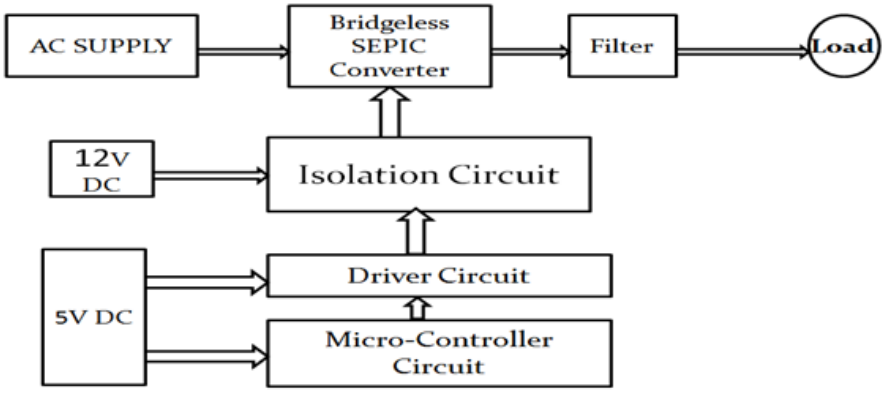


Figure 5. Circuit diagram for Mode3

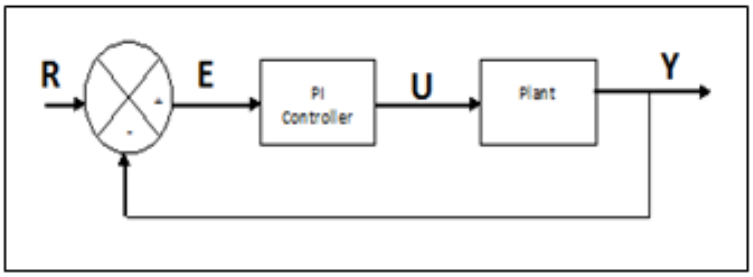
4.1 Block Diagram

The block diagram consists of power factor improvement unit based on microcontroller which consist of SEPIC PFC converter and PI controller. The input is in the form of AC. Bridgeless rectifier/Bridgeless SEPIC converter is used to convert AC to DC. The DC voltage is given to DC to DC converter; output of converter is fed to different types of load. The PI controller is used to calculate power factor by using phase difference between voltage and current. The DSPIC30F devices contain extensive Digital Signal Processor (DSP) functionality within a high performance 16-bit microcontroller (MCU) architecture. Device block diagrams for the dsPIC30F4011 and dsPIC30F4012 device.



4.2 Proportional Integral (PI) Control

The combination of proportional and integral terms is important to increase the speed of the response and to eliminate the steady state. The multi loop control is proposed for the converter, outer voltage controller generating the reference current to regulate the DC voltage and the inner PI controller generating the gating signals as shown in Figure 4. The high frequency switching of the converter produces switching ripples on the DC voltage. Thus, the measured DC voltage is processed through a band stop filter to eliminate the noise on the measurements.



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5. SIMULATION RESULTS

5.1 SEPIC PFC Converter Using Bridge Configuration

The Figure 6 represents the simulation for SEPIC PFC converter using bridge configuration. Here the input voltage is given through variable ac source as shown in Figure7. Boosting of the input voltage is done by the SEPIC converter which acts as a boost converter. The converter converts ac to dc and then used to run the load. Here we have used PWM technique to generate pulse. This pulse is given to the MOSFET switch in the converter side. Scope is connected to view the power factor and the total harmonic distortion. The output dc voltage and current respectively are shown in Figure 7.

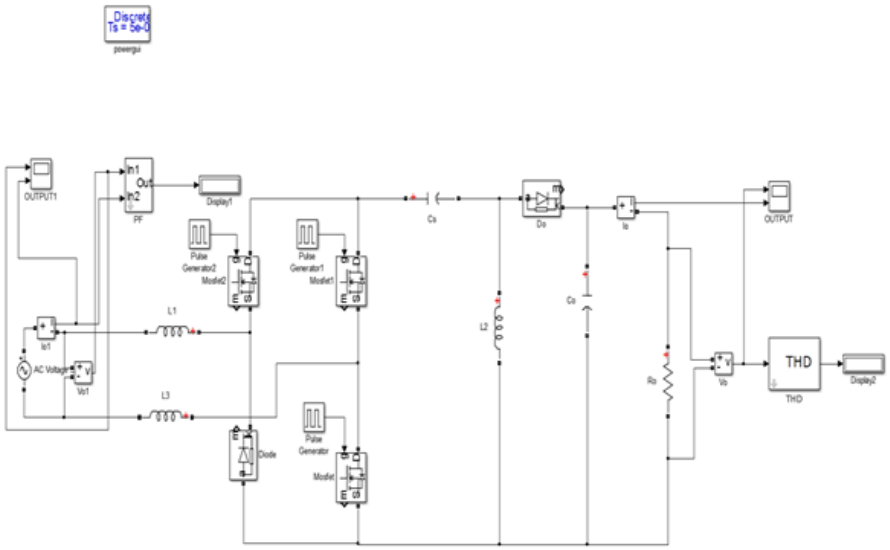

Figure 6. Simulation diagram for existing system

The proposed single phase bridgeless SEPIC topology is simulated by MATLAB based on the design. The presents the transient input voltage, input current, output voltage, output current for conventional SEPIC PFC converter.

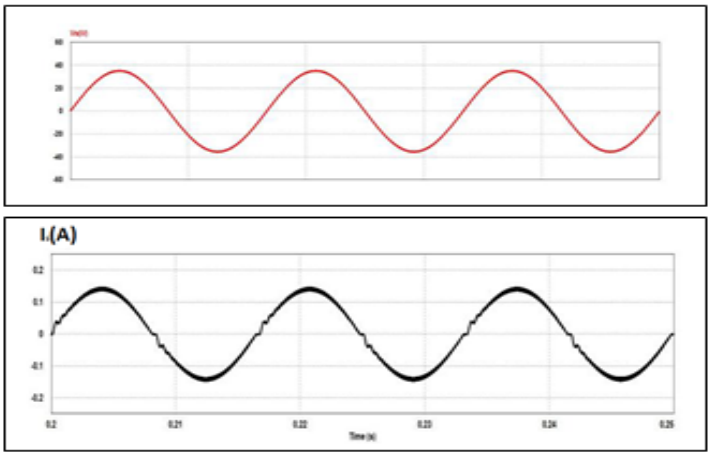

Figure 7. Input voltage and current waveforms

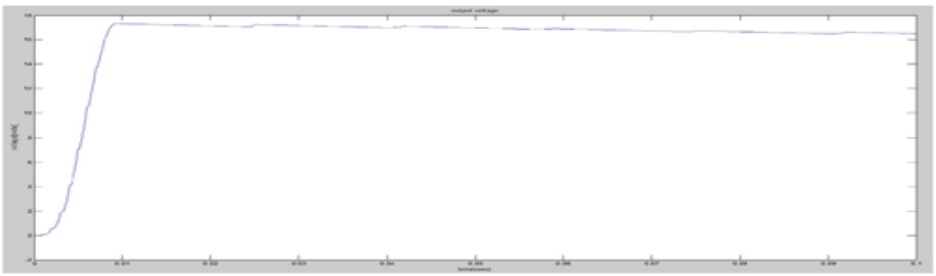

Figure 8. Output Voltage Waveforms for Conventional System

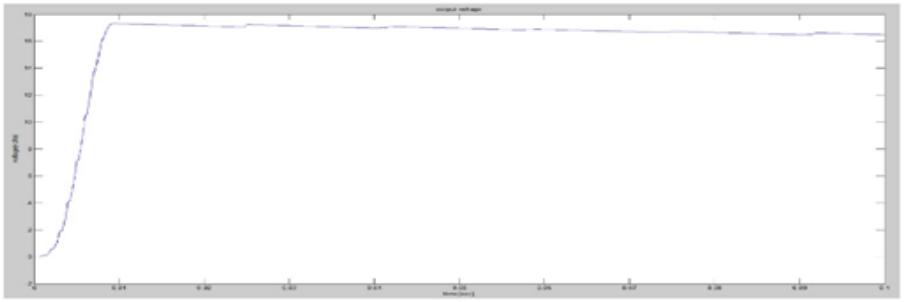

Figure 9. Output Current Waveforms for Conventional System

5.2 SEPIC PFC Converter Using Bridgeless Configuration

The Figure 10. represents simulation of SEPIC PFC converter with bridgeless configuration by removing input bridge. The four diodes are replaced with MOSFETS. The input voltage is given through variable ac source. Boosting of the input voltage is done by the SEPIC converter which acts as a boost converter. The converter converts ac to dc and then used to run the load. PWM technique is used to generate pulse. This pulse is given to the MOSFETS for switching purpose in the converter circuit. Scope is connected to view the power factor and the total harmonic distortion. The output voltage and current are shown in Figure 11.

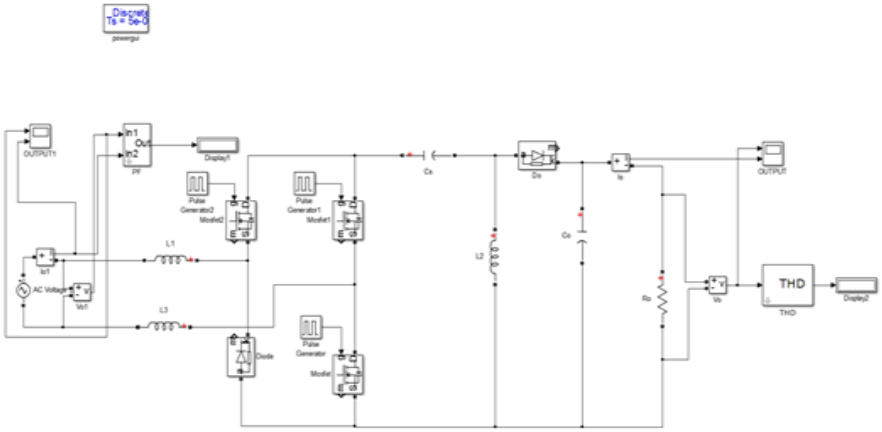

Figure 10. Simulation diagram for proposed system

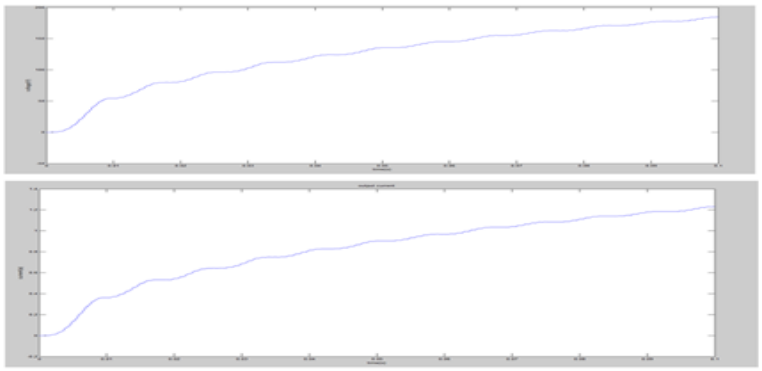

Figure 11. Waveforms of Output voltage and Output current

5.3 Comparsion of Power Factor and THD

Table .1 Comparison of PF and THD

	P.F	T.H.D	OUTPUT
Conventional	83.97%	2.9977	18volts
Proposed	98.83%	0.9944	150volts

Simulation results have been compared with the conventional sepic converter. It has obtained that the power factor correction for conventional sepic converter is 0.8397 with total harmonics distortion of 0.4677. In the proposed, bridgeless sepic converter, the power factor correction is 0.9888 with reduced total harmonics distortion of 0.1563.By comparing the conventional converter with the proposed converter, the proposed bridgeless sepic converter power factor is improved by 1.49% with reduced total harmonic distortion of 31.14%.

6. EXPERIMENTAL RESULTS

The experimental circuit of the proposed converter is developed. The experimental results of input voltage, input current and output voltage for conventional SEPIC PFC are shown in the Figure 9. For the input voltage of 24 Vrms. Output voltage of 10 Vrms and input current of 140mA, the THD is measured to be 15.63%, with power factor of 98.88%.

The experimental results of input voltage input current and output voltage for proposed SEPIC PFC of input voltage of 24Vrms, output voltage of 10Vrms, and the input current of 140 mA shown in fig.6, the THD is measured to be 15.837%, with power factor of .9. The output voltage ripples is obtained 0.15 V at 10 Vdc. The phase of input current is similar to the input voltage and the obtained PF is nearly unity shown in Figure 10.

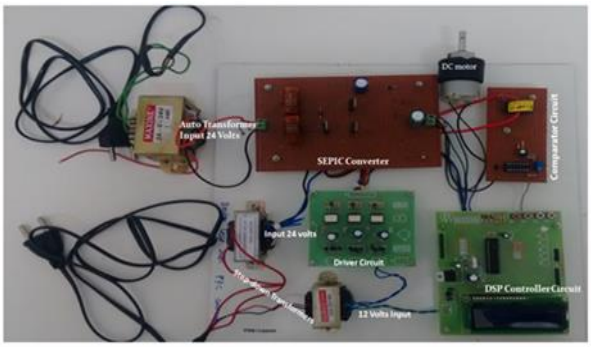

Figure 12. Experimental Prototype for Proposed Bridgeless SEPIC Converter

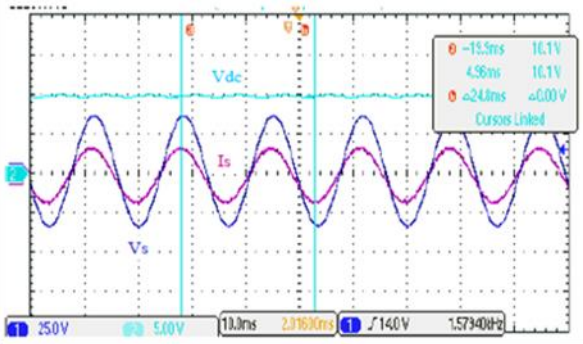

Figure 13. Proposed converter with Input voltage and Input current are in Phase

Theoritical Calculation for P.F and THD for Proposed Converter

Input Voltage (E) = 24 Volts
Input Current (I) = 60mA
Resistance (R0) = 145 Ω
Power Factor (P.F) = Real power(p) / Apparent Power(S)
Real Power (p) = E2/R
= (24)2/ 145
= 3.9 watts
Reactive Power (Q) = I*E
= 60*10-3*24

= 1.4 watts
Apparent Power (S) = sqrt (Q2+P2)
= sqrt [(1.4)2+(3.9)2]
= 4.01 watts
Power Factor(P.F) = P/S
= 3.9/4.01
= 0.9883
Therefore,
Power Factor (P.F) = 98.83%
To find THD:

THD = sqrt {[1/(P.F)2]-1}
= sqrt {[1/(0.9883)2]-1}
= 15.63%

7. CONCLUSION

A Novel Single Phase bridgeless AC/DC PFC converter topology is proposed, analysed and compared with the simulation to improve the power factor (PF) as well as Total Harmonic Distortion (THD) in grid applications. The full bridge consisting of diode in input is removed and replaced by bridgeless SEPIC converter. Topology are compared with conventional SEPIC converter, the proposed bridgeless SEPIC PFC topology provides much better performance than conventional SEPIC PFC converter. The topology is implemented on a converter operating from 25V AC input to generate into 10V DC. By this we can achieve high PF and low THD.

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