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Appropriate Switching State Selection to Avoid Capacitor Imbalance in Five-Level NPC

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ABSTRACT

An intrinsic problem with neutral point clamped (NPC) multilevel inverters (MLI) is unbalance of capacitor voltage. There are many mitigation techniques well established in the literature to balance the neutral point voltage for 3-level inverter. These techniques employ either Carrier based pulse width modulation (CBPWM), Space vector pulse width modulation (SVPWM) or hybrid of both the PWM techniques. Balancing becomes complicated as the level of the inverter increases due to addition of capacitor junctions. The imbalance in capacitor voltages may cause uneven voltage distribution among switching devices and sometimes may cause failure. It also increases harmonic content in its output waveform. This paper develops new modulation scheme for balancing capacitor voltages for 5level inverter .The scheme is a hybrid PWM which is a combination of both CBPWM and SVPWM techniques. As per this scheme CBPWM is applied to meet the load demand and at the zero crossings of the reference signal, CBPWM is blocked and for one carrier cycle. During this SVPWM is applied with appropriate switching state selection to neutralize the imbalance in capacitor voltage.

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1. INTRODUCTION

Now-a-days, multilevel converters are playing an important role in most of the medium and high power industrial and utility applications. This is because of their capability to operate at lower switching losses, reduction of electromagnetic interference, improved THD, less stress on the switches compared to two level converters. Among the wide varieties of multilevel converters, NPC MLI is widely chosen for many high power applications due to the following reasons

1) Static voltage equalization among switches.
2) Reduced dV/dt.
3) No dynamic voltage sharing problem.
4) Economics of the converter.

Despite of the above advantages, NPC MLI has an inherent drawback of unbalance in capacitor voltages at its DC side. Due to the difference in tolerance values of the capacitors and turn on-off times of the switches increases the unbalance to large extent making the converter operation undesirable [1]. A 3-level NPC converter consists of only two capacitors which make the control over the unbalance in capacitor voltages in a straight forward approach [8]. There exist many stabilization techniques in literature for three level clamped converters such as level shifted reference PWM, SVPWM techniques, in which control is done inherently without any use of external circuit [10]. But as the level of inverter increases capacitor junctions

increase which makes the control quite difficult. This unbalance of capacitor voltages leads to device failure and distorted voltage and current waveforms in the output. As a remedy to this usage of auxiliary dc/dc converters in the place of capacitors were proposed in [3].And techniques with back-back connection i.e. use an active rectifier as a front end to a multilevel inverter system in which both requires an external circuit[4]. Both these add to increased cost and complexity in control. This paper presents a novel control technique which provides inherent control over the saturation of capacitor voltages for a five level NPC converter without usage of any external circuit. The control scheme proposed is a hybrid of carrier based and SVPWM techniques with selection of appropriate switching states for stabilization of neutral point voltage [9]. Figure 1 describes the structure of five level diode clamped converter.

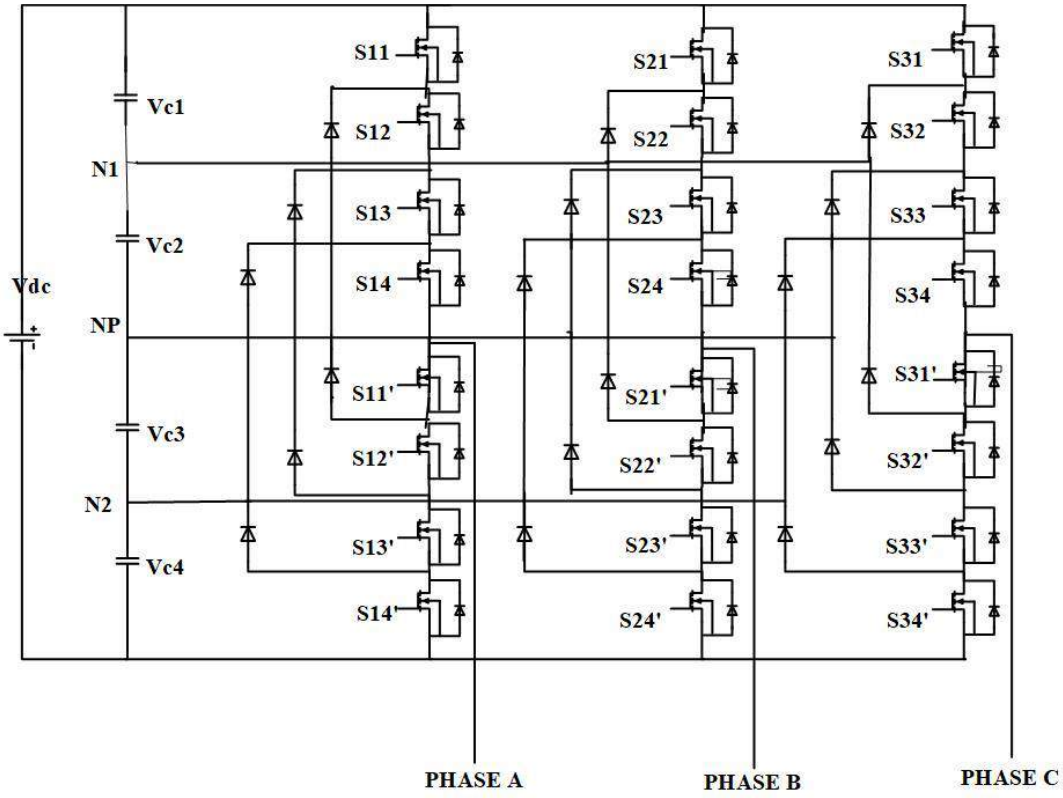


Figure 1. Five level DCMLI Topology

2. FIVE-LEVEL INVERTER

Figure 1 describes the structure of five level diode clamped converter. This converter topology employs clamped diodes that are responsible for equal voltage sharing among switches making them more reliable [2]. A 3-phase N level diode clamped inverter needs (N-1) capacitors, 3(N-1) (N-2) clamped diodes, 6(N-1) active switches. This paper deals with the five level NPC which consists of 4 capacitors forming 3 capacitor junctions [1]. The current through these capacitor junctions is responsible for unbalance in capacitor voltages making the inverter operation undesirable. It uses 36 clamped diodes and 24 active switches of same voltage sharing making it more economical compared to other converters. The following table provides the phase to neutral point voltages according to the switching positions. Figure 2 shows DC bus capacitors and their junction currents

Table 1. Switching table for five-level Inverter

S_1	S_2	S_3	S_4	V_{an}
1	1	1	1	V_{dc}
1	1	1	0	$3V_{dc}/4$
1	1	0	0	$V_{dc}/2$
1	0	0	0	$V_{dc}/4$

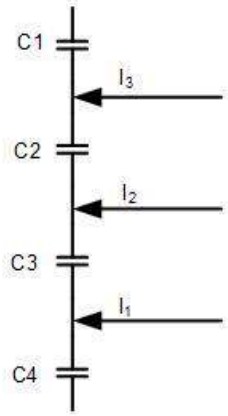


Figure 2. DC bus capacitors and their junction currents

As shown in Figure 2 I1,I2,I3 represents the average values of the currents entering the capacitor junctions.

3. BALANCING STRATEGY

The Underlining principle in maintaining balance of DC capacitor voltages is by making average capacitor junction currents zero. Figure 3 shows junction currents waveforms.

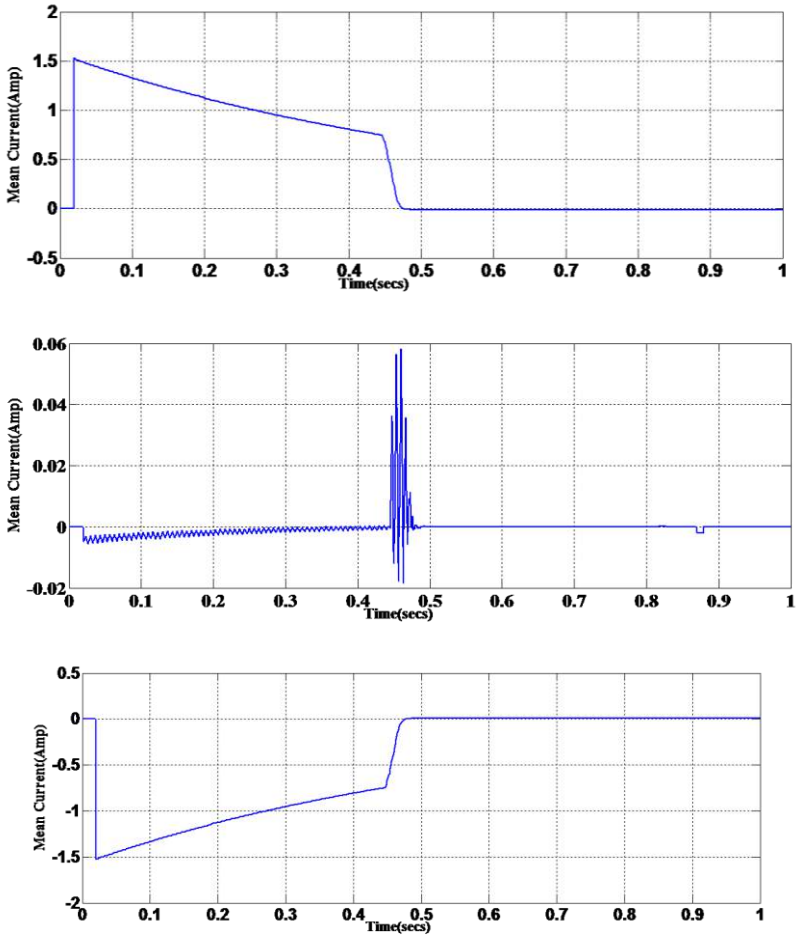


Figure 3. Junction currents waveforms

When the average currents of the capacitor junctions are maintained at zero, saturation of capacitor voltages can be avoided [7]. As shown in Figure 3 the average capacitor junction currents are non-zero when a conventional sine PWM technique (IPD) is applied to a 5-level clamped converter. The non-zero capacitor junction currents lead to saturation of capacitor voltages [2]. This in-turn reduces the level of inverterfrom five to three.

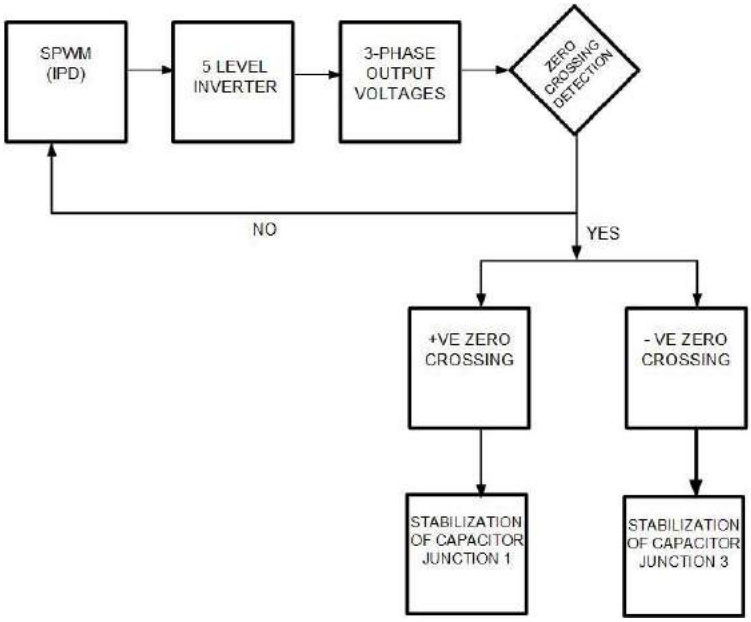


Figure 4. Flow chart of the proposed control logic

Table 2. Appropriate switching state selection

States	V_{c1}	V_{c2}	V_{c3}	V_{c4}
433	disch	ch	ch	ch
100	ch	ch	ch	disch
231	ch	ch	disch	ch
104	disch	disch	disch	ch
214	disch	disch	ch	ch
322	ch	disch	ch	ch

The block diagram of the proposed technique is shown in Figure.4 as per the novel modulation technique proposed carrier PWM is applied to meet the load demand and at zero crossings of the reference appropriate switching state is applied to balance the capacitor voltages. The appropriate switching state is selected based on capacitor voltage difference, the switching state is selected to discharge the overcharged capacitor and charge the undercharged capacitor. This is done with the help of suitable application of states shown in table from available 125 states, these states injects opposite current into each capacitor junction making the average current zero [6]. This controlling is done only at zero crossings of three phase output voltage for about 1carriercycle.The selection of control during zero crossings reduces distortion in output voltage [5]. Application of control technique other than zero crossing might increase the distortion in output. The stabilization of these capacitor junctions makes the neutral point balanced.

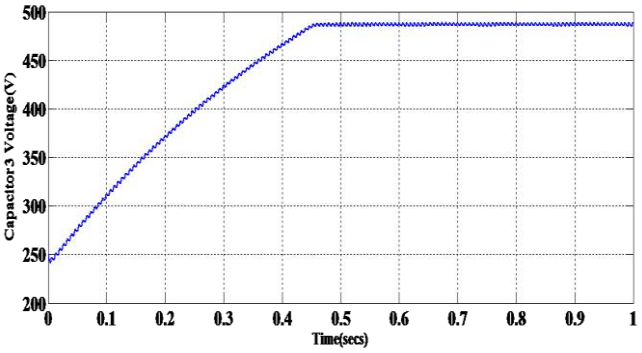
The control technique to avoid the saturation of capacitor voltages is done only during the zero crossings. For the time period other than zero crossings, a conventional carrier PWM (IPD) is applied.The balance of capacitor junction-1 is done during the positive zero crossings for about 1 carrier cycle. Similarly during the negative zero crossings junction 2 is balanced by injecting current of opposite polarity [3]. This makes the capacitors changing their behaviour i.e. charging to discharging or discharging to charging. The injection of current into capacitor junctions is done with the help of following states represented in the Table.3.

4. RESULTS AND ANALYSIS

To evaluate the proposed technique a 5-level NPC inverter supplied from a 1000V DC source supplying unity power factor load is taken. It has been supplied with conventional carrier PWM, proposed PWM technique and observations have been made.

4.1 Carrier based PWM (CBPWM)

This paper employs in-phase disposition with modulation index=1and frequency modulation ratio 21 to demonstrate the saturation of capacitor voltages. From Figure 5 it can be observed that the outer capacitors get overcharged to twice the intended voltage and the inner capacitors are discharged to zero voltage. Figure 6 shows the output phase voltages which approach three-level after the capacitors get saturated. Figure 7 shows the Fast Fourier transform of output waveform indicating its harmonic profile.



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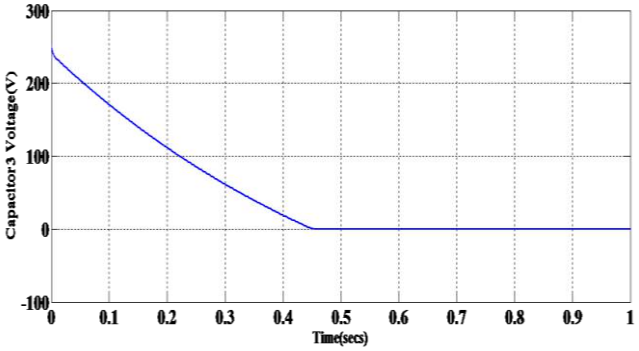

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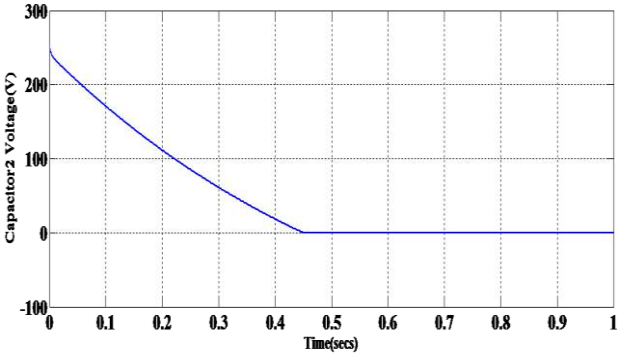

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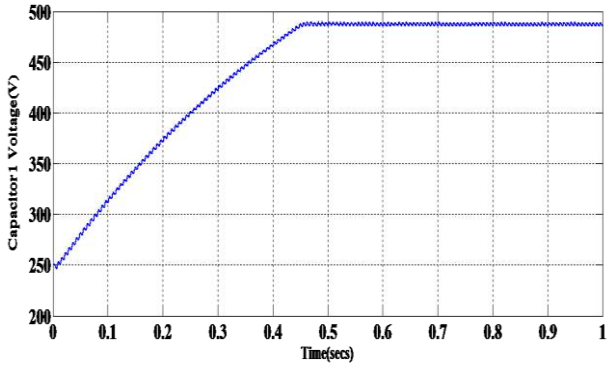


(d)

Figure 5 Capacitor voltages with conventional carrier PWM technique a) C1 b) C2 c) C3 d) C4

4.2. Proposed Control technique

The proposed control technique is applied by following the block diagram illustrated in Figure 4. The Figure 7 shows that the capacitors share the voltage equally and the unbalance in capacitor voltage can be avoided by employing the proposed technique.Figure 8 shows the output phase voltage, the five-levels in output can be observed with some distortion.Figure 9 shows the FFT of the output with proposed technique, It can be observed there is slight increase in THD. This increase in THD can be attributed to application of Space vector to neutralize the capacitor voltage difference.

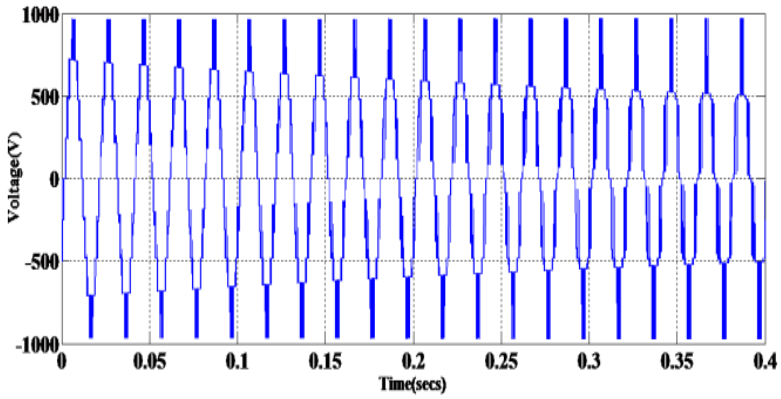
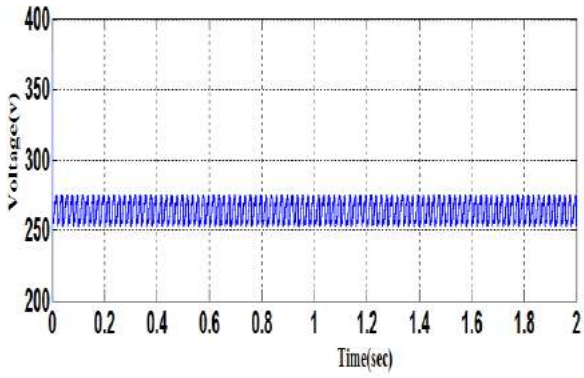


Figure 6 Output phase voltages



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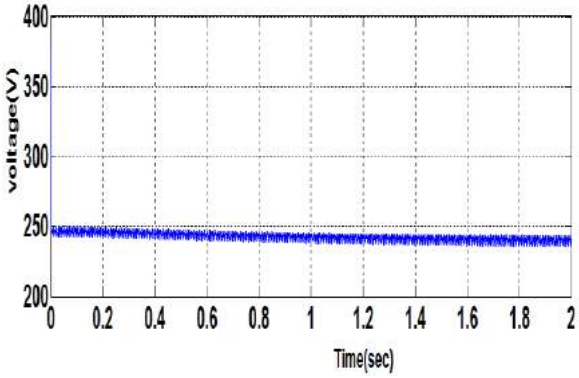

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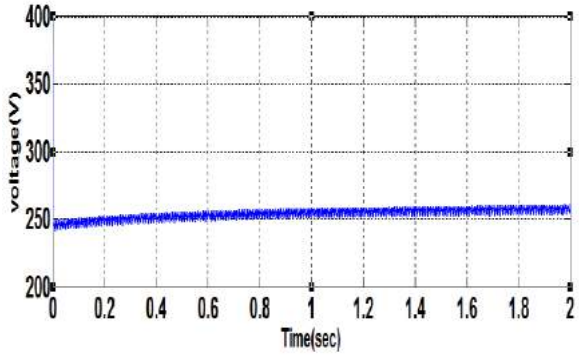

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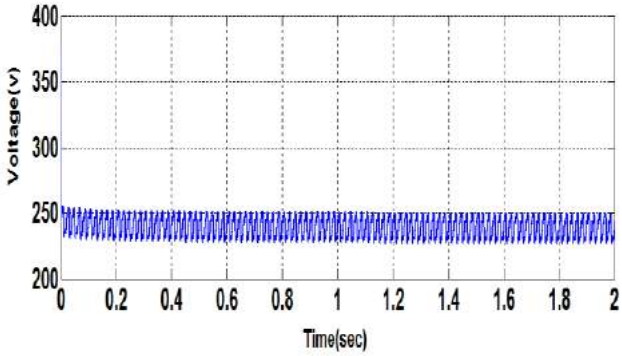

(d)

Figure 7 Capacitor voltages with proposed PWM technique a) C1 b) C2 c) C3 d) C4

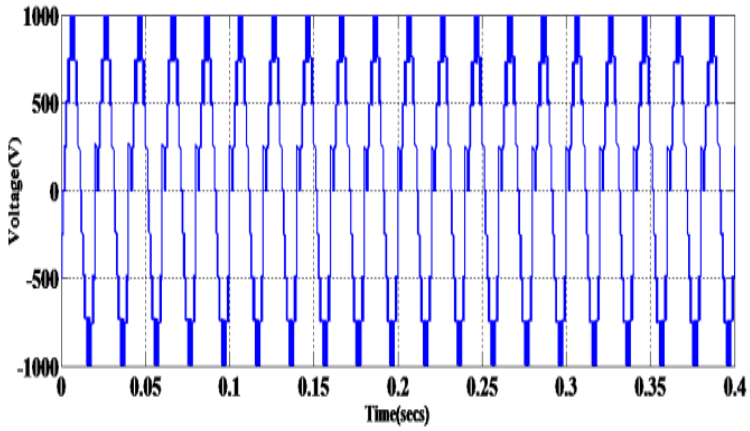

Figure 8 Output phase voltages

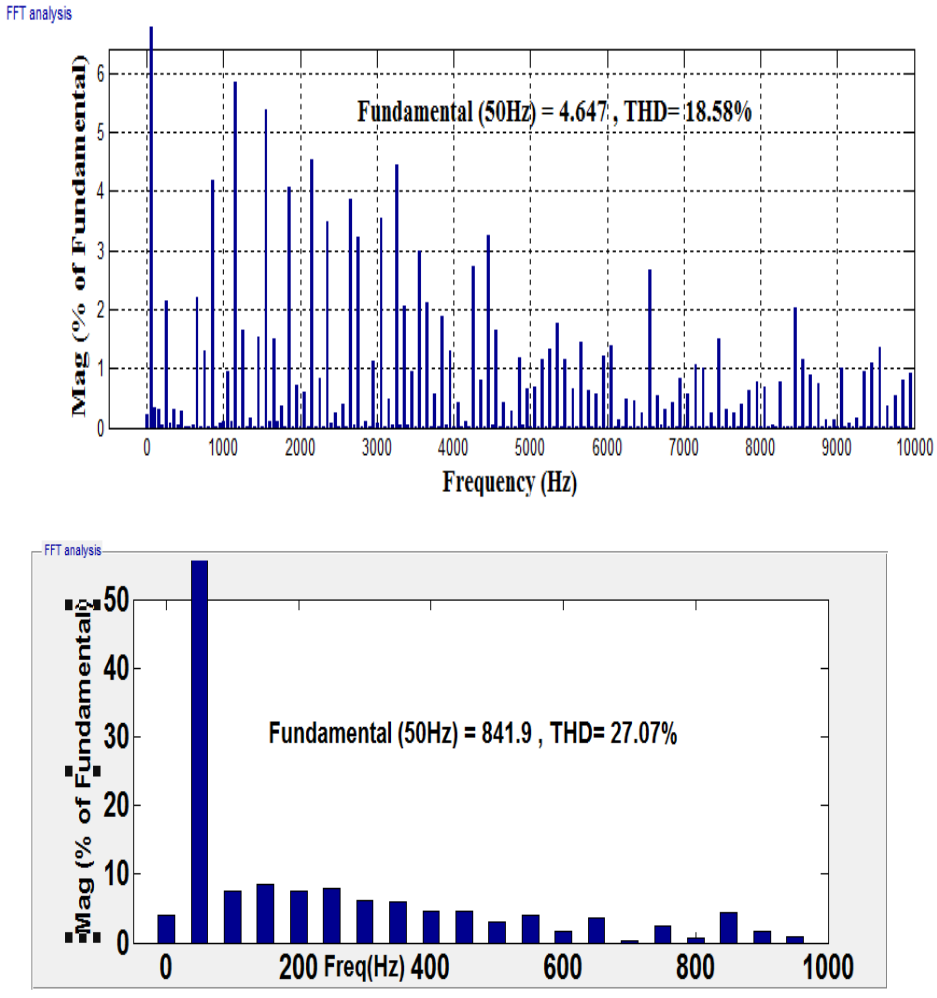

Figure 9 Output phase voltages THD with (a)Conventional CBPWM (b)Proposed PWM

5. CONCLUSION

Despite of many applications of Five-Level inverter in Medium and high power range, its usage is limited due to unbalance in capacitor voltages. Techniques were proposed in literature to solve this problem, but these techniques either used external circuitry like dc-dc converters in place or used front end converters. But there isn't a control technique which provides an inherent solution to this problem. This paper attempts to find a solution to this problem, a novel control technique to this problem for five-level inverter has been proposed. It can be observed from the results that the capacitor saturation problem is solved but with slight increase in THD.

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