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Space Vector Pulse Width Modulation Scheme for a Seven-Phase Voltage Source Inverter

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Abstract

This paper analyses a simple space vector PWM (SVPWM) scheme for a seven-phase voltage source inverter. At first the conventional method of producing sinusoidal output voltage by utilizing six active and a zero space vectors are used to synthesis the input reference and then new PWM scheme called time equivalent space vector PWM is presented. A comparison of the proposed scheme with the conventional scheme is presented based on various performance indices. Extensive Simulation results are provided to validate the findings.

Keywords: *space vector PWM, Time equivalent space vector PWM (TESVPWM), THD, seven-phase, VSI.*

1. Introduction

Speed controlled electric drives predominately utilise three-phase ac machines. However, since the variable speed ac drives require a power electronic converter interface, the number of machine phases may not be limited to three. This has led to an increase in the interest in multi-phase (more than three-phase) ac drive applications, especially in conjunction with traction, EV/HEVs and electric ship propulsion. Multi-phase machines offer some inherent advantages over their three-phase counterparts such as increase in the frequency of torque pulsation, reduction in the size of the machines, greater fault tolerance and reduction in power switch rating of converter etc.. Supply for a multi-phase variable speed drive is in the majority of cases provided by a Voltage Source Inverter (VSI).

There are two methods of controlling the output voltage and frequency of inverters namely: square wave mode and pulse width modulation mode. A number of PWM techniques are available to control a three-phase VSI [1]. However, Space Vector Pulse Width Modulation (SVPWM) has become the most popular one because of the easiness of digital implementation and better DC bus utilisation, when compared to the ramp-comparison sinusoidal PWM method. SVPWM for three-phase voltage source inverter has been extensively discussed in the literature [1]. . SVPWM for a five-phase inverter is taken up in [2-9] and SVPWM for six-phase inverters are elaborated in [10-13]. Seven-phase inverter for a seven-phase brushless dc motor is illustrated in [14] and space vector PWM to generate sinusoidal output is elaborated in [15-16]. More than seven-phase for instance nine-phase [17] and twelve phase [18] inverters are also available in the literature. In principle, there is a lot of flexibility available in choosing the proper space vector combination for an effective control of multi-phase VSIs because of a large number of space vectors.

This paper analyses SVPWM technique to provide variable voltage and frequency output from a seven-phase VSI. Modelling of a seven-phase VSI is reviewed in terms of space vector representation. The model obtained is decomposed into six two dimensional orthogonal space. The switching combinations yield 128 space vectors spanning over fourteen sectors. The six active vector application (conventional) yields sinusoidal output voltages A new scheme is proposed in this paper termed as Time Equivalent Space Vector PWM. In this scheme the gating time of each power switch is obtained by using reference voltage magnitude only. The complex implementation of conventional SVPWM is thus avoided. The analysis is done in terms of quality of output voltages and the implementation approach. A comparison is done for the conventional scheme and proposed TESVPWM scheme. Simulation results are provided to support the analytical and theoretical findings.

2. Modelling of a Seven-Phase VSI

Power circuit topology of a seven-phase VSI is shown in Fig. 1. Each switch in the circuit consists of two power semiconductor devices, connected in anti-parallel. One of these is a fully controllable semiconductor, such as a bipolar transistor or IGBT, while the second one is a diode. The input of the inverter is a dc voltage, which is regarded further on as being constant. The inverter outputs are denoted in Fig. 1 with lower case symbols (*a,b,c,d,e,f,g*) while the points of connection of the outputs to inverter legs have symbols in capital letters (*A,B,C,D,E,F,G*). A complete space vector model of a seven-phase VSI is reported in [19]. A brief review is presented here. The total number of space vectors available in a seven-phase VSI is 2^7=128. Out of these 128 space voltage vectors, 126 are active and two are zero space vectors and they form nine concentric polygons of fourteen sides in d-q plane with zero space vectors at the origin as shown in Fig-2.

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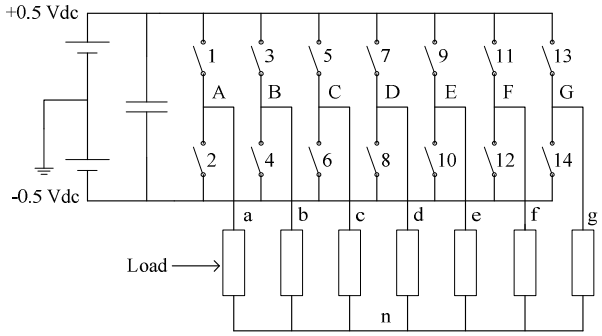


Figure 1. Seven-phase voltage source inverter power circuit

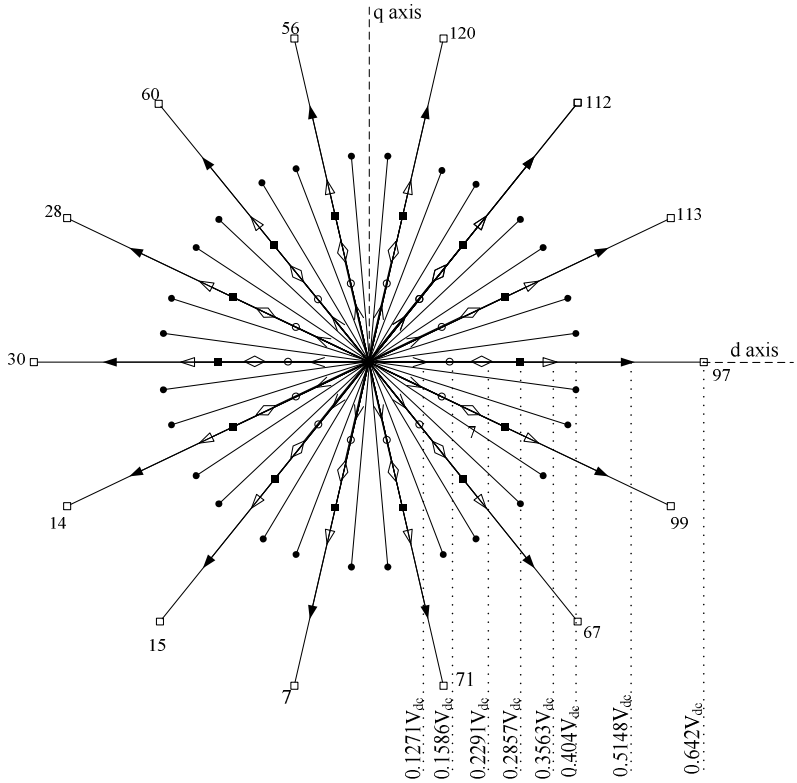


Figure 2. Phase-to-neutral voltage space vectors for states 1-128 (states127-128 are at origin) in *d-q* plane

However, since a seven-phase system is under consideration, one has to represent the inverter space vectors in a seven-dimensional space. Such a space can be decomposed into three two-dimensional sub-spaces (*d-q*, x_1-y_1 and x_2-y_2) and one single-dimensional sub-space (zero-sequence). Since the load is assumed to be star-connected with isolated neutral point, zero-sequence cannot be excited and it is therefore sufficient to consider only three two-dimensional sub-spaces, *d-q*, x_1-y_1 and x_2-y_2. Inverter voltage space vector in *d-q* sub-space is given with [20],

$$\underline{v}_{dq}=(2/7)\left(v_a+av_b+a^2v_c+a^3v_d+a^{*3}v_e+a^{*2}v_f+a^{*}v_g\right) \tag{1}$$

where $a=e^{j2\pi/7}$, $a^2=e^{j4\pi/7}$, $a^3=e^{j6\pi/7}$ and * stands for a complex conjugate. On the basis of the general decoupling transformation matrix for an *n*-phase system, inverter voltage space vectors in the second two-dimensional sub-space (x_1-y_1) and the third two-dimensional sub-space (x_2-y_2) are determined with,

$$\begin{aligned}\underline{v}_{x1y1}&=(2/7)\left(v_a+a^2v_b+a^4v_c+a^6v_d+av_e+a^3v_f+a^5v_g\right)\\ \underline{v}_{x2y2}&=(2/7)\left(v_a+a^3v_b+a^6v_c+a^2v_d+a^5v_e+av_f+a^4v_g\right)\end{aligned} \tag{2}$$

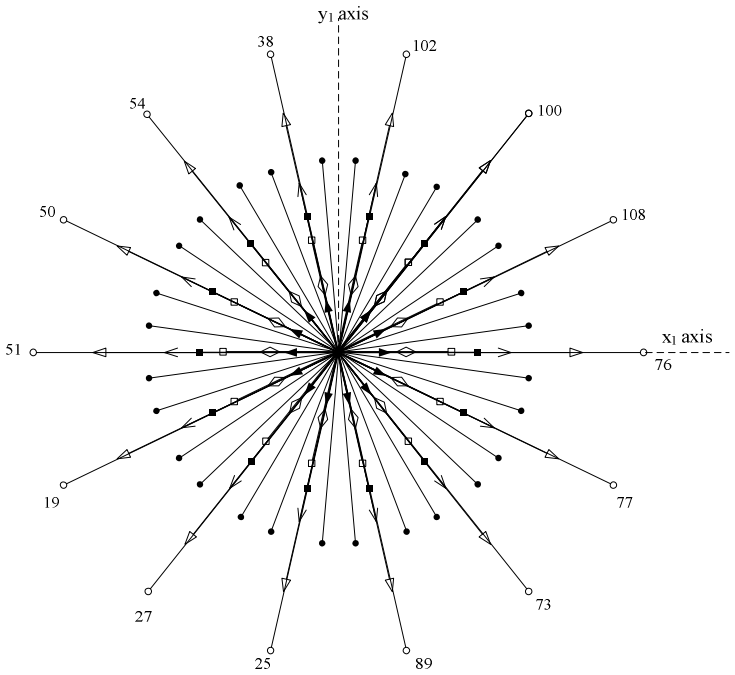


Figure 3. Phase-to-neutral voltage space vectors for states 1-128 (states127-128 are at origin) in x_1-y_1 plane

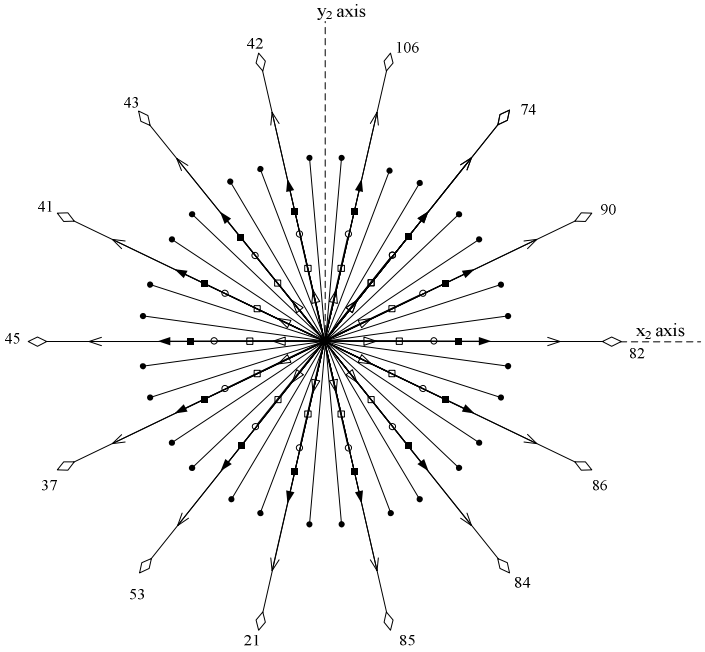


Figure 4. Phase-to-neutral voltage space vectors for states 1-128 (states127-128 are at origin) in x_2-y_2 plane

The zero-sequence component is identically equal to zero because of the assumption of isolated neutral point. The phase voltage space vectors in two orthogonal planes, obtained using (1), are shown in Figs. 3 & 4. It can be seen from Figs. 2, 3 and 4 , the vector mapping in d-q axis, x1-y1 axis and x2-y2 axis. There are in total fourteen distinct sectors with 25.714286° (π/7 radians) spacing. The inner-most space vectors in *d-q* plane are redundant and are therefore omitted from further discussion. This is in full compliance with observation of [17], where it is stated that only subset with maximum length vectors have to be used for any given combination of the switches that are 'on' and 'off' (3-4 and 4-3 in this case). The middle region space vectors correspond to two switches being 'on' from upper (lower) set and five switches being 'off' from lower (upper) set or vice-versa and one switch being 'on' from upper (lower) set and six switches being 'off' from lower (upper) set or vice-versa. In what follows, the vectors belonging to the middle region are simply termed medium and small vectors, while the vectors of the outer-most region are called large vectors.

Table 1 - magnitude and phase angle of vectors in *d-q*, x_1-y_1 and x_2-y_2 axis

Decimal Value	Binary Equiv.	d-q axis		x_1-y_1 axis		x_2-y_2 axis	
		Magnitude (p.u.)	Angle (degree)	Magnitude (p.u.)	Angle (degree)	Magnitude (p.u.)	Angle (degree)
0	0000000	0	0	0	0	0	0
1	0000001	0.2857	-51.4286	0.2857	-102.857	0.2857	-154.286
2	0000010	0.2857	-102.857	0.2857	154.2857	0.2857	51.4286
3	0000011	0.5148	-77.1429	0.3563	-154.286	0.1271	128.5714
4	0000100	0.2857	-154.286	0.2857	51.4286	0.2857	-102.857
5	0000101	0.3563	-102.857	0.1271	-25.7143	0.5148	-128.571
6	0000110	0.5148	-128.571	0.3563	102.8571	0.1271	-25.7143
7	0000111	0.642	-102.857	0.1586	154.2857	0.2291	-128.571
8	0001000	0.2857	154.2857	0.2857	-51.4286	0.2857	102.8571
9	0001001	0.1271	-128.571	0.5148	-77.1429	0.3563	154.2857
10	0001010	0.3563	-154.286	0.1271	-128.571	0.5148	77.1429
11	0001011	0.404	-110.705	0.404	-110.705	0.404	110.7048
12	0001100	0.5148	180	0.3563	0	0.1271	180
13	0001101	0.404	-146.438	0.404	-43.5809	0.404	-162.133
14	0001110	0.642	-154.286	0.1586	51.4286	0.2291	77.1429
15	0001111	0.642	-128.571	0.1586	-77.1429	0.2291	154.2857
16	0010000	0.2857	102.8571	0.2857	-154.286	0.2857	-51.4286
17	0010001	0.1271	25.7143	0.5148	-128.571	0.3563	-102.857
18	0010010	0.1271	-180	0.5148	180	0.3563	0
19	0010011	0.2291	-77.1429	0.642	-154.286	0.1586	-51.4286
20	0010100	0.3563	154.2857	0.1271	128.5714	0.5148	-77.1429
21	0010101	0.1586	-154.286	0.2291	-128.571	0.642	-102.857
22	0010110	0.404	-162.133	0.404	146.438	0.404	-43.5809
23	0010111	0.404	-120.724	0.404	-172.152	0.404	-84.9905
24	0011000	0.5148	128.5714	0.3563	-102.857	0.1271	25.7143
25	0011001	0.2291	128.5714	0.642	-102.857	0.1586	-154.286
26	0011010	0.404	162.1334	0.404	-146.438	0.404	43.5809
27	0011011	0.2291	-154.286	0.642	-128.571	0.1586	77.1429
28	0011100	0.642	154.2857	0.1586	-51.4286	0.2291	-77.1429
29	0011101	0.404	172.1523	0.404	-84.9905	0.404	-120.724
30	0011110	0.642	180	0.1586	180	0.2291	0
31	0011111	0.5148	-154.286	0.3563	-128.571	0.1271	-102.857
32	0100000	0.2857	51.4286	0.2857	102.8571	0.2857	154.2857
33	0100001	0.3563	0	0.1271	180	0.5148	180
34	0100010	0.1271	-25.7143	0.5148	128.5714	0.3563	102.8571
35	0100011	0.404	-43.5809	0.404	162.1334	0.404	146.438
36	0100100	0.1271	128.5714	0.5148	77.1429	0.3563	-154.286
37	0100101	0.1586	-51.4286	0.2291	77.1429	0.642	-154.286
38	0100110	0.2291	-128.571	0.642	102.8571	0.1586	154.2857
39	0100111	0.404	-84.9905	0.404	120.7238	0.404	-172.152
40	0101000	0.3563	102.8571	0.1271	25.7143	0.5148	128.5714
41	0101001	0.1586	51.4286	0.2291	-77.1429	0.642	154.2857
42	0101010	0.1586	154.2857	0.2291	128.5714	0.642	102.8571
43	0101011	0.1586	-77.1429	0.2291	-154.286	0.642	128.5714

44	0101100	0.404	146.438	0.404	43.5809	0.404	162.1334
45	0101101	0.1586	180	0.2291	0	0.642	180
46	0101110	0.404	-172.152	0.404	84.9905	0.404	120.7238
47	0101111	0.3563	-128.571	0.1271	102.8571	0.5148	154.2857
48	0110000	0.5148	77.1429	0.3563	154.2857	0.1271	-128.571
49	0110001	0.404	43.5809	0.404	-162.133	0.404	-146.438
50	0110010	0.2291	77.1429	0.642	154.2857	0.1586	51.4286
51	0110011	0.2291	0	0.642	180	0.1586	-180
52	0110100	0.404	110.7048	0.404	110.7048	0.404	-110.705
53	0110101	0.1586	77.1429	0.2291	154.2857	0.642	-128.571
54	0110110	0.2291	154.2857	0.642	128.5714	0.1586	-77.1429
55	0110111	0.1271	-102.857	0.5148	154.2857	0.3563	-128.571
56	0111000	0.642	102.8571	0.1586	-154.286	0.2291	128.5714
57	0111001	0.404	84.9905	0.404	-120.724	0.404	172.1523
58	0111010	0.404	120.7238	0.404	172.1523	0.404	84.9905
59	0111011	0.1271	102.8571	0.5148	-154.286	0.3563	128.5714
60	0111100	0.642	128.5714	0.1586	77.1429	0.2291	-154.286
61	0111101	0.3563	128.5714	0.1271	-102.857	0.5148	-154.286
62	0111110	0.5148	154.2857	0.3563	128.5714	0.1271	102.8571
63	0111111	0.2857	-180	0.2857	180	0.2857	-180
64	1000000	0.2857	0	0.2857	0	0.2857	0
65	1000001	0.5148	-25.7143	0.3563	-51.4286	0.1271	-77.1429
66	1000010	0.3563	-51.4286	0.1271	77.1429	0.5148	25.7143
67	1000011	0.642	-51.4286	0.1586	-102.857	0.2291	25.7143
68	1000100	0.1271	-77.1429	0.5148	25.7143	0.3563	-51.4286
69	1000101	0.404	-59.2762	0.404	-7.8477	0.404	-95.0095
70	1000110	0.404	-95.0095	0.404	59.2762	0.404	-7.8477
71	1000111	0.642	-77.1429	0.1586	25.7143	0.2291	-51.4286
72	1001000	0.1271	77.1429	0.5148	-25.7143	0.3563	51.4286
73	1001001	0.2291	-25.7143	0.642	-51.4286	0.1586	102.8571
74	1001010	0.1586	-102.857	0.2291	-25.7143	0.642	51.4286
75	1001011	0.404	-69.2952	0.404	-69.2952	0.404	69.2952
76	1001100	0.2291	180	0.642	0	0.1586	0
77	1001101	0.2291	-102.857	0.642	-25.7143	0.1586	-128.571
78	1001110	0.404	-136.419	0.404	17.8666	0.404	33.562
79	1001111	0.5148	-102.857	0.3563	-25.7143	0.1271	51.4286
80	1010000	0.3563	51.4286	0.1271	-77.1429	0.5148	-25.7143
81	1010001	0.404	7.8477	0.404	-95.0095	0.404	-59.2762
82	1010010	0.1586	0	0.2291	180	0.642	0
83	1010011	0.404	-33.562	0.404	-136.419	0.404	-17.8666
84	1010100	0.1586	102.8571	0.2291	25.7143	0.642	-51.4286
85	1010101	0.1586	-25.7143	0.2291	-51.4286	0.642	-77.1429
86	1010110	0.1586	-128.571	0.2291	102.8571	0.642	-25.7143
87	1010111	0.3563	-77.1429	0.1271	-154.286	0.5148	-51.4286
88	1011000	0.404	95.0095	0.404	-59.2762	0.404	7.8477
89	1011001	0.2291	51.4286	0.642	-77.1429	0.1586	-25.7143
90	1011010	0.1586	128.5714	0.2291	-102.857	0.642	25.7143

91	1011011	0.1271	-51.4286	0.5148	-102.857	0.3563	25.7143
92	1011100	0.404	136.4191	0.404	-17.8666	0.404	-33.562
93	1011101	0.1271	154.2857	0.5148	-51.4286	0.3563	-77.1429
94	1011110	0.3563	180	0.1271	0	0.5148	0
95	1011111	0.2857	-128.571	0.2857	-77.1429	0.2857	-25.7143
96	1100000	0.5148	25.7143	0.3563	51.4286	0.1271	77.1429
97	1100001	0.642	0	0.1586	0	0.2291	180
98	1100010	0.404	-7.8477	0.404	95.0095	0.404	59.2762
99	1100011	0.642	-25.7143	0.1586	128.5714	0.2291	102.8571
100	1100100	0.2291	25.7143	0.642	51.4286	0.1586	-102.857
101	1100101	0.404	-17.8666	0.404	33.562	0.404	-136.419
102	1100110	0.2291	-51.4286	0.642	77.1429	0.1586	25.7143
103	1100111	0.5148	-51.4286	0.3563	77.1429	0.1271	-154.286
104	1101000	0.404	59.2762	0.404	7.8477	0.404	95.0095
105	1101001	0.404	17.8666	0.404	-33.562	0.404	136.4191
106	1101010	0.1586	25.7143	0.2291	51.4286	0.642	77.1429
107	1101011	0.3563	-25.7143	0.1271	-51.4286	0.5148	102.8571
108	1101100	0.2291	102.8571	0.642	25.7143	0.1586	128.5714
109	1101101	0.1271	0	0.5148	0	0.3563	180
110	1101110	0.1271	-154.286	0.5148	51.4286	0.3563	77.1429
111	1101111	0.2857	-77.1429	0.2857	25.7143	0.2857	128.5714
112	1110000	0.642	51.4286	0.1586	102.8571	0.2291	-25.7143
113	1110001	0.642	25.7143	0.1586	-128.571	0.2291	-102.857
114	1110010	0.404	33.562	0.404	136.4191	0.404	17.8666
115	1110011	0.5148	0	0.3563	180	0.1271	0
116	1110100	0.404	69.2952	0.404	69.2952	0.404	-69.2952
117	1110101	0.3563	25.7143	0.1271	51.4286	0.5148	-102.857
118	1110110	0.1271	51.4286	0.5148	102.8571	0.3563	-25.7143
119	1110111	0.2857	-25.7143	0.2857	128.5714	0.2857	-77.1429
120	1111000	0.642	77.1429	0.1586	-25.7143	0.2291	51.4286
121	1111001	0.5148	51.4286	0.3563	-77.1429	0.1271	154.2857
122	1111010	0.3563	77.1429	0.1271	154.2857	0.5148	51.4286
123	1111011	0.2857	25.7143	0.2857	-128.571	0.2857	77.1429
124	1111100	0.5148	102.8571	0.3563	25.7143	0.1271	-51.4286
125	1111101	0.2857	77.1429	0.2857	-25.7143	0.2857	-128.571
126	1111110	0.2857	128.5714	0.2857	77.1429	0.2857	25.7143
127	1111111	0	0	0	0	0	0

3. Conventional Space Vector PWM Scheme

As emphasised in [17], the number of applied active space vectors for multi-phase VSI with an odd phase number should be equal to $(n-1)$, n is the number of phases of inverter, for sinusoidal output. This means that one needs to apply six active vectors in each switching period, rather than two or four for obtaining sinusoidal output. Thus six active vectors and one zero vector is chosen to implement the SVPWM. The switching pattern and the sequence of the space vectors for this scheme is illustrated in Fig. 5. It is observed from the switching pattern of Fig. 5 that the switching in all the phases are staggered i.e. all switches change state at different instants of time. The total number of switching in each switching period is still twenty-eight, thus preserving the requirement that each switch changes state only twice in a switching period.

Using equal volt-second criterion, For sector I, the following is obtained;

$$
\begin{aligned}
v_{d-q} &= 0.642\delta_1 + 0.5148\delta_{15} + 0.2857\delta_{71} \\
v_{x1-y1} &= 0.1586\delta_1 - 0.3563\delta_{15} + 0.2857\delta_{71} \\
v_{x2-y2} &= -0.2291\delta_1 + 0.1272\delta_{15} + 0.2857\delta_{71}
\end{aligned} \tag{3}
$$

Where δ_1, δ_{15}, δ_{71} are duty cycles and suffixes denote the vector numbers, their co-efficiants are their respective magnitudes and negative sign showing their directions which is opposite to normal direction. Solving equation (6) for δ_1, δ_{15} and δ_{71} by assuming v_{d-q} = 0.513 p.u. (maxium achievable output voltage) and v_{x1-y1} and v_{x2-y2} equal to zero, one gets, δ_1 = 0.43338, δ_{15} = 0.3484 and δ_{71} = 0.1926. The time of application of zero space vectors is now given as $t_0 = t_s - t_{a1} - t_{a2} - t_{a3} - t_{b1} - t_{b2} - t_{b3}$ where t_{a1}, t_{a2}, t_{a3}, t_{b1}, t_{b2} and t_{b3} are timings of vectors respectively.

It is seen that the maximum available output voltage with this SVPWM method is $0.513V_{dc}$.

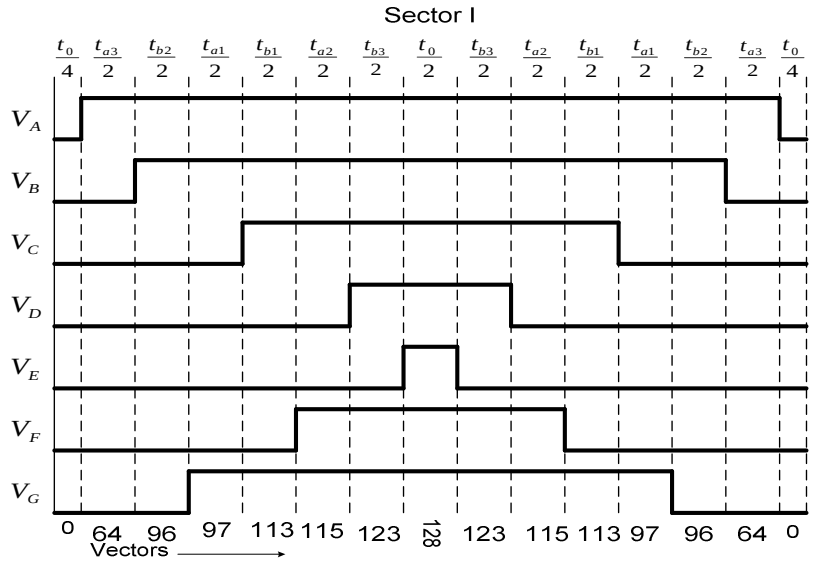


Figure 5 Switching pattern and space vector disposition for one cycle of operation

4. Proposed Time Equivalent Space Vector PWM Scheme

The presented modulation called here "Time Equivalent Space Vector PWM (TESVPWM)" utilises simply the sampled reference voltages to generate the gating time for which each inverter leg to yield sinusoidal output. This method is an extension of the technique developed for a three-phase VSI [20]. The major advantage offered by the proposed scheme is its flexible nature as relocation of "effective time" within the switching period results in various types of PWM scheme such as carrier-based, SVPWM and discontinuous modulation. Additionally the computation time is greatly reduced as the sector identification and reference of lookup table is not used in the proposed algorithm contrary to the conventional SVPWM techniques elaborated in the previous section. In the proposed algorithm the reference voltages are sampled at fixed time interval equal to the switching time of the inverter. The sampled amplitudes are converted to equivalent time signals. The time signals thus obtained are imaginary quantities as they will be negative for negative reference voltage amplitudes. Thus a time offset is added to these signals to obtain the real gating time of each inverter leg. This offset addition centers the active switching vectors within the switching interval offering high performance PWM similar to SVPWM. The algorithm is given below, Where *Vx; x=a,b,c,d,e,f,g*; is the sampled amplitudes of reference phase voltages during sampling interval and T_s is the inverter switching period. T_x*; x=a,b,c,d,e,f,g;* are referred as time equivalents of the sampled amplitudes of reference phase voltages. T_{max} and T_{min} are the maximum and minimum values of *Tx* during sampling interval. T_o is the time duration for which the zero vectors is applied in the switching interval. T_{offset} is the offset time when added to time equivalent becomes gating time signal or the inverter leg switching time $T_{gx;}$*x=a,b,c,d,e,f,g* [8].

Algorithm of the proposed TESVPWM:

(a) Sample the reference voltages V_a, V_b, V_c, V_d, V_e, V_f & V_g in every switching period T_s.
(b) Determine the equivalent times T_1,T_2, T_3,T_4, T_5, T_6 & T_7 given by expreesion,

where x *a,b,c,d,e,f and g;* $T_{xs} = V_{xs} \times \frac{T_S}{V_{dc}}$;

(c) Determine T_{offset}; $T_{offset} = \frac{T_S}{2} - \frac{T_{\max} + T_{\min}}{V_{dc}}$

(d) Then the inverter leg switching times are obtained as
$T_{gx} = T_x + T_{offset;}$ x = *a,b,c,d,e,f and g.*

Fig. 6 shows the principal of Time Equivalent method for seven-phase, if one fundamental cycle of modulating signal is divided into ten equal parts (sectors) and sampling is done in the first part then the equivalent mathematical analysis for first part is given below and on the basis of this analysis the equivalent switching wave form is shown in Fig. 7.

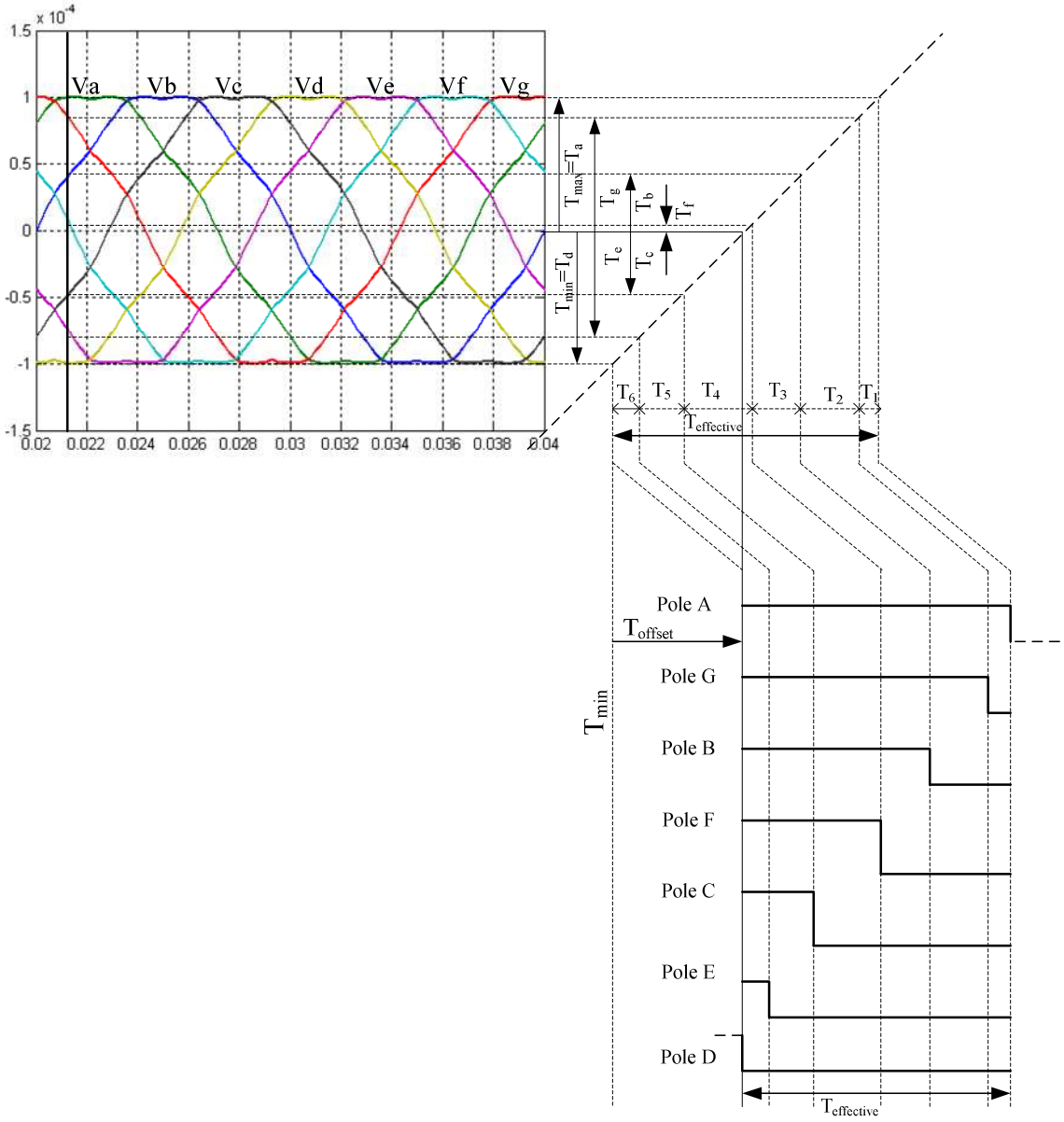


Figure 6 Principal of TESVPWM for sector 1

Sector1

$T_{max} = T_a$; $T_{min} = T_d$;

$T_{effective} = T_{max} - T_{min} = T_a - T_d$

$$T_{offset} = \frac{T_0}{2} - T_{min} = \frac{T_0}{2} - T_d;$$

$$T_1 = T_a - T_g; \quad T_2 = T_g - T_b; \quad T_3 = T_b - T_f;$$

$$T_4 = T_f - T_c; \quad T_5 = T_c - T_e; \quad T_6 = T_e - T_d;$$

$$T_{ga} = T_a + T_{offset} = T_a + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_1 + T_2 + T_3 + T_4 + T_5 + T_6;$$

$$T_{gb} = T_b + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_3 + T_4 + T_5 + T_6;$$

$$T_{gc} = T_c + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_5 + T_6;$$

$$T_{gd} = T_d + \frac{T_0}{2} - T_d = \frac{T_0}{2};$$

$$T_{ge} = T_e + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_6;$$

$$T_{gf} = T_f + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_4 + T_5 + T_6;$$

$$T_{gg} = T_g + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_2 + T_3 + T_4 + T_5 + T_6;$$

From the switching waveform of Fig. 7, for first part the space vectors used are 64,65,97,99,115 and 119 for the implementation of modulation scheme. Their positions in the *d-q* plane can be seen in Fig. 3 and in *x-y* plane in Fig. 4.

The proposed TESVPWM is simulated using Matlab/Simulink model shown . The seven-phase voltage is provided with amplitude equals to ± 0.5 V_{DC} and V_{DC} is kept unity. The switching frequency is chosen equal to 5 KHz.

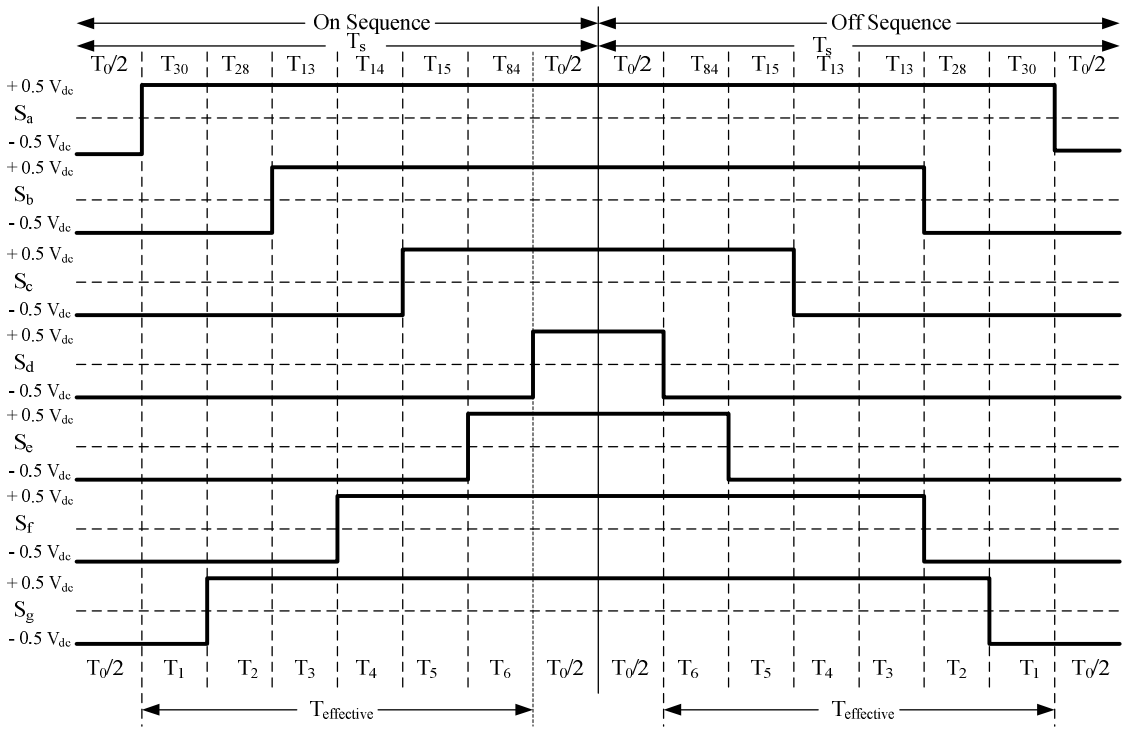
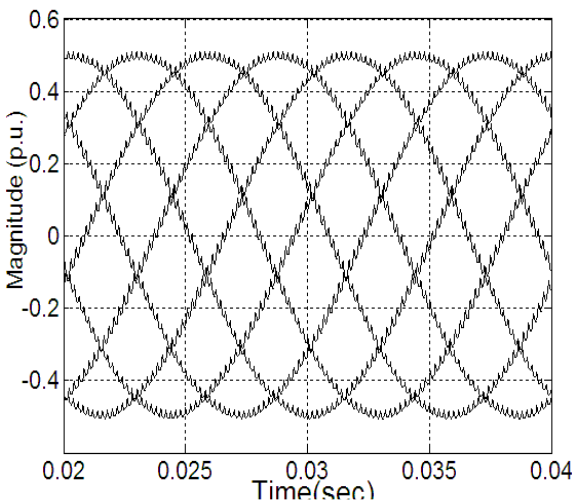


Figure7 Switching waveform for sector 1

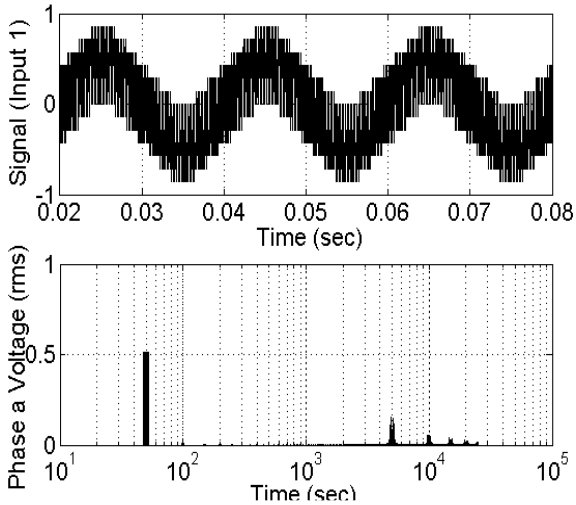
5. Simulation Results

Simulation results are provided in Fig. 8. Fig. 8(a) shows the filtered output voltage after connecting a R-L load at the output terminals and Fig. 8(b) shows the harmonic spectrum for the output phase 'a' voltage and Fig. 8(c)

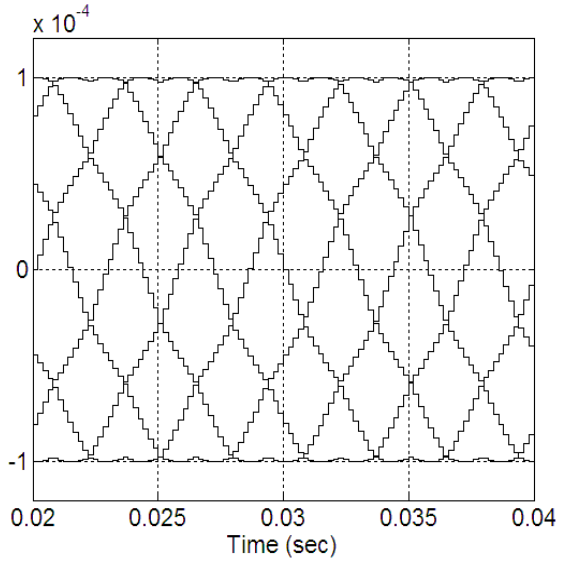
shows the offset time signals as calculated after the mathematical analysis; it shows both the maximum value as well as the minimum value for the offset and the offset time signal. Fig. 8(d) shows the net modulating signals after adding the offset signal to equivalent time signal for each phase. Thus it can be concluded that the output of this scheme is similar to the one offered by the space vector PWM. The maximum modulation index obtained here is 0.515.



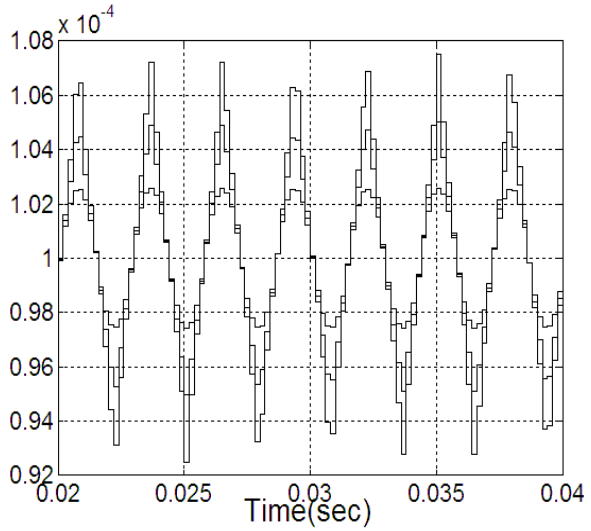
(a) Filtered Output voltage



(b)Harmonic spectrum phase 'a' voltage



(c) Offset time signals



(d) Modulating signals

Figure 8 simulation results using TSVPWM

Table 2 Vectors used for TESVPWM in different sectors

Sector No.	Vectors	Sector No.	Vectors
1	64,65,97,99,115,119	6	8,12,28,30,62,63
2	64,96,97,113,121,123	7	4,12,14,30,31,63
3	32,48,112,120,121,125	8	2,6,7,15,79,95
4	16,48,56,120,124,125	9	2,3,7,71,79,111
5	16,24,56,60,62,126	10	1,3,67,71,103,111

6. Experimental Investigation

Experimental investigation is performed to implement the proposed scheme for a seven-phase VSI. Three standard three-phase VSIs are used to provide seven-phase output. The DC link is paralleled to make it common for all the three modules. The DSP TMS320F2812 has provision of generating four independent PWM outputs per event manager thus a maximum of eight-phase inverter can be controlled using one DSP. Out of five PWM, three are generated using full compare units and the other one is generated by the GP timer compares units. The full compare unit has programmable dead-band for PWM output pairs but the other one PWM channel does not have the provision of dead band. Thus a dead band generating circuit is fabricated which act upon those PWM signals which do not have inbuilt dead band. A distribution panel is developed which distributes the fourteen PWM signals generated from DSP to three power modules. The schematic of a DSP based seven-phase VSI is presented in Fig. 9 and Fig. 10 shows the Switching pattern for seven-phase VSI using TESVPWM, during one switching period in sector 1. Fig 11 shows the filtered output phase to neutral output for sinusoidal voltages.

Seven phase voltage setup

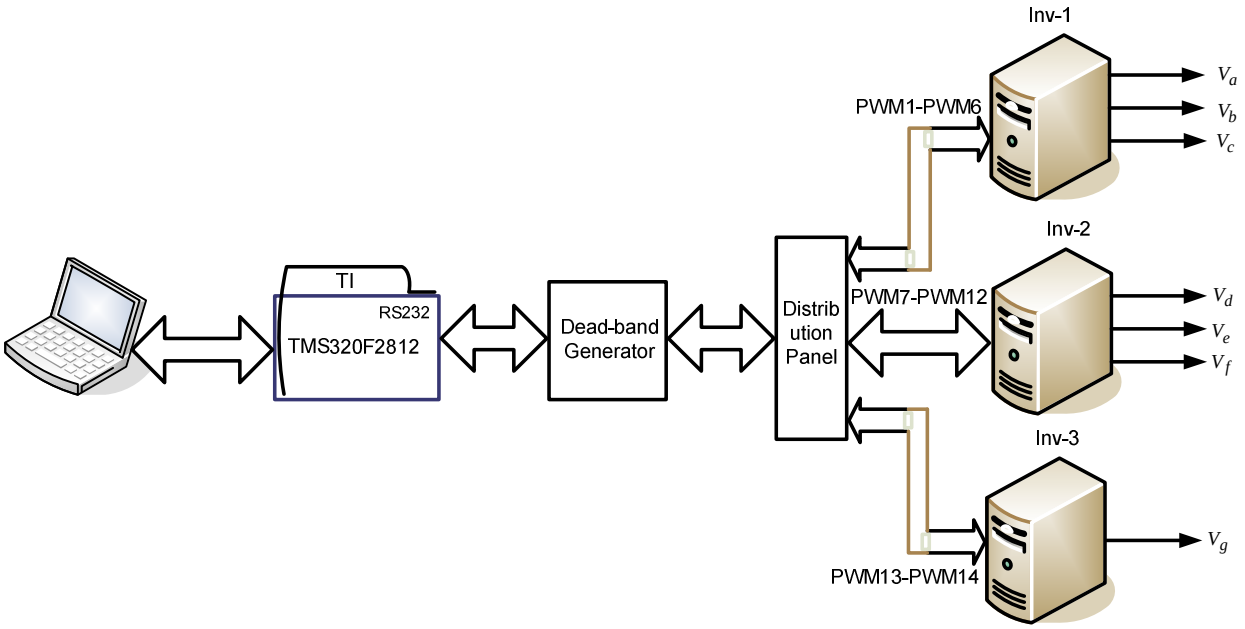


Figure. 9 Block schematic of a DSP based seven-phase VSI.

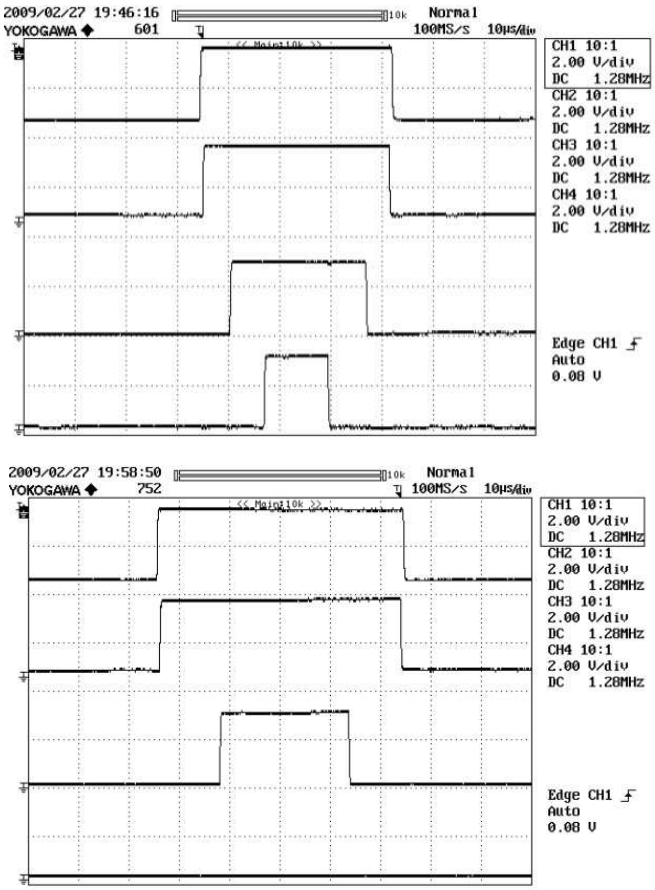


Figure. 10 Switching pattern for seven-phase VSI using TESVPWM, during one switching period in sector 1. Inverter legs *A*, *B*, *C* and D in upper part and inverter legs *E*, *F* and *G* in lower part

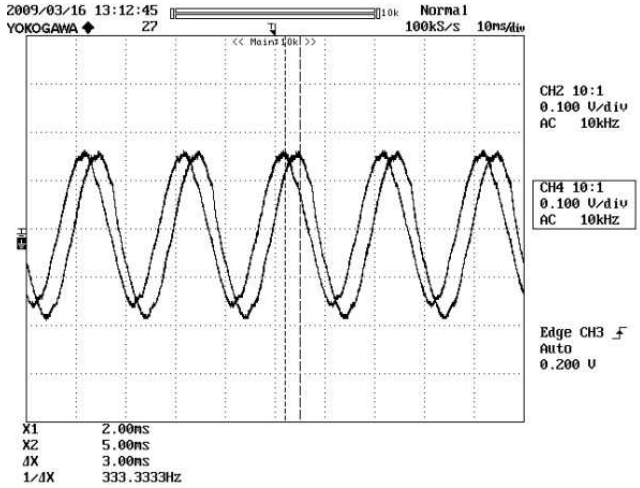


Figure 11. Filtered phase to neutral voltage for sinusoidal output

7. Conclusion

In this paper a simple voltage modulation technique is presented and is designated as time equivalent SVPWM for seven-phase voltage source inverter. In the proposed method, reference space vector is sampled at a regular interval to determine the inverter switching vectors and their time durations in a sampling interval. These equivalent times are then converted to the actual gating time of each leg. In comparison with the present convention SVPWM schemes, in the proposed scheme, there is no need to look for sectors, vectors, lookup tables and no need to calculate the time of application for switching vectors. The proposed method offers a simple approach to realise the complex SVPWM algorithm. The output obtainable has the same quality as that of the conventional SVPWM.

The proposed TESVPWM offers major advantages in real time DSP implementation due its computational efficiency. The Matlab/Simulink implementation and their simulation results are provided. The simulation and experimental results matches to good extent.

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