A new brushless DC motor driving resonant pole inverter optimized for batteries

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ABSTRACT

The brushless DC motor (BLDC) has gained significant popularity in industrial settings due to its notable attributes such as low inertia, rapid response, high power density, exceptional dependability, and reputation for being conservation-free. Typically, these are equipped by a tight-switching PWM inverter, which results in significant switching losses. Consequently, the dissipation of switching loss necessitates the use of sizable heat sinks, resulting in an increase in both the physical dimensions and mass of the drive system. Numerous researchers have developed soft switching inverters with the aim of minimizing switching losses. The utilization of a soft-switching circuit may give rise to additional issues, including heightened voltage stress, incomplete pulse width modulation control, and intricate control scheme or implementation. The present study introduces a basic soft-switching circuit that is suitable for employment in BLDC drive systems powered by batteries. The inverter exhibits low loss for power switching and voltage stress is less on the main switches, while also featuring a straightforward control scheme that is easily implementable. Upon conducting analytical analysis, simulation results were presented by evaluating the theoretical analysis.

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1. INTRODUCTION
The brushless DC motor (BLDC) has gained significant popularity among various implementations due to its compact size, high power density, low at maintenance requirements, and exceptional reliability [1], all of which are crucial design considerations [2]. BLDC drives powered by batteries utilize a configuration of parallel and series batteries as their primary power source [3]. Typically, the BLDC motor is powered by a hard-switching PWM inverter, resulting in decreased inverter efficiency and the generation of heat that

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necessitates dissipation through a heat sink [4]. Minimizing switching losses not only results in a reduction in the size of the heat sink, but also extends the endurance of the power source during operation [5], [6].

BLDC motors are often preferred in portable devices due to their economic competitiveness and suitability in various applications when in comparison to different types of electric motors [7]. The utilization of BLDC motors is often limited to scenarios where space is restricted and there is a requirement for optimal torque per volume ratios [8], [9] due to their comparatively higher cost in comparison to other motor types. DC power supplies, such as batteries and ultracapacitors, are commonly utilized as the primary source of power in situations involving vehicles, portable tools [10], and other similar applications [11]. The accessibility of mid-point in batteries and ultra-capacitors is typically free of charge due to their composition of multiple cells arranged in series [12], [13].

In the recent past, a number of soft switching inverters were proposed and can be categorized into three main groups: resonant pole inverter, resonant ac-link inverter, and resonant dc-link inverter [10]. The utilization of a resonant ac-link inverter is deemed unsuitable for the purpose of driving BLDC motors [14]. The implementation of a resonant dc-link inverter [15] results in elevated switches voltage stress and increased dc-link voltage ripple. Quasi-parallel resonant DC-link inverters [16] have been put forward as a solution to address these issues [17], albeit with the drawback of increased conduction losses [18] due to the additional main conduction path [19].

The auxiliary resonant commutated pole inverter (ARCPI) [20] as well as the ordinary resonant snubber inverter have the capability to achieve zero voltage switching (ZVS) without causing any increase in voltage stress over the main switches [21]. Additionally, both inverters are able to attain genuine pulse width modulation (PWM) control [22]. However, the incorporation of two auxiliary switches per phase is necessary [23], thereby resulting in a significant increase in the overall cost of the inverter [24]. The transition inverter [25], employs a solitary auxiliary switch that operates at a significantly higher switching frequency than the main switches [26]. This design feature serves to restrict the switching frequency of the inverter.

Resonant-pole inverters are comprised of a resonant inductor [27] and a pair of resonant capacitors that are connected in parallel with each inverter leg [28]. This particular category of the device allows for individual switching of each leg, resulting in authentic pulse width modulation (PWM) control [29]. Furthermore, the voltage of the DC-link remains unaffected [30], thereby eliminating the necessity for supplementary main path switches. The present study presents a novel resonant pole inverter that is appropriate for battery-powered BLDC motors [31]. This inverter utilizes natural power supplies and eliminates extraneous components, resulting in a straightforward topology and control scheme [32], a compact form factor, and ease of implementation.

2. RESONANT INVERTER TOPOLOGY

In Figure 1, you can see a detailed diagrammatic explanation of anormal controller that is used in BLDC motor drive. In order to produce the gate sequence of the switches of inverter, this controller makes use of a combinatorial logic circuit. The input signals for this logic are provided by these sensors for hall effect or even slotted optical disks, which are included within the motor as position sensors.

Assuming that the gate firing angle pulses are of 120° apart from each other for soft switching drive. The approach for controlling the technique is a PI PWM forward loop that is controlled by current. PWM controllers typically use a switching frequency of 20 KHz for their triangle wave forms. According to what is shown in [10], only the three bottom switches received PWM, and the three top switches only operate when the commutation frequency was on the order of a 100 Hz. According to what is stated in, this causes a smaller ripple in the current. Hence, it is not necessary for the three higher switches to operate when the switching conditions are set to mild.

Figure 2 shows the schematic for the inverter, consisting of three phase inverters with six switches (S₁, S₂, S₃, S₄, S₅, S₆) Three auxiliary switches (S₄, S₅, S₆), three snubber capacitors (Cₐa, Cₐb, Cₐc), an inductor (Lₐ), and a freewheeling diode (Dₐ) serve as the resonant circuit of a conventional three-phase inverter. Three lower main switches, auxiliary switches, and snubber capacitors are all linked in parallel to the outputs of the inverter legs. The midpoint access point and a single side of the inductor are linked. A diode with freewheeling connections is placed between the system ground and the other side of the resonant inductor.

The emitters of the secondary switches are interconnected to one another, it is only necessary to have one supplementary supply for the gate drive. Because the snubber capacitors (Cₐa, Cₐb, Cₐc) can reduce the speed of operation of the voltage rise rate, it is possible for below switches to be off state during the entirety of a PWM cycle when the situation is ZVS. The voltage spike during turn-off can be deleted, and the power losses that occur during the turn-off process can be minimized. It is essential to turn on the secondary switch that corresponds to the lower switch (S₉, S₈, S₇) prior activating the lower switch. After that, the snubber capacitor is allowed to discharge, and the ZVS state is applied to the lower switches. Phase current
commutation involves moving the converting state from one lower switch to another. Switch \( S_2 \), for instance, is switched on while switch \( S_6 \) is turned off. In the ZVS situation, \( S_c \) can also be immediately disabled as an alternative. This enables switch \( S_2 \) to achieve the ZVS condition by allowing the auxiliary switch \( S_c \) to drain the snubber capacitor \( C_{rb} \). The operation is the same as that of the hard switching inverter if the switching state is switched during phase current commutation from one upper switch to another higher switch. This is due to the switching power losses of the upper switches being substantially smaller than those of the lower switches.

**Figure 1. Explanation of controller diagram for BLDC motor**

**Figure 2. Diagrammatic explanation of inverter**

3. OPERATING APPROACHES

This article describes the circumstance in which switch \( S_1 \) is turned at state and switch \( S_2 \) twisted under PWM frequency so that it is more comfortable for the reader. Figure 3 depicts the theoretical wave shapes that this inverter is capable of producing. The same logic applies to the operation of other combinations of upper and lower switches. This circuit is capable of functioning in one of six distinct approaches.

3.1. Approach 0

It is presumable that \( S_6 \) is disabled at the start of each PWM cycle. The motor’s load current, which is assumed to remain constant throughout each PWM cycle, is carried by the anti-parallel diode of \( S_3 \) (D). As a result, the supply voltage, which is determined by the formula \( V_s = V_{hi} + V_{low} \), is charged to the same level as the snubber capacitor, also known as \( C_{sb} \). To avoid a large discharge current running through the capacitor at the start of each cycle, we first discharge the snubber capacitor (\( C_{sb} \)) over a secondary channel.
3.2. Approach 1 ($t_0 < t < t_1$)

The beginning of the resonance cycle is marked by the mounting edge of the firing signal that is supplied for switch $S_6$. At this point (depicted by $t_1$ in Figure 4), the secondary switch $S_b$ will begin to operate. The linear increase in the current via the auxiliary switch is caused by the inductor’s inductance. The current from the inductor flows back into the power supply. One way to characterize the inductor’s voltage and current is as (1). Where $L_r$ denotes the inductance of the resonant inductor. Once the current in inductor equals the current at load, this approach is terminated. This approach duration can be determined by (2).

$$\frac{di_{Lr}}{dt} = \frac{(n-1)V_s}{nL_r} \quad (1)$$
$$\Delta t_1 = t_1 - t_0 = \frac{nL_rI_0}{(n-1)V_s} \quad (2)$$

3.3. Approach 2 ($t_1 < t < t_2$)

Until the moment where the capacitor entirely discharges to zero, the resonant inductor ($L_r$) and snubber capacitor ($C_{rb}$) produce resonance. the start time, the transformer’s current ($i_{Lr}$), and the capacitor’s voltage are all redefined (depicted in Figure 5).

$$\begin{cases} 
    u_{S6} = L_r \frac{di_{Lr}(t)}{dt} + \frac{(n-1)V_s}{n} \\
    -C_r \frac{du_{S6}(t)}{dt} = i_{Lr}(t) - I_0 
\end{cases} \quad (3)$$

In this equation, $C_r$ represents the snubber capacitor $C_{rb}$. The solution to (3) can be used to determine the length of this approach by changing the beginning values (4).

$$\begin{cases} 
    u_{S6}(t) = \frac{(n-1)V_s}{n} \cos(\omega_r t) + \frac{V_s}{n} \\
    i_{Lr}(t) = I_0 + \frac{(n-1)V_s}{n} \frac{C_r}{V_s} \sin(\omega_r t) \quad (4) 
\end{cases}$$

Where $\omega_r = \sqrt{\frac{1}{L_r C_r}}$ by defining $u_{CR}(t) = u_{S6}(t) = 0$, we can find the duration of the resonance in (5).

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r} \left( 1 - \frac{1}{n-1} \right) \quad (5)$$

Interval of this approach is independent of load current. Current of resonance inductor at the end of this approach calculated in (6).
\[ i_{Lr}(t_2) = I_0 + V_s \sqrt{\frac{(n-2)C_r}{nL_r}} \]  

Also, maximum current of inductor can be calculated from (7).

\[ I_{Lr-max} = I_0 + \frac{(n-1)}{n} \frac{V_s}{\sqrt{L_r}} \]  

Figure 4. Circuit explanation for approach 1  
Figure 5. Circuit explanation for approach 2

3.4. Approach 3 \( (t_2<t<t_3) \)

The non-parallel diode known as \( D_{fp} \) includes on when voltage on the \( C_{rb} \) pin approaches zero, and the current flowing through the inductor discharges linearly to zero as it enters the bottom area of the voltage source. The voltage-current relationship of the inductor is described in (8) (depicted in Figure 6).

\[ \frac{di_{Lr}(t)}{dt} = \frac{V_s}{nL_r} \]  

As there is no voltage across the \( S_6 \) as a result, the \( S_6 \) can now be on under ZVS circumstances. With changing the start time and assuming that the approach will end when \( i_{Lr} = 0 \), the length of time it lasts may be calculated. This calculation’s outcomes are shown in (9).

\[ \Delta t_3 = t_3 - t_2 = \sqrt{n(n-2)L_rC_r} \]  

The length of the interval is unaffected by the current at load, as seen in (9). The \( S_6 \) relay needs to be switched to the ZVS state during this time.

3.5. Approach 4 \( (t_3<t<t_4) \)

Here, the current in inductor, denoted by \( i_{Lr} \), continues to as (8). \( S_6 \) and \( S_b \) share an equal portion of the load current. Hence, the remaining current in the inductor linearly decreases until it reaches zero. This current partially passes through \( S_6 \) and \( D_{fp} \). Hence, the length of time that has passed can be stated as (10) (depicted in Figure 7).

\[ \Delta t_4 = t_4 - t_3 = \frac{nL_rI_0}{V_s} \]  

As there is no voltage across the auxiliary switch \( S_b \) when operating in this approach (due to the fact that both \( S_6 \) and \( D_{fp} \) are conducting), the switch is able to be off when ZVS is met.

3.6. Approach 5 \( (t_4<t<t_5) \)

The resonant circuit is not being used and the current across the inductor is 0, and the circuit is operating in a hard switching mode, where the switches are turned ON and OFF without any consideration for the inductor current waveform. This hard switching PWM converter would likely have higher switching losses and potentially lower efficiency compared to converters that utilize resonant or soft switching techniques.
3.7. Approach 6 ($t_5 < t < t_6$)

Directly turning off $S_6$ prevents the resonance circuit from functioning properly. During the turn-off period, the snubber capacitor $C_{rb}$ ensures that the voltage on $S_6$ remains at zero, thereby preparing the ZVS condition. The length of this interval can also be determined using (11) to a straightforward rule on the rate of current decay in capacitors.

$$\Delta t_5 = t_5 - t_6 = \frac{C_{rb} V_s}{I_0}$$  \hspace{1cm} (11)

The second period will now begin in approach 0, with the load current flowing through the freewheeling diode $D_{fp}$. $S_6$ can be started to turn off instantly in ZVS condition (similar to approach 6), turning on supplementary switch $S_c$ to discharge the snubber capacitor $C_{rc}$, and then switching $S_2$ to ZVS condition. Phase current commutation changes the switching state from one lower switch to another (for example, turning off $S_8$ and turning on $S_2$) (similar to approaches 1–4).

4. SIMULATION RESULTS

For simulation, the following parameters are considered. The switching frequency is 20 KHz, the stator has an inductance of 1.6 mH and a resistance of 172 ohms. The capacitance of each snubber capacitor is measured to be 47 nF, whereas the resonant inductor's inductance is 7.5 H.

The Figure 8 shows the gate signals for switches of inverter. These gate signals help in switching on and off at regular intervals in logical sequence. The primary switch's delay time in respect to the PWM pulse is 2.2 µS, while the auxiliary switch's pulse width is 4.5 S. Figure 9 represents the current and voltage waveforms of ARCPI inverter switches. The extreme load current conditions are considered as 25 A and the DC link voltage is adjusted to 300 V when the motor is taken as 3.3 KW BLDC Motor with $V_{peak}$ value is 139 V.

Figure 10 represents the speed signal of BLDC motor without feedback. The motor speed is reaching to maximum and due to error signal; it droops to minimum value. Figure 11 represents line current and line voltage of BLDC motor. Figure 12 represents three phase voltage signals to motor input signal.
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Figure 13 represents the current at the motor and speed signal output at the BLDC motor with feedback from motor to PI controller. The speed output waveform represents a stable output after connecting a closed loop feedback signal with a value of 1390 rpm. Figure 14 represents the torque of BLDC motor after closed loop feedback signal from motor to PI controller.

5. CONCLUSION

The present study introduces a specialized soft switching converter designed for the purpose of driving a BLDC motor through battery power. The converter in question employs a distinct pulse width modulation (PWM) converter and leverages the inherent characteristics of said supply of energy to streamline the topology and minimize resonant components. The veracity of the put forth topology and algorithm is validated through software simulation under both full-load and 10% of full load conditions. Based on the outcomes of the simulation, these conclusions can be drawn. All switches that are controlled by pulse width modulation (PWM) and operate at high frequencies are designed to function under soft switching conditions.

The voltage stress experienced by both the primary and secondary switches is restricted to the direct current link voltage. Under the ZCS condition, all auxiliary switches are activated, while under the ZVZCS condition, they are deactivated. The implementation of D_{fp}, when deactivated when zero current condition, which effectively mitigates the issue of reverse recovery in diodes. The regular functioning of the inverter remains unaltered. Due to the high switching frequency of 20 kHz, it is possible to eliminate acoustic noise and mitigate the impact of inverter output harmonics on motor ripple.

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